DVD-Video Recorder

DVDR880 & DVDR890

/001 /021 /051

Service
Service
Service

PHILIPS
LETS RECORD DVD
TR 01001_001
080502

ServiceManual

CLASS 1
LASER PRODUCT

DVD+ReWritable

DVD VIDEO

COMPACT disc DIGITAL VIDEO

COMPACT disc DIGITAL AUDIO

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PHILIPS

1. Technical Specifications and Connection Facilities

1.1 General:

Mains voltage : 198V-276V
Mains frequency : 43 Hz - 63Hz
Power consumption mains : 28 W
Power consumption standby : < 7 W
Power consumption low power stand-by : < 3 W

1.2 RF Tuner

Test equipment:Fluke 54200 TV Signal generator
Test streams:PAL BG Philips Standard test pattern

1.2.1 System:

PAL B/G, PAL D/K, SECAM L/L’, PAL I

1.2.2 RF - Loop Through:

Frequency range : 45 MHz - 860 MHz
Gain: (ANT IN - ANT OUT) : -6 dB to 0dB

1.2.3 Radio Interference:

input voltage /3 tone method (+40 dB min) : no limit

1.2.4 Receiver:

PLL tuning with AFC for optimum reception
Frequency range: : 45.25 MHz - 857 MHz
Sensitivity at 40 dB S/N : ≥ 60dBµV at 75Ω (video unweighted)

1.2.5 Video Performance:

Channel 25 / 503,25 MHz,
Test pattern: PAL BG PHILIPS standard test pattern,
RF Level 74 dBV
Measured on SCART 1
Frequency response: : 0 - 4.00 MHz +0-4dB
Group delay (0.1 MHz - 4.4 MHz) : 0 nsec ± 150nsec

1.2.6 Audio Performance:

Audio Performance Analogue - HiFi:
Frequency response at SCART 1 (L+R) output: : 100 Hz - 12 kHz / 0± 3dB
S/N according to DIN 45405, 7, 1967 : and PHILIPS standard test pattern video signal: : FM: ≥ 50dB; AM ≥ 45dB, unweighted
Harmonic distortion (1 kHz, ± 25 kHz deviation): : FM ≤ 1.5%; AM ≤ 2%

Audio Performance NICAM:
Frequency response at SCART 1(L+R) output: : 40 Hz - 15 kHz 0 ± 3dB
S/N according to DIN 45405, 7, 1967 : and PHILIPS standard test pattern video signal: : ≥ 60 dB unweighted
Harmonic distortion (1 kHz): : ≤ 0.5 %

1.2.7 Tuning

Automatic Search Tuning
scanning time without antenna : typ. 3 min. PAL
stop level (vision carrier) : ≥ 37dBµV
Maximum tuning error of a recalled program : ± 62.5 kHz
Maximum tuning error during operation : ± 100 kHz

Tuning Principle
automatic B,G, I, DK and L/L’detection
manual selection in "STORE" mode

1.3 Analogue Inputs

1.3.1 SCART 1 (Connected to TV)

Pin Signals:
1 - Audio R 1.8V RMS
2 - Audio R
3 - Audio L 1.8V RMS
4 - Audio GND
5 - Blue/Chroma GND
6 - Audio L
7 - Blue out/ Chroma in 0.7Vpp ± 0.1V into 75 Ohm (*)
8 - Function switch <2V = TV
>4.5V / <7V = asp. ratio 16:9 DVD
>9.5V / <12V = asp. ratio 4:3 DVD
9 - Green GND
10 - P50 control
11 - Green 0.7Vpp ± 0.1V into 75 Ohm (*)
12 - Nc
13 - Red/Chroma GND
14 - fast switch GND
15 - Red out/ Chroma out 0.7Vpp ± 0.1V into 75 Ohm (*)
± 3dB 0.3Vpp Chroma (burst)
16 - fast switch RGB/ CVBS or Y <0.4V into 75 Ohm = CVBS
>1V / <3V into 75 Ohm = RGB
17 - Y/CVBS GND
OUT
18 - Y/CVBS GND
IN
19 - CVBS/Y 1Vpp ± 0.1V into 75 Ohm (*)
20 - CVBS/Y
21 - Shield

1.3.2 SCART 2 (Connected to AUX)

Pin Signals:
1 -Audio R 1.8V RMS
2 -Audio R
3 -Audio L 1.8V RMS
4 -Audio GND
5 -Blue/Chroma GND
6 -Audio L
7 -Blue in/ Chroma out ± 3dB 0.3Vpp Chroma (burst)
8 -Function switch
9 -Green GND
10 -P50 control

11 -Green
12 -Nc
13 -Red/Chroma GND
14 -fast switch GND
15 -Red in/ Chroma in
16 -fast switch RGB/ CVBS or Y
17 -CVBS GND OUT
18 -CVBS GND IN
19 -CVBS/Y/RGB sync 1Vpp ± 0.1V into 75 Ohm (*)
20 -CVBS/Y
21 -Shield

(*) for 100% white

1.3.3 Audio/Video Front Input Connectors

Audio
Input voltage : 2 Vrms
Input impedance : >10kΩ

Video - Cinch
Input voltage : 1 Vpp ± 3dB
Input impedance : 75 Ω

Video - YC (Hosiden)
Input voltage Y : 1Vpp ± 3dB
Input impedance Y : 75 Ω
Input voltage C : burst 300 mVpp ± 3 dB
Input impedance C : 75 Ω

1.4 Video Performance

All outputs loaded with 75 Ohm
SNR measurements over full bandwidth without weighting.

1.4.1 SCART (RGB)

SNR : > -65 dB on all output
Bandwidth : 4.8 MHz ± 2dB

1.5 Audio Performance CD

1.5.1 Cinch Output Rear

Output voltage 2 channel mode : 2Vrms ± 2dB
Channel unbalance (1kHz) : <1dB
Crosstalk 1kHz : >95dB
Crosstalk 20Hz-20kHz : >85dB
Frequency response 20Hz- 20kHz : ±0.2dB max
Signal to noise ratio : >95 dB
Dynamic range 1kHz : >85dB
Dynamic range 20Hz-20kHz : >80dB
Distortion and noise 1kHz : >85dB
Distortion and noise 20Hz-20kHz : >75dB
Intermodulation distortion : >77dB
Mute : >95dB
Outband attenuation: : >40dB above 30kHz

1.5.2 Scart Audio

Output voltage 2 channel mode : 1.6Vrms ± 2dB
Channel unbalance (1kHz) : <1dB
Crosstalk 1kHz : >85dB
Crosstalk 20Hz-20kHz : >70dB
Frequency response 20Hz- 20kHz : ± 0.2dB max
Signal to noise ratio : >85 dB
Dynamic range 1kHz : >75dB
Dynamic range 20Hz-20kHz : >70dB
Distortion and noise 1kHz : >75dB
Distortion and noise 20Hz-20kHz : >65dB
Intermodulation distortion : >70dB
Mute (spin-up, pause, access) : >85dB
Outband attenuation: : >40dB above 25kHz

1.6 Digital Output

1.6.1 Coaxial

CDDA/ LPCM (incl MPEG1) : according IEC958
MPEG2, AC3 audio : according IEC1937
DTS : according IEC1937, amendment 1

1.7 Digital Video Input (IEEE 1394)

1.7.1 Applicable Standards

Implementation according:
IEEE Std 1394-1995
IEC 61883 - Part 1
IEC 61883 - Part 2 SD-DVCR (02-01-1997)
Specification of consumer use digital VCR's using 6.3 mm magnetic tape - dec.1994
Mechanical connection according:
Annex A of 61883-1

1.8 P50 System Control

Via SCART pin nr 10

1.9 Dimensions and Weight

Height of feet : 10mm
Apparatus tray closed : WxDxH :435 x 324.5 x 88cm
Apparatus tray open : WxDxH :435 x 366 x 88cm
Weight without packaging : app. 4 kg ± 0.5 kg
Weight in packaging : app. 6.5 kg

1.10 Laser Output Power & Wavelength

1.10.1 DVD

Output power during reading : 0.8mW
Output power during writing : 20mW
Wavelength : 660nm

1.10.2 CD

Output power : 0.3mW
Wavelength : 780nm

2. Safety Information, General Notes

2.1 Safety Instructions

2.1.1 General Safety

Safety regulations require that during a repair:

- Connect the unit to the mains via an isolation transformer.
- Replace safety components, indicated by the symbol , only by components identical to the original ones. Any other component substitution (other than original type) may increase risk of fire or electrical shock hazard.

Safety regulations require that after a repair, you must return the unit in its original condition. Pay, in particular, attention to the following points:

- Route the wires/cables correctly, and fix them with the mounted cable clamps.
- Check the insulation of the mains lead for external damage.
- Check the electrical DC resistance between the mains plug and the secondary side:
  1. Unplug the mains cord, and connect a wire between the two pins of the mains plug.
  2. Set the mains switch to the 'on' position (keep the mains cord unplugged!).
  3. Measure the resistance value between the mains plug and the front panel, controls, and chassis bottom.
  4. Repair or correct unit when the resistance measurement is less than 1 MΩ.
  5. Verify this, before you return the unit to the customer/user (ref. UL-standard no. 1492).
  6. Switch the unit ‘off’, and remove the wire between the two pins of the mains plug.

2.1.2 Laser Safety

This unit employs a laser. Only qualified service personnel may remove the cover, or attempt to service this device (due to possible eye injury).

Laser Device Unit

Type	Semiconductor laser GaAlAs
Wavelength	650 nm (DVD) 780 nm (VCD/CD)
Output Power	20 mW (DVD+RW writing) 0.8 mW (DVD reading) 0.3 mW (VCD/CD reading)
Beam divergence	60 degree

CLASS 1
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Figure 2-1

Note: Use of controls or adjustments or performance of procedure other than those specified herein, may result in hazardous radiation exposure. Avoid direct exposure to beam.

2.2 Warnings

2.2.1 General

- All ICs and many other semiconductors are susceptible to electrostatic discharges (ESD,). Careless handling during repair can reduce life drastically. Make sure that, during repair, you are at the same potential as the mass of the set by a wristband with resistance. Keep components and tools at this same potential.
  Available ESD protection equipment:
  - Complete kit ESD3 (small tablemat, wristband, connection box, extension cable and earth cable) 4822 310 10671.
  - Wristband tester 4822 344 13999.
- Be careful during measurements in the live voltage section. The primary side of the power supply (pos. 1005), including the heatsink, carries live mains voltage when you connect the player to the mains (even when the player is 'off'!). It is possible to touch copper tracks and/or components in this unshielded primary area, when you service the player. Service personnel must take precautions to prevent touching this area or components in this area. A 'lightning stroke' and a stripe-marked printing on the printed wiring board, indicate the primary side of the power supply.
- Never replace modules, or components, while the unit is ‘on’.

2.2.2 Laser

- The use of optical instruments with this product, will increase eye hazard.
- Only qualified service personnel may remove the cover or attempt to service this device, due to possible eye injury.
- Repair handling should take place as much as possible with a disc loaded inside the player.
- Text below is placed inside the unit, on the laser cover shield:

CAUTION VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID EXPOSURE TO BEAM
ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING VED ÅBNING UNDGÅ UDSÆTTELSE FOR STRÅLING
ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING NÅR DEKSEL ÅPNES UNNGÅ EKSPONERING FOR STRÅLEN
VARNING SYNLIG OCH OSYNLIG LASERSTRÅLNING NÄR DENNA DEL ÄR ÖPPNAD BETRAKTA EJ STRÅLEN
VARO! AVATT AESSA OLET ALTTIINA NÄKYVÄLLE JA NÄKYMÄTTÖMÄLLE LASER SÄTEILYLLE. ÄLÄ KATSO SÄTEESEEN
VORSICHT SICHTBARE UND UNSICHTBARE LASERSTRAHLUNG WENN ABDECKUNG GEÖFFNET NICHT DEM STRAHL AUSSETSEN
DANGER VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID DIRECT EXPOSURE TO BEAM
ATTENTION RAYONNEMENT LASER VISIBLE ET INVISIBLE EN CAS D'OUVERTURE EXPOSITION DANGEREUSE AU FAISCEAU

Figure 2-2

2.2.3 Notes

Dolby
Manufactered under licence from Dolby Laboratories. “Dolby”, “Pro Logic” and the double-D symbol are trademarks of Dolby Laboratories. Confidential Unpublished Works.
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DOLBY SURROUND
PRO • LOGIC

Figure 2-3

Trusurround
TRUSURROUND, **SRS** and symbol (fig 2-4) are trademarks of SRS Labs, Inc. TRUSURROUND technology is manufactured under licence frm SRS labs, Inc.

®

Figure 2-4

Video Plus

“Video Plus+” and “PlusCode” are registered trademarks of the Gemstar Development Corporation. The “Video Plus+” system is manufactored under licence from the Gemstar Development Corporation.

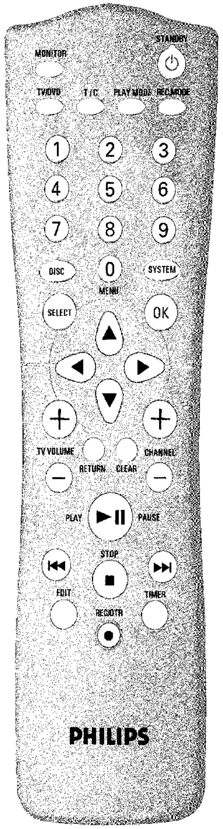
Figure 2-5

Macrovision

This product incorporates copyright protection technology that is protected by method claims of certain U.S. patents and other intellectual property rights owned by Macrovision Corporation and other rights owners.

Use of this copyright protection technology must be autorized by Macrovision Corporation, and is intended for home and other limited viewing uses only unless otherwise authorized by Macrovision Corporation. Reverse engineering or disassembly is prohibited.

3. Directions For Use



The remote control

ENGLISH

MONITOR	**Monitor**: This button lets you switch between the (internal) TV tuner in the DVD recorder (TV picture on the TV set) and playback on the DVD recorder
STANDBY ⏻	**Switch on or off**: To switch set on or off, interrupt menu function, interrupt a programmed recording (TIMER)
TV/DVD	**TV/DVD switch**: Switches the scart socket **EXT 2 AUX I/O** directly to the TV set. This lets you watch the picture from any unit connected to this scart socket (set-top box', video recorder or satellite receiver) and at the same time record from another source. If you have not connected a device to scart socket **EXT 2 AUX I/O** you can use this button to switch between TV reception and DVD recorder. This, however, functions only if you have connected your TV set to the DVD recorder using a scart cable (socket **EXT 1 TO TV-I/O**) and your TV set reacts to the switching.
T/C	**Title/Chapter**: Choose the 'T'(Title)/'C'(Chapter) directly from the menu bar If 'INFO' appears in the display, the index menu from a recorded disc or an introductory film will be shown. In this case, this function is not available.
PLAY MODE	**Playback type**: Choose between repeat, shuffle play and intro-scan
REC. MODE	**Record type (quality)**: To select the maximum possible record time
0..9	**Number buttons**: 0 - 9
DISC-MENU	**Disc menu**: To show the DVD menu or the index screen
SYSTEM-MENU	**System menu**: Call up/cancel the main menu (menu bar at the top of the screen)
SELECT	**Select**: Select function/value
OK	**Store/confirm**: To store or confirm entry
◀ ▶ ▲ ▼	**Cursor keys**: Left, right, up, down
RETURN	**Back**: Return to previous menu on a video CD (VCD). This function works also on some DVD's.
CLEAR	**Delete**: To delete last entry or clear programmed recording (TIMER)
CHANNEL +	**Plus**: Next programme number
CHANNEL –	**Minus**: Previous programme number
PLAY/PAUSE ▶II	**Playback/pause**: Play back a disc. If this button is pressed during playback, the DVD recorder switches to pause. You will see a still picture. If this button is pressed during recording, the DVD recorder will also switch to pause.

I◀◀	**Select previous title/search backwards**: Briefly press the button during playback: Previous chapter/film or previous title Hold down the button: Search backwards Hold down the button during the still picture: slow motion backwards
▶▶I	**Select next title/search forwards**: Briefly press the button during playback: Next chapter/film or next title Hold down the button: Search forwards Hold down the button during the still picture: slow motion forward
STOP ■	**Stop**: Stop playback / recording, except with programmed recordings (TIMER) Hold down the button to open and close the disc tray.
REC/OTR ●	**Record**: Record the current TV channel
EDIT	**EDIT**: For displaying the edit menu for DVD+(RW) discs, for setting chapter markers
TIMER	**TIMER**: To program a recording with ShowView® / without ShowView® or to alter/clear programmed recordings

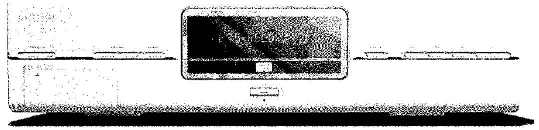
Additional TV functions

TV VOLUME +	**TV volume**: Increase TV volume
TV VOLUME –	**TV volume**: Reduce TV volume

For the following functions you need to hold down the button **DVD/TV** at the side and then select the function you need with the appropriate button.

0..9	**Number buttons**: 0 - 9
CHANNEL +	**TV programme number**: To select a higher programme number
CHANNEL –	**TV programme number**: To select a lower programme number

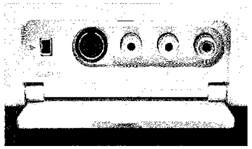
Front of the device



STANDBY/ON	**Switch on or off**: To switch off or on, interrupt a function, interrupt a programmed recording (TIMER)
CHANNEL –	**Select**: Lower programme number
CHANNEL +	**Select**: Higher programme number
REC MODE	**Record type (quality)**: To select the maximum possible record time

RECORD	**Record**: Record the current TV channel
RECORD LED	**Recording in progress**: Red light on the **RECORD** button to indicate recording in progress
OPEN/CLOSE	**Open/close disc tray**: Open/close disc tray
⏮	Select previous title/search backwards
⏭	Select next title/search forwards
■STOP	**Stop**: Interrupt playback/recording
▶ PLAY/PAUSE	**Playback/pause**: Play back recorded disc, interrupt playback, still picture

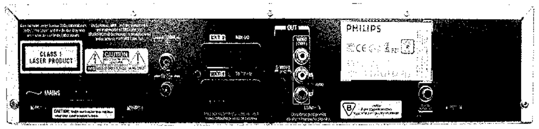
Behind the flap at the left-hand corner on the front



DV	**i-Link / DV socket (digital video input, IEEE 1394, FireWire)**: Connecting a digital camcorder or other suitable device (programme number 'CAM2').
S-VIDEO	**S-Video socket**: Connection of SVHS/Hi8 camcorders or SVHS/Hi8 video recorders (programme number 'CAM1')
Yellow socket VIDEO	**Video input socket**: Connection of camcorders or video recorders (programme number 'CAM1')
White/red socket left AUDIO right	**Audio input socket left/right**: Connection of camcorders or video recorders (programme number 'CAM1')

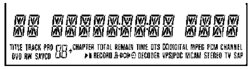
Switching between sockets **IN S-VIDEO (Y/C)** and **IN VIDEO (CVBS)** is done automatically. In case both sockets are used, the signal received at socket **IN S-VIDEO (Y/C)** is treated with priority.

Back of the unit



∿MAINS	**Mains socket**: Connection to the mains supply (230V/50Hz)
ANTENNA	**Aerial input**: Connection of the aerial
TV	**Aerial output**: Connection of the TV set
EXT 2 AUX I/O	**Scart socket 2**: Connection of an additional device (satellite receiver, set-top box, video recorder, camcorder, etc.)
EXT 1 TO TV-I/O	**Scart socket 1**: Connection of a TV set. RGB- output
OUT S-VIDEO (Y/C)	**S-Video output**: Connection of an S-Video compatible TV set
OUT VIDEO (CVBS)	**Video output (yellow socket)**: Connection of a TV set with a video input (CVBS, Composite Video)
OUT L AUDIO R	**Analogue audio output (white/red socket)**: Connection of a TV set with audio input sockets or connection of an additional device
DIGITAL AUDIO OUT	**Digital audio output**: Connection of a digital audio device (amplifier/receiver)

The symbols on your DVD recorder display


TITLE TRACK PRO 88+ CHAPTER TOTAL REMAIN TIME DTS DDIGITAL MPEG PCM CHANNEL
DVD RW SAVCD ▶II RECORD ⌀ o((⏲ DECODER VPS/PDC NICAM STEREO TV SAP

These symbols can light up on your DVD recorder display:

TITLE	Displays the title number selected/played (DVD)
TRACK	Displays the track selected/played (VCD/CD)
DVD+RW	Displays the inserted DVD disc: DVD /DVD+R / DVD+RW. Disc types 'DVD-R/DVD-RW ' are shown as DVD.
S-VCD	Displays the CD-disc inserted: S VCD/VCD/CD
88+	Displays recording type (Quality)/Playback type'HQ, SP+, EP, EP+'.
CHAPTER	Displays the chapter selected/played
TOTAL TIME	Total playback time
REMAIN TIME	Time remaining
TIME	Time used
DTS	A DTS audio signal is available on the digital audio output
DD DIGITAL	A Dolby digital audio signal is available on the digital audio output
MPEG	An MPEG audio signal is available on the digital audio output
PCM	A PCM audio signal is available on the digital audio output
CHANNEL	Channel/programme number
▶	Playback in progress
II	Playback/record interrupted (Pause)
RECORD	Recording in progress
⌀	A satellite recording has been programmed.
o((	A remote control signal has been received
⏲	A recording (timer) has been programmed
DECODER	A decoder has been assigned to the current TV channel (programme)

VPS/PDC	Video programming system / programme delivery control: A VPS or PDC code will be transmitted for the selected TV program
NICAM	The DVD recorder has detected a Nicam audio signal.
STEREO	During playback a HiFi/2 channel tone was detected or a HiFi/2 channel tone was received
88:88	Multi-function display/Text line •) Clock •) Disc/title playing time •) OTR switch-off time •) Title name •) Display of programme number of TV channel/position/channel name/function. •) Display of informations, warnings.

ENGLISH

Messages in the DVD recorder display

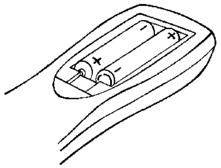
READING
TITLE TRACK PRO 88 CHAPTER TOTAL REMAIN TIME DTS DIGITAL MPEG PCM CHANNEL
DVD RW SAVCD RECORD DECODER VPS/PDC NICAM STEREO TV SAP

The following messages may appear in your DVD recorder display

TV ON	The DVD recorder is currently in the initial installation mode. Switch on your TV set and read section 'Installing your DVD recorder' in chapter 'Initial Installation'.
NO SIGNAL	No input signal available (signal inadequate or unstable)
MENU	The menu on the screen is active
OPENING	Disc tray opening
TRAY OPEN	Disc tray open
CLOSING	Disc tray closing
READING	Disc being read
MENU UPDT	Once recording has been successfully completed the table of contents is created.
INIT MENU	The menu structure is created after the first recording has been made on a new disc
COPY PROT	You have tried to copy a copy-protected DVD/video cassette.
WAIT	Please wait until this message disappears. The DVD recorder is busy performing a task.
NO DISC	No disc has been inserted for recording. If a disc has been inserted, perhaps it cannot be read.
INFO	Information on the inserted DVD is displayed on the screen
BUSY	The DVD recorder is processing the changes to make them DVD compatible
ERASING	The entire disc is erased
EMPTYDISC	The disc inserted is either new or has been completely erased (no recordings).
PROTECTED	The disc is protected against recording.
MAX TITLE	The maximum number of titles per disc has been reached. The maximum number of titles per disc is 48.
MAX CHAP	The maximum number of chapters per title/disc has been reached. The maximum number of chapters per title is 99, and 124 per disc.
DISC FULL	The disc is full. There is no space for new recordings
PAL DISC	A disc with PAL recordings has been inserted. The machine is trying to record an NTSC signal. Insert a new disc or one that contains NTSC recordings.
NTSC DISC	A disc with NTSC recordings has been inserted. The machine is trying to record a PAL signal. Insert a new disc or one that contains PAL recordings.
RECORDING	An illegal action (e.g. **OPEN/CLOSE** button) was attempted during recording.
FREETITLE	Playback was started for an empty title or the following title is empty
DISC LOCK	An attempt has been made to record during playback of a protected disc. This message appears if an attempt is made to insert a chapter marker (**EDIT** button).
DISC ERR	An error occurred when the title was being written. If this error keeps occurring, please clean the disc or use a new one. You will find information on how to clean the disc in the next chapter in the section 'Cleaning the discs'.
DISC WARN	An error occurred when writing the title. Recording was continued; the error was skipped
SETUP	After the automatic channel search, the menu for time/date settings appears on the screen.
WAIT 01	During the automatic channel search, the TV channels found will be count
BLOCKED	It is not possible to close/open the disc tray.
SAFE RECO	The new recording will be made at the end of all the other recordings (SAFE RECORD).
EASYLINK	The 'EasyLink' function is currently transferring information from the TV set.

2 Connecting the DVD recorder

Preparing the remote control for operation



The remote control and its batteries are packed separately in the original DVD recorder packaging. You must install the batteries in the remote control before use - described in the following section.

❶ Take the remote control of the DVD recorder and the enclosed batteries (2 batteries).

❷ Open the battery compartment, insert the batteries as shown and then close the battery compartment.

The remote control is now ready to use.
Its range is approximately 5 to 10 meters.

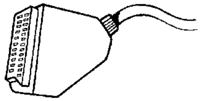
'Aim' correctly
In the following sections, you will need the remote control for the first time. Always point the front of the remote control at the DVD recorder and not at the TV set.

Tip

Connecting your DVD recorder to the TV set

The necessary cable connections must be made before you can record or playback TV programmes using your DVD recorder.

Connect the DVD recorder **directly** to your TV set. If there is a video recorder in between the picture quality may be poor because of the copy protection system built into the DVD recorder.
We recommend that you use a scart cable to connect your TV set and DVD recorder.



What is a scart cable?
The scart or Euro AV cable serves as the universal connector for picture, sound and control signals. With this type of connection, there is practically no loss of quality in picture or sound transmission.

?

When you install your DVD recorder for the first time, select one of the following options:

'Connecting with a scart cable and Easy Link'
If your TV set is equipped with 'Easy Link, Cinema Link, NexTView Link, Q-Link, Smart Link, Megalogic, Datalogic, ...' and you wish to use a scart cable.

What is Easy Link?
If your TV set is equipped with functions such as Easy Link, Cinema Link, NexTView Link, Q-Link, Smart Link, Megalogic or Datalogic, which are fully compatible with one another (TV set, DVD recorder, etc.), your DVD recorder can exchange information with your TV set. Please see your TV's operating instructions.

?

'Connecting with a scart cable without Easy Link'
If your TV set is not equipped with 'Easy Link, Cinema Link, NexTView Link, Q-Link, Smart Link,, Megalogic, Datalogic, ...' and you wish to use a scart cable.

'Connecting with an S-Video (Y/C) cable'
If your TV set is equipped with an S-Video (SVHS) socket.

What is an 'S-Video (Y/C) cable'?
This connecting cable, also known as the SVHS cable, is used to transmit the brightness signal (Y signal) and colour signal (C signal) separately. This mini DIN socket/plug is also called a Hosiden socket/plug.

?

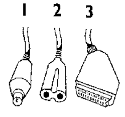
'Connecting with video (CVBS) cable'
If your TV set is equipped only with a video (CVBS) socket.

What is 'Video (CVBS)'?
This socket, usually referred to as the Cinch socket, is used for transmitting the composite video signal (FBAS, CVBS). In this method of transmission the colour signal and the brightness signal are transmitted on the same cable. In certain circumstances, this can lead to problems with the picture, such as 'Moiré' patterns.

?

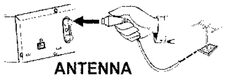
Connecting with a scart cable and 'Easy Link'

Your DVD recorder can exchange information with your TV set using 'Easy Link'. Your TV channels can also be transferred in the same order from your TV set to your DVD recorder using 'Easy Link'.

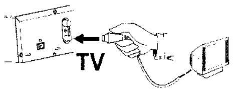


Have the following cables ready:
an aerial cable (1, supplied), a mains cable (2, supplied), a special scart cable (3, suitable for Easylink).

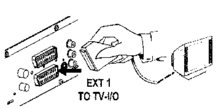
❶ Switch off your TV set.



❷ Remove the aerial cable plug from your TV set. Insert it into the **ANTENNA** socket at the back of the DVD recorder.

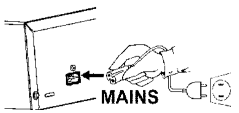


❸ Insert one end of the supplied aerial cable into the **TV** socket at the back of the DVD recorder and the other end into the aerial input socket at the back of the TV set.

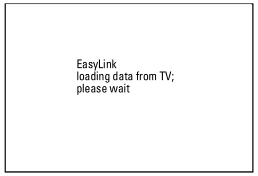


❹ Plug a special scart cable (for Easylink) into the scart socket **EXT 1 TO TV-I/O** at the back of the DVD recorder and the corresponding scart socket at the back of the TV set (see TV set operating instructions).

❺ Switch on the TV set.



❻ Insert one end of the supplied mains cable into the mains socket **~MAINS** at the back of the DVD recorder and the other end into the wall socket.



EasyLink
loading data from TV;
please wait

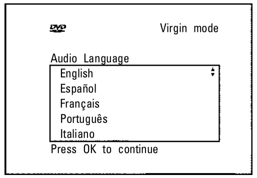
❼ A message appears on the screen announcing that the transfer has started. 'EASYLINK' appears on the display during transfer.
The TV set transfers all stored TV channels, in the same order, to the DVD recorder.
This may take several minutes.

×'*Time*', '*Year*', '*Month*', '*Date*' appears on my TV screen for confirmation

Normally, the date and time are transferred from the data of the TV channel that is stored under programme P01. If the aerial signal is too weak or disrupted, you must manually set the time and date:

❶ Check if the time in line '***Time***' is correct.
❷ If required, change the time with the number buttons **0..9** on your remote control.
❸ Select the next line with ▲ or ▼ .
❹ Check the displayed settings for: '***Year***', '***Month***' and '***Date***'.
❺ When all information is correct, save by pressing **OK** .

Problem



Virgin mode

Audio Language
English
Español
Français
Português
Italiano
Press OK to continue

×I can see more installation menus on my TV set

Not all the necessary data has been transferred. Please enter the settings by hand as follows. For more information on the various functions see 'Initial installation' in 'Installing your DVD recorder'.

❶ Select the desired audio language using ▼ or ▲ and confirm with **OK** .
❷ Select the desired subtitle language with ▼ or ▲ and confirm with **OK** .
❸ Select the desired picture format using ▼ or ▲ .

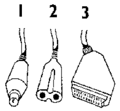
'***4:3 letterbox***'	For a 4:3 TV set; cinema format (black bars above and below the picture)
'***4:3 panscan***'	For a 4:3 TV set; full height format with the sides cut off
'***16:9***'	For a 16:9 TV set

❹ Confirm with **OK** .
❺ Select your country with ▼ or ▲ .
If your country does not appear, select '***Other***'.
❻ Confirm with **OK** .

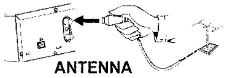
Problem

Initial installation is now complete.

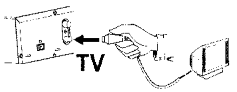
Connecting with a scart cable without 'Easy Link'



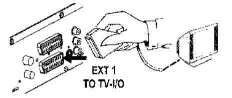
Have the following cables ready:
an aerial cable (1, supplied), a mains cable (2, supplied), a scart cable (3).



❶ Remove the aerial cable plug from your TV set. Insert it into the **ANTENNA** socket at the back of the DVD recorder.



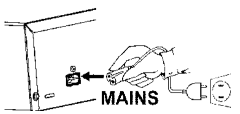
❷ Insert one end of the supplied aerial cable into the **TV** socket at the back of the DVD recorder and the other end into the aerial input socket at the back of the TV set.



❸ Plug a scart cable into the scart socket **EXT 1 TO TV-I/O** at the back of the DVD recorder and the scart socket for the DVD recorder at the back of the TV set (see TV set operating instructions).

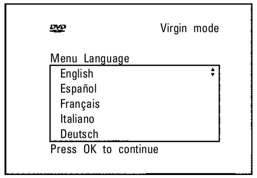
My TV set has several scart sockets. Which one should I use?
Select the scart socket that is suitable for both video output and for video input.
My TV set shows me a selection menu for the scart socket
Select 'VCR' as the source for this scart socket.

❹ Switch on the TV set.



❺ Insert one end of the supplied mains cable into the mains socket **∿MAINS** at the back of the DVD recorder and the other end into the wall socket. 'TV ON ' will appear on the display.

❻ If the connection was properly made and your TV was **automatically switched** to the programme number for the scart socket, e.g. 'EXT', '0', 'AV', you will see the following picture:



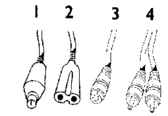
Virgin mode

Menu Language
English
Español
Français
Italiano
Deutsch
Press OK to continue

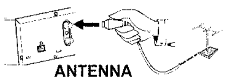
× My screen is empty.
- ✓ Many TV sets are switched by the DVD recorder to the programme number for the scart socket by way of a control signal sent through the scart cable.
- ✓ If the TV set does not automatically switch to the scart socket programme number, manually change to the corresponding programme number on your TV set (see your TV's operating instructions).
- ✓ Check that the scart cable is connected from the TV set to the **EXT 1 TO TV-I/O** socket on the DVD recorder. The **EXT 2 AUX I/O** socket is intended only for additional devices.

Then, read the paragraph on 'Initial installation' in 'Installing your DVD recorder'.

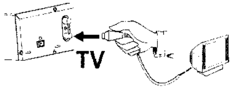
Connecting with an S-Video(Y/C)cable



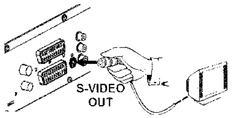
Have the following cables ready:
an aerial cable (1, supplied), a mains cable (2, supplied), an S-Video (SVHS) cable (3), an audio cable (4, supplied, red/white plug).



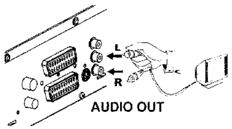
❶ Remove the aerial cable plug from your TV set. Insert it into the **ANTENNA** socket at the back of the DVD recorder.



❷ Insert one end of the supplied aerial cable into the **TV** socket at the back of the DVD recorder and the other end into the aerial input socket at the back of the TV set.

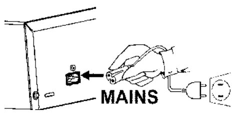


❸ Insert one end of a S-Video (SVHS) cable into the **OUT S-VIDEO (Y/C)** socket at the back of the DVD recorder and the other end into the S-Video (SVHS) input socket on the TV set (usually labelled 'S-Video in' or 'SVHS in'. See TV operating instructions).



❹ Insert one end of the supplied audio (Cinch) cable into the red/white Cinch socket **OUT L AUDIO R** at the back of the DVD recorder and the other end into the audio input socket (usually red/white) on the TV set (usually labelled 'Audio in' or 'AV in'. See TV operating instructions).

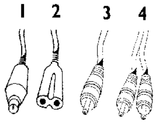
❺ Switch on the TV set. Switch the TV set over to this input socket or select the relevant channel number. Please see your TV's operating instructions for the channel number you need.



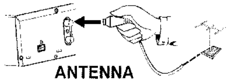
❻ Insert one end of the supplied mains cable into the mains socket **∿MAINS** at the back of the DVD recorder and the other end into the wall socket. 'TV ON ' will appear on the display.

Then, read the paragraph on 'Initial installation' in 'Installing your DVD recorder'.

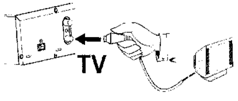
Connecting with video(CVBS) cable



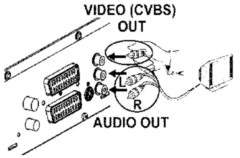
Have the following cables ready:
an aerial cable (1, supplied), a mains cable (2, supplied), a video (CVBS) cable (3, supplied, yellow plug), an audio cable (4, supplied, red/white plug).



❶ Remove the aerial cable plug from your TV set. Insert it into the **ANTENNA** socket at the back of the DVD recorder.



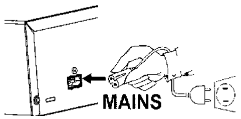
❷ Insert one end of the supplied aerial cable into the **TV** socket at the back of the DVD recorder and the other end into the aerial input socket at the back of the TV set.



❸ Insert one end of the supplied video (CVBS) cable into the yellow Cinch socket **OUT VIDEO (CVBS)** at the back of the DVD recorder and the other end into the video input socket (usually yellow) on the TV set (usually labelled 'Video in' or 'AV in'. See TV operating instructions).

❹ Insert one end of the supplied audio (Cinch) cable into the red/white Cinch socket **OUT L AUDIO R** at the back of the DVD recorder and the other end into the audio input socket (usually red/white) on the TV set (usually labelled 'Audio in' or 'AV in'. See TV operating instructions).

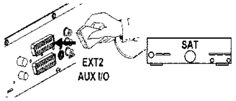
❺ Switch on the TV set. Switch the TV set over to the Video/Audio input socket or select the relevant programme number. Please see your TV's operating instructions for the programme number you need.



❻ Insert one end of the supplied mains cable into the mains socket **~MAINS** at the back of the DVD recorder and the other end into the wall socket. 'TV ON ' will appear on the display.

Then, read the paragraph on 'Initial installation' in 'Installing your DVD recorder'.

Connecting additional devices to the second scart socket



You can connect additional devices such as decoders, satellite receivers, camcorders, etc. to the **EXT 2 AUX I/O** socket. When playback is started on this additional device the DVD recorder automatically connects the **EXT 2 AUX I/O** scart socket with the **EXT 1 TO TV-I/O** scart socket. You will then see the picture from the additional device on your TV set, even if the DVD recorder is switched off.
The **TV/DVD** button on the remote control allows you to switch between playback through the **EXT 2 AUX I/O** scart socket and playback from the DVD recorder.

Connecting additional video recorders

You can connect a video recorder to the **EXT 2 AUX I/O** socket. If you have an SVHS video recorder you can additionally use the **OUT S-VIDEO (Y/C)** socket and the **OUT L AUDIO R** sockets.

Please note:
Most pre-recorded video cassettes and DVDs are copy-protected. If you try to copy them you will see the message 'COPY PROT' on the DVD recorder's display.

× When copying video cassettes the display on the DVD recorder shows 'NO SIGNAL'.
- ✓ Check that the scart cable is plugged in firmly.
- ✓ The DVD recorder may not be able to recognise the video input signal if this signal is poor or does not comply with relevant standards.

× When I copy DVD video discs or pre-recorded video cassettes the picture is fuzzy and the brightness varies
- ✓ This happens if you try to copy DVDs or video cassettes that have been copy-protected. Even though the picture on the TV is fine the recording on a DVD+R(W) is faulty. This interference is unavoidable with copy-protected DVDs or video cassettes.

Problem

Connect camcorder to the front sockets

To copy camcorder recordings, you can use the front sockets. These sockets are located behind the flap on the left hand side.

Best Picture Quality

If you have a DV or Digital 8 camcorder, connect the **DV** input of the DVD recorder to the appropriate DV output on the camcorder.

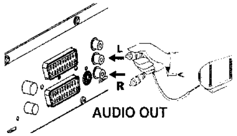
Very good Picture Quality

If you have a Hi8 or S-VHS(C) camcorder, connect the **S-VIDEO** input of the DVD recorder to the appropriate S-VHS output on the camcorder.
You must also connect the audio input **left AUDIO right** on the DVD recorder to the audio output on the camcorder.

Good Picture Quality

If you have a camcorder that only has a single video output (Composite Video, CVBS), connect the **VIDEO** input on the DVD recorder to the appropriate output on the camcorder.
You must also connect the audio input **left AUDIO right** on the DVD recorder to the audio output on the camcorder.

Connecting audio devices to the analogue audio sockets

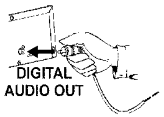


Two analogue audio sockets **OUT L AUDIO R** (audio signal output left/right) are located at the back of the DVD recorder.

These can be used to connect the following:
- **•) a receiver with Dolby-Pro-Logic**
- **•) a receiver with two-channel analogue stereo**

Can I use the 'Phono' input on my amplifier?
This socket (input) on the amplifier is designed only for record players without preamplifiers. Do **not** use this input for connecting the DVD recorder.
The DVD recorder or the amplifier may be damaged as a result.
?

Connecting audio devices to the digital audio socket



At the back of the DVD recorder there is a digital audio output socket **DIGITAL AUDIO OUT** for an coaxial cable.

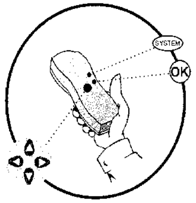
These can be used to connect the following:
- **•) an A/V receiver or an A/V amplifier with a digital multi-channel sound decoder**
- **•) a receiver with two-channel digital stereo (PCM)**

Digital multi-channel sound ?
Digital multi-channel sound offers the best possible sound quality. You will need a multi-channel A/V receiver or amplifier that supports at least one of the audio formats of the DVD recorder (MPEG2, Dolby Digital and DTS). Consult the operating instructions for your receiver to find out which audio formats it supports.
?

Problem

× All I can hear from my loudspeakers is a loud distorted noise
✓ The receiver is not compatible with the digital audio format of the DVD recorder. The audio format of the DVD disc is displayed in the status window when you switch to another language. Playback in six-channel digital surround sound is only possible if the receiver has a digital multi-channel sound decoder.

3 Installing your DVD recorder



Initial installation

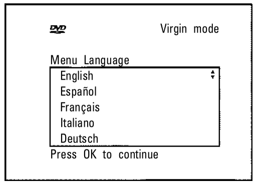
After successfully connecting your DVD recorder to the TV set and other additional devices as described in the previous chapter, this chapter will show you how to start the initial installation. The DVD recorder automatically seeks out and stores all available TV channels.

Aim correctly with the remote control
In the following sections, you will need the remote control for the first time. Aim the remote control at the DVD recorder and not at the TV set.

Connecting additional devices
If you have connected additional devices such as a satellite receiver to the aerial cable, switch them on. The automatic channel search will recognise it and save it.

No aerial connected
Even if you only want to use the DVD recorder to play back or have only connected a satellite receiver, you must still complete the initial installation. This is necessary so that the basic settings are stored correctly. Once initial installation is complete you can use the DVD recorder as normal.

Tip

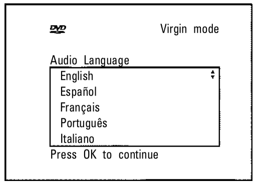

Virgin mode
Menu Language
English
Español
Français
Italiano
Deutsch
Press OK to continue

❶ Select the desired language for the on-screen menu by pressing ▼ or ▲ .

What is an on-screen menu?
The multi-language on-screen menu takes the mystery out of using your new DVD recorder. All settings and/or functions are displayed on your TV screen in the relevant language.

?

❷ Confirm with **OK** .

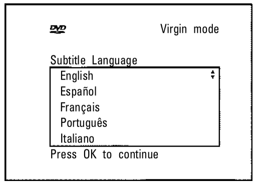

Virgin mode
Audio Language
English
Español
Français
Português
Italiano
Press OK to continue

❸ Select the desired audio language using ▼ or ▲ .

What is an audio language?
The DVD will play the sound in the language you select, provided this language is available on the disc. If it is not available on the disc the fist language on the DVD will be used instead. The DVD Video Disc menu, if available, will also be displayed in the language you select.

?

❹ Confirm with **OK** .

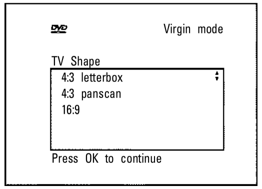

Virgin mode
Subtitle Language
English
Español
Français
Português
Italiano
Press OK to continue

❺ Select the desired language for the subtitles by pressing ▼ or ▲ .

What is the subtitle language?
The subtitles will be displayed in the language you select, provided this language is available on the disc. If it is not available on the disc the fist language on the DVD will be used instead.

?

❻ Confirm with **OK** .


Virgin mode
TV Shape
4:3 letterbox
4:3 panscan
16:9
Press OK to continue

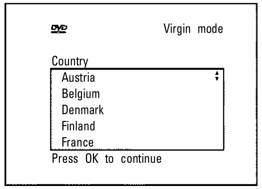
❼ Select the desired screen format position using ▼ or ▲ . These settings will only be used if you insert a DVD that contains this information.

Which screen formats can I select?

'*4:3 letterbox*'	for wide-screen (cinema format) with black borders at the top and bottom of the screen.
'*4:3 panscan*'	for a full-height picture with cropped edges.
'*16:9*'	for a wide-screen TV set (screen edge ratio 16:9)

?

❽ Confirm with **OK** .

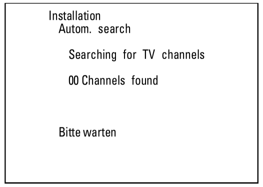

Virgin mode
Country
Austria
Belgium
Denmark
Finland
France
Press OK to continue

❾ Select your country with ▼ or ▲ .
If your country does not appear, select '*Other*'.

Why do I have to set the country?
To call up the specific settings for the respective country, you must first install the country.

?

❿ Confirm with **OK** .

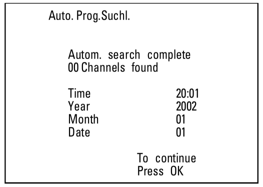

Installation
Autom. search
Searching for TV channels
00 Channels found
Bitte warten

⓫ After you connect the aerial (or cable TV, satellite receiver, etc.) to the DVD recorder, press **OK** .
The automatic TV channel search starts. 'WAIT' will appear on the display.

×The DVD recorder cannot find any TV stations
✓ Select channel 1 on the TV set. Can you see the stored TV channel on the TV set?
If not, check the cable connection from the aerial (aerial socket) to the DVD recorder and to the TV set.
✓ Please have patience.
The DVD recorder searches the entire frequency range in order to find and store the largest possible number of TV channels. It is possible that the TV channels in your country are broadcast in a higher frequency range. As soon as this range is reached during the search, the DVD recorder will find the TV channels.
✓ If no aerial is connected, complete the basic settings and then, if desired, start the automatic channel search (see section 'Automatic TV channel search').

Problem

⓬ When the automatic TV channel search is complete, '***Autom. search complete***' will appear on the TV screen.
'***Time***', '***Year***', '***Month***', '***Date***' will appear on the TV screen.



```
Auto. Prog.Suchl.

   Autom. search complete
   00 Channels found

   Time              20:01
   Year              2002
   Month             01
   Date              01

             To continue
             Press OK
```

⓭ Check if the time in '***Time***' is correct.

⓮ If required, change the time with the number buttons **0..9** on your remote control.

⓯ Select the next line with ▲ or ▼ .

⓰ Check if the displayed settings for: ***Year***, '***Month***' and '***Date***' are correct.

⓱ When all information is correct, save by pressing **OK** .

ENGLISH

The initial installation is now complete.

Satellite receiver

If you are connecting a satellite receiver, please read the section on 'Using a satellite receiver'.

Decoder

If you are connecting a decoder, you must install it as described in the next section.

Tip

× **Sound may be distorted on some TV channels.**

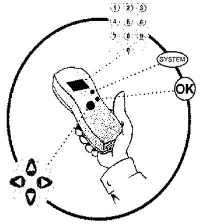
✓ If the sound is distorted on any of the stored TV channels or if there is no sound at all, the wrong TV system may have been stored for the TV channel. Read 'Manual TV channel search' for information on how to change the TV system.

Problem

Using a satellite receiver

TV channels from a satellite receiver (connected to scart socket **EXT 2 AUX I/O**) are received on the DVD recorder on programme number '***EXT2***'

If necessary, use the **MONITOR** button to switch to the internal tuner.
Then select programme number '***EXT1***' with **0** on the remote control and programme number '***EXT2***' with **CHANNEL −** .
You should select the TV channels to be received by the satellite receiver directly on the receiver itself.



Allocating a decoder

Some TV channels send coded TV signals that can only be viewed properly with a purchased or rented decoder. You can connect such a decoder (descrambler) to your DVD recorder. The following function automatically activates the connected decoder for the TV channel you want to watch.

How do I allocate the decoder for Easy Link?

If your TC=V set supports 'Easy Link' the decoder must be assigned to the relevant TV channel on the TV set (see the operating instructions for your TV set). Settings cannot then be made in this menu.

?

❶ Switch on the TV set. If required, select the programme number for the DVD recorder.

❷ Switch on the DVD recorder using **STANDBY/ON** .

❸ Use the **CHANNEL +** and **CHANNEL −** buttons on the DVD recorder or the number buttons **0..9** on the remote control to select the TV channel for which you want to use the decoder. If necessary, use the **MONITOR** button to switch to the internal tuner.

❹ Press the **SYSTEM-MENU** button on the remote control. The menu bar will appear at the top of the screen.

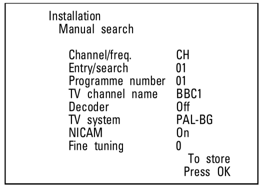
❺ Select 'Tλ' using ◀ or ▶ .

❻ Select line '***Installation***' using ▼ or ▲ and confirm with ▶ .

❼ Select line '***Manual search***' using ▼ or ▲ and confirm with ▶ .

❽ Select line '***Decoder***' using ▼ or ▲ .

❾ Select function '***On***' with ◀ or ▶ .



```
Installation
  Manual search

    Channel/freq.      CH
    Entry/search       01
    Programme number   01
    TV channel name    BBC1
    Decoder            Off
    TV system          PAL-BG
    NICAM              On
    Fine tuning        0
                         To store
                         Press OK
```

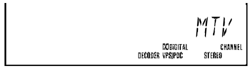
How can I switch the decoder off again?

Select '***Off***' (decoder off) on the TV screen in the line '***Decoder***' using ▶ .

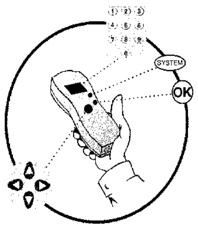
?

❿ Confirm with **OK** .

⓫ To end, press **SYSTEM-MENU** .



Your decoder has now been allocated to this TV channel.
When this TV channel is selected, the 'DECODER' symbol will appear in the DVD recorder display.



Manual TV channel search

In some cases, not all of the available TV channels may have been found and stored during initial installation. In this case, you will need to search for and store the missing or coded TV channels manually.

Manual search with EasyLink

With 'Easy Link', the DVD recorder will automatically download the TV channels stored on the TV set. This is why some lines have no function. To store new TV channels, they must first be stored on the TV set. The information will then be transferred to the DVD recorder automatically.

Tip

❶ Switch on the TV set. If required, select the programme number for the DVD recorder.

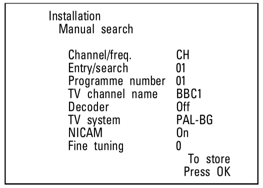
❷ Switch on the DVD recorder using **STANDBY/ON** .

❸ Press **SYSTEM-MENU** on the remote control. The menu bar appears.

❹ Select 'ꚍ' using ◀ or ▶ .

❺ Select '***Installation***' using ▼ or ▲ and confirm with ▶ .

❻ Select '***Manual search***' using ▼ or ▲ and confirm with ▶ .



```
Installation
  Manual search

    Channel/freq.       CH
    Entry/search        01
    Programme number    01
    TV channel name     BBC1
    Decoder             Off
    TV system           PAL-BG
    NICAM               On
    Fine tuning         0
                          To store
                          Press OK
```

❼ In '***Channel/freq.***', select the desired display using ▶

What is hidden behind the settings?

'***Freq.***': Display/entry of frequencies
'***CH***': Display/entry of channels
'***S-CH***': Display/entry of special channels

What is a special channel?

TV signals are transmitted in certain pre-defined frequency ranges. These ranges are divided into channels. A specific frequency/channel is assigned to each TV station. Certain frequency ranges are specified as special channels (hyperband channels).

?

❽ In '***Entry/search***', enter the frequency or channel of the TV station using the number buttons **0..9** .

× I don't know the channel for my TV station

✓ In this case, press ▶ to start the automatic search. A changing channel number/frequency number will appear on the TV screen.
Continue the automatic search until you have found the TV channel you are looking for.

Problem

❾ Using ◀ or ▶ in '***Programme number***', select the programme number you want to use for the TV channel, e.g. '***01***'.

How can I change the displayed symbol of a TV channel?

❶ In '***TV channel name***', press ▶ .
❷ Select the desired symbol position using ◀ or ▶ .
❸ Change the symbol at the symbol position with ▼ or ▲ .
❹ Select the next symbol position in the same way.
❺ Keep pressing ▶ until the cursor disappears.

Tip

How can I change the TV system of the TV channel?

In '***TV system***', use ◀ or ▶ to select the TV system that produces the least distortion of picture and sound.

What is NICAM?

NICAM is a digital sound transmission system. Using NICAM, you can transmit either 1 stereo channel or 2 separate mono channels. However, if reception is poor and the sound distorted you can turn off NICAM.
In '***NICAM***', select '***Off***' using ◀ or ▶ .

How can I improve the automatic process for storing channels?

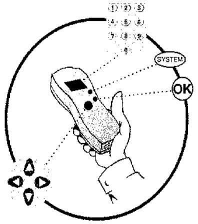
To change the automatic process for storing channels (fine tuning), select '***Fine tuning***'.
Using ◀ or ▶ you can try to fine-tune the TV channel manually.

Experts

❿ Press **OK** to store the TV channel.

⓫ To search for other TV channels, begin again at ❽ .

⓬ To end, press **SYSTEM-MENU** .



Sorting TV channels automatically (Follow TV)

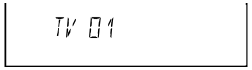
When the automatic channel search function is activated, the TV channels are stored in a specific order. This may differ from the order in which the TV channels appear on your TV set.
This function changes the order of the TV channels stored in your DVD recorder to match the order on the TV set.
This only works if the DVD recorder (**EXT 1 TO TV-I/O** socket) and the TV set **are connected with a scart cable**.

What does EASYLINK do?

If your TV set supports 'Easylink...', TV channels will be stored during initial installation in the same order as they appear on the TV set. To store the TV channels in a different order, you'll need to change the order on the TV set. When you start the Follow TV function the information is transferred again from the TV set.

?

❶ Switch on the TV set. If required, select the programme number for the DVD recorder.



❷ Switch on the DVD recorder using **STANDBY/ON** .

❸ Press the **SYSTEM-MENU** button on the remote control. The menu bar appears.

❹ Select 'ꝉᴧ' using ◄ or ► .

❺ Select '***Installation***' using ▼ or ▲ and confirm with ► .

❻ Select '***Follow TV***' using ▼ or ▲ and confirm with ► .

❼ Confirm the message on the screen with **OK** . 'TV 01' will appear in the DVD recorder display.

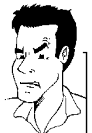
ENGLISH

❽ Select programme number '1' **on the TV set**.

× I cannot switch my TV set to programme number '1'
✓ If you have connected additional devices to the **EXT 2 AUX I/O** socket, please disconnect these devices. Other connected devices may have switched the TV set to the programme number of the scart socket.

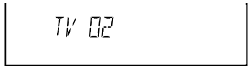
Problem

❾ Confirm with **OK** on the DVD recorder remote control.
'WAIT' will appear on the display. The DVD recorder compares the TV channels on the TV set and the DVD recorder.
If the DVD recorder finds the same TV channel as on the TV set it stores it at 'P01'.



×'NOTV' will appear in the display. The DVD recorder is not receiving a video signal from the TV set.
✓ Check the connectors at both ends of the scart cable.
✓ Check your TV's operating instructions to see which scart socket is used for video signals.
✓ If the problem persists, you won't be able to use this feature. Please read 'Sorting and clearing TV channels manually'.

Problem



❿ Wait until for example 'TV 02' appears in the display.

⓫ Select the next programme number **on the TV set**, e.g. '2'.

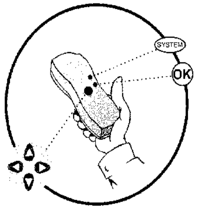
⓬ Confirm with **OK** on the DVD recorder remote control.

Deleting sorting
You can delete incorrect TV channel sorting by pressing ◄ .

Tip

⓭ Repeat steps ❿ to ⓬ until you have assigned all the TV channels.

⓮ To end, press **SYSTEM-MENU** .



Automatic TV channel search

During installation, all available TV channels are searched for and stored. If the channel assignments of your cable or satellite TV provider change or if you are reinstalling the DVD recorder, e.g. after moving house, you can start this procedure again. This will replace the stored TV channels with the new ones.

What does Easy Link do?
With Easylink, you can search for and store TV channels only on the TV set. These settings are accepted by the DVD recorder. Use this function to start the transfer of TV channels from the TV set.

?

❶ Switch on the TV set. If required, select the programme number for the DVD recorder.

❷ Switch on the DVD recorder using **STANDBY/ON** .

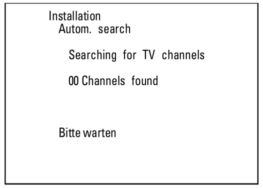
❸ Press **SYSTEM-MENU** on the remote control. The menu bar will appear at the top of the screen.

❹ Select 'ꝉᴧ' using ◄ or ► .

❺ Select line '***Installation***' using ▼ or ▲ and confirm with ► .

❻ Select line '***Autom. search***' using ▼ or ▲ .

❼ Press ► .



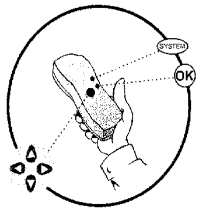
Installation
Autom. search
Searching for TV channels
00 Channels found
Bitte warten

❽ The automatic TV channel search starts. This allows the DVD recorder to save all available TV channels. This procedure may take several minutes.

❾ When the automatic search is completed, '***Autom. search complete***' will appear on the TV screen.

❿ To end, press **SYSTEM-MENU** .

You can read about how to search for a TV channel manually in section 'Adding and clearing TV channels manually'.



Sorting and clearing TV channels manually

After you have performed the automatic channel search you may not agree with the sequence in which the individual TV channels have been allocated to the programme positions (programme numbers). You can use this function to rearrange the TV channels already stored or to delete TV channels you don't want or those with poor reception.

The teletext clock resets automatically

If you store a TV channel which transmits TXT/PDC on programme number 'P01', the date and time will automatically be transmitted and constantly updated. As a result, the changes from summer time to winter time and back again will be made automatically.

Tip

What does Easy Link do?

With Easylink, TV channels can only be searched for and saved on the TV set. These settings are then accepted by the DVD recorder. That is why you cannot select this function manually.

?

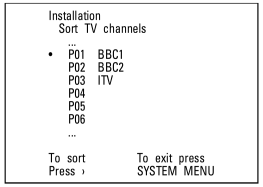
❶ Switch on the TV set. If required, select the programme number for the DVD recorder.

❷ Turn on the DVD recorder. Press the **SYSTEM-MENU** button on the remote control. The menu bar will appear at the top of the screen.

❸ Select 'T⅄' using ◀ or ▶ .

❹ Select line '***Installation***' using ▼ or ▲ and confirm with ▶ .

❺ Select line '***Sort TV channels***' using ▼ or ▲ and confirm with ▶ .



```
Installation
  Sort TV channels
  ...
•  P01  BBC1
   P02  BBC2
   P03  ITV
   P04
   P05
   P06
   ...
To sort        To exit press
Press ›        SYSTEM MENU
```

❻ Select the TV channel that you want to delete or whose order you want to change using ▼ or ▲ .

❼ Confirm with ▶ .

Deleting TV channels

Unwanted channels or those with poor reception can be deleted using **CLEAR**. After that you can continue at step ❻ .

Tip

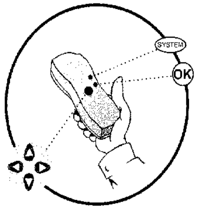
❽ Using ▼ or ▲ , shift the TV channel to the desired position and press the ◀ button. The DVD recorder will insert the TV channel.

❾ Repeat steps ❻ to ❽ until you have resorted/deleted all desired TV channels.

❿ To save, press **OK** .

⓫ To end, press **SYSTEM-MENU** .

Setting the language/country



You can select the country and the subtitle language as well as the audio language for DVD playback. Please observe that with some DVDs, you can change the audio language and/or subtitle language only via the DVD disc menu.
Moreover, you can set one of the displayed languages for the on-screen menu (OSD). However, the DVD recorder display will only display English text regardless of this setting.

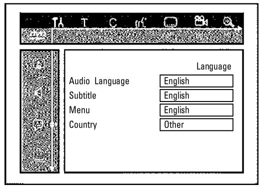
❶ Switch on the TV set. If required, select the programme number for the DVD recorder.

❷ Switch on the DVD recorder using **STANDBY/ON** .

❸ Press **SYSTEM-MENU** on the remote control. The menu bar appears.

❹ Select the 'T⅄' icon using ◀ or ▶ .

❺ Select '***Language***' using ▼ or ▲ and confirm with ▶ .



```
                     Language
Audio Language       English
Subtitle             English
Menu                 English
Country              Other
```

❻ Select the appropriate line and confirm with ▶ .

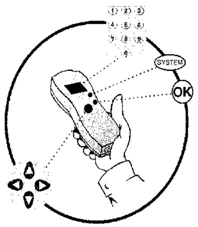
Which settings can I choose?

Audio Language: Playback language (audio language)
Subtitle: Subtitle language
Menu: Language of the OSD menu
Country: Location (country)

Tip

❼ Select the appropriate setting using ▼ or ▲ and confirm with **OK** .

❽ To end, press **SYSTEM-MENU** .



Setting the time and date

If the display shows an incorrect time or '--:--', the time and date must be reset manually.
If a TV channel which transmits TXT/PDC (teletext/PDC) is stored under programme number 'P01', the time and date will automatically be taken from the TXT/PDC information.

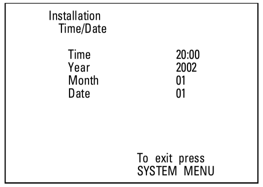
ENGLISH

❶ Press **SYSTEM-MENU** on the remote control. The menu bar appears.

❷ Select the 'Ƭ⅄' icon using ◀ or ▶ .

❸ Select '***Installation***' using ▼ or ▲ and confirm with ▶ .

❹ Select '***Time/Date***' using ▼ or ▲ and confirm with ▶ .



```
Installation
  Time/Date

    Time          20:00
    Year          2002
    Month         01
    Date          01


                  To exit press
                  SYSTEM MENU
```

❺ Check if the time in '***Time***' is correct. If required, change the time with the number buttons **0..9** on your remote control.

❻ Check '***Year***', '***Month***' and '***Date***' in the same way. To move between the fields, use ▼ or ▲ .

❼ Check the displayed settings and confirm with **OK** .
'***Stored***' will appear briefly on the screen.

❽ To end, press **SYSTEM-MENU** .

4 Information on the TV screen

You can check and change many of the features and settings on your DVD recorder using the system menu. The menu bar cannot be displayed during recording.

Icons in the menu bar

Use the **SYSTEM-MENU** button to call up and close the menu bar (main menu). You can select the appropriate feature using ◀ and ▶ . You confirm a feature using ▼ . This takes you to a submenu or executes the feature immediately.
Depending on the current disc, some features may not be available.

Menu bar 1

Ƭ⅄	**User preferences**
T	**Title/Track**
C	**Chapter/Index**
((ℓ	**Audio language**
▭	**Subtitle language**
🎥	**Camera angle**
🔍	**Zoom**

Menu bar 2

To display menu bar 2, press ▶ while menu bar 1 is displayed.

🔊	**Sound**
◂▯▸	**Frame-by-frame playback**
▷	**Slow motion**
▶▶	**Fast motion**
🕘	**Search by time**

Temporary feedback icons

Temporary feedback icons appear in the top left hand corner of the menu bar with information on the different operating modes. This information appears briefly when certain disc features are activated :

shuffle	**Shuffle**: Shuffle play
scan	**Scan**
repeat	**Repeat entire disc**
title	**Repeat title**
track	**Repeat track**
chapter	**Repeat chapter**
A-	**Repeat from A to end**
A-B	**Repeat from A to B**
	Camera angle
locked	**Child lock active**
resume	**Auto resume**
✕	**Action not allowed**

Status box

The status box displays the current operating mode (status) of the DVD recorder and the current disc type. This display can be switched off.

Disc type icons

RW	**DVD+RW**
DVD+R	**DVD+R**
DVD	**DVD video**
VCD	**Video CD**
no disc	**No disc**
error	**Error**

Operating mode icons

● rec	**Record**
■ stop	**Stop**
▶ play	**Play**
❚❚ pause	**Pause play**
●❚❚ pause	**Record pause**
▶▶ 8x	**Search forwards (8x speed)**
◀◀ 8x	**Search backwards (8x speed)**
▷ slow	**Slow motion**

Tuner info box

This box appears in the lower left-hand corner of the screen. The aerial signal, the TV channel and name of the TV channel are shown.

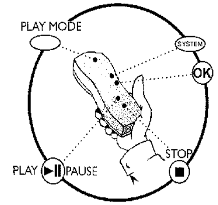
Y	**Current channel/selected input socket**
Y×	**No signal** TV channel is not available/additional device is not connected or is switched off
Y🔒	**Copy-protected signal**

Timer information box

This box appears above the tuner information box. When a timer recording is set, it shows the timer icon and the start time or date of the first programme to be recorded.
If no timer recording is scheduled, the current time is displayed.
This box disappears during playback of a disc or after a recording starts.

◷!	**Timer starts on the day shown**
◷⇥	**OTR recording runs until the stop time displayed**
◷	**Current time** No timer event programmed

5 Playback



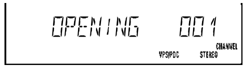
Playback hints

This DVD recorder will play the following systems:
- DVD video
- (Super)Video-CD disc
- DVD+RW disc
- DVD+R Disc
- DVD-RW (videomode, finalised)
- DVD-R
- CD-R
- CD-RW
- Audio CD
- MP3-CD

You can operate the DVD recorder using the remote control or the buttons on the front of the DVD recorder.

ENGLISH

Inserting a disc



❶ Press the **OPEN/CLOSE** button on the front. The disc tray opens. The dialog box shows 'OPENING' and then 'TRAY OPEN'.

❷ Insert the disc carefully into the tray, with the label uppermost and press **PLAY/PAUSE ▶II** or **OPEN/CLOSE**. The dialog box shows 'CLOSING' and then 'READING'. The information on the disc is read.

How do I insert a double-sided DVD?
Double-sided discs are not printed on either side. The labelling is in the centre on each side of the disc. The labelling of the side you wish to play must be uppermost.

Opening/closing the tray using the remote control
You can open and close the disc tray using the remote control.
Press and hold the **STOP ■** button on the remote control until the dialog box shows 'OPENING' or 'CLOSING'.

Tip

❸ Playback begins automatically.

A menu may appear during playback of a DVD. In case titles and chapters are numbered, press a number button on the remote control. You can also select a menu item using ◀, ▶, ▲, ▼ and confirm with **OK**.
For further information, read chapter 'Playing a DVD video disc'.

During the playback of a DVD+RW, the index screen overview appears. Choose the title you want to play back using ▼, ▲, I◀◀, ▶▶I.
Confirm with **OK**.
For further information, read chapter 'Playing a DVD+RW/+R disc'.

If the playback does not start automatically, press **PLAY/PAUSE ▶II**.
For further information, read chapter 'Playing an audio CD'.

If the '■' symbol appears in the display, start playback by pressing **PLAY/PAUSE ▶II**. If a menu appears on the screen, use the remote control buttons indicated on the screen to select the menu option you want (PREV= I◀◀, NEXT= ▶▶I) or with the number buttons **0..9**.
For further information see ' Playing a (Super) Video CD'.

Playing a DVD video disc

×'PIN' will appear on the display
✓ The child lock was activated for the inserted disc. Read section 'Access control' and 'Authorising a disc' and in chapter 'Access control (child lock)'.

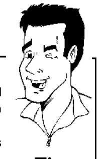
×The menu on the screen is showing an 'X'
✓ Some DVD discs can be manufactured so that certain steps are required before the disc can be played, or so that only limited operation is possible during playback. When an 'X' appears on the screen the selected feature is not possible.

×The screen is showing regional code information
✓ Since DVD films are not normally released in all parts of the world at the same time, all DVD players have a specific regional code. Discs can be given a regional code. If the regional codes differ between the player and the disc, playback is not possible.
✓ The regional code is shown on the label on the back of the machine.
✓ The regional code does not apply to recordable DVD discs.

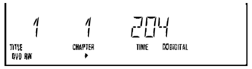
×The screen is prompting me to choose an option from the menu.
✓ Select the option you want using ▲, ▼, ◀, ▶ or the number keys **0..9**.
In some cases you need to confirm with **OK**.
You can also access the menu using **DISC-MENU** on the remote control.

Problem

How can I access hidden information?
❶ Press the **DISC-MENU** button on the remote control. A menu will appear on the screen. For some feature films this may appear after an introductory sequence.
❷ Select the option you want using ▲, ▼, ◀, ▶ or the number keys **0..9**.
Confirm with **OK**.



Tip



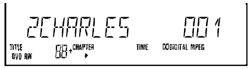
❶ If playback does not start automatically, press **PLAY/PAUSE ►II** .
The display shows:
title, chapter, time elapsed.

❷ To stop the disc, press **STOP ■** on the remote control or **■STOP** on the DVD recorder.

❸ To eject the disc, press **OPEN/CLOSE** on the front of the DVD recorder.

Playing a DVD+RW/+R disc

❶ If the disc is write-protected or a finalised DVD+R disc, playback starts automatically.



❷ If playback does not start automatically, select the title you want to watch from the Index Picture Screen using ▼ or ▲ .
You can also use the I◄◄ or ►►I buttons on the front of the set.

❸ Press **PLAY/PAUSE ►II** .
The display shows:
title number, recording quality.

×I see the message 'EMPTYDISC' in the display
✓ There are no recordings on this disc.

Problem

❹ To stop the disc, press **STOP ■** on the remote control or **■STOP** on the DVD recorder.

❺ To eject the disc, press **OPEN/CLOSE** on the front of the DVD recorder.

What should I note when playing back different recording types (qualities)?
The correct recording quality '***HQ***(HQ), ***SP+***(SP+), ***EP***(EP), ***EP+***(EP+)' will automatically be selected during playback.
For more information, please read section 'Selecting the recording type (Quality)' in chapter 'Manual recording'.

?

Playing an audio CD

You can use your DVD recorder to play audio CDs

❶ Insert an audio CD. Playback starts automatically.

Audio CD display'
If the TV is on, the audio CD screen appears automatically
During play, the current track number and its elapsed playing time will show on the TV screen and on the recorder display.

Tip

❷ Stop playback using **STOP ■** . The number of tracks and the total time are displayed.

Playing an MP3 CD

MP3 (MPEG1 Audio Layer-3) files are highly compressed music files. Using this technology the data volume can be compressed by a factor of 10. This means it is possible to record 10 hours of music in CD quality on a single CD-ROM.

When creating MP3 CDs please note the following:
Supported file system: ISO9660, Joliet
Supported formats: *.mp3
File names: maximum 64 ASCII characters (Joliet)
Maximum of 99 albums, 999 tracks
Supported sampling frequencies: 44.1kHz, 48kHz. Files with lesser than 44.1kHZ will be skipped.
Supported bit rate: 32, 64, 96, 128, 192, 256 (kbps)
ID3 Tag: Version 1, 1.1. If the version is higher, the directory name is used for the album and the filename for the track.

Important notes for playback:
In agreement with SDMI the digital audio output will not work during MP3 playback.
Only the first session of a multi-session CD will play back.

❶ Insert an MP3 CD. Playback starts automatically.

MP3 CD display
If the TV is on, the MP3 CD screen appears automatically
During playback, the current track number and its elapsed playing time will show on the TV screen and on the recorder display.
During interrupted playback (**STOP ■**), the current track number will show on the TV screen and on the recorder display.
If available in the so-called ID tag, more information will be displayed on: album, track, and artist.

Tip

❷ Stop playback using **STOP ■** . The number of albums will be shown in the display.

Tip

Additional playback features

Select the previous or next title with I◀◀ or ▶▶I .

Choose the previous or the next album using ▲ or ▼ .
Choose the previous or next title with ◀ or ▶ .
You can also use the number buttons **0..9** on the remote control to enter the number of the album/track.

You can also use **T/C** to select titles and albums.

1. Press **T/C** and then select symbol 'T' for album or 'C' for title with ▶ or ◀ .
2. Select the number of the album/title with ▼ , ▲ or with the number buttons **0..9** on the remote control.

You can also use repeat functions (Button **PLAY MODE**).

Playing a (Super) Video CD

(Super) Video CDs may be equipped with PBC (Play Back Control). This means that special playback functions (menus) can be directly selected. The Video CD must be PBC-compatible (see CD packaging).
'PBC' is turned on by default.

1. Insert a (Super) Video CD and press **PLAY/PAUSE ▶II** .
   If the '■' symbol appears in the display, start playback by pressing **PLAY/PAUSE ▶II** .
2. If a menu appears on the screen, use the remote control buttons indicated on the screen to select the menu option you want (PREV= I◀◀ , NEXT= ▶▶I) or with the number buttons **0..9** .
   If the PBC menu contains a title list, the desired title can be chosen directly.
3. The **RETURN** button will take you back to the previous menu.
4. Stop playback using **STOP ■** .

6 Additional playback features

Changing to another title/chapter

If there is more than one title or chapter on the disc, follow the instructions to change to another title or chapter. If there are several chapters within the title, these will be shown. It is possible to select these titles using the menu bar.

1. During playback use the ▶▶I button to move to the next title/chapter. Pressing I◀◀ takes you to the start of the current title or chapter. Pressing I◀◀ twice takes you to the start of the previous title or chapter.

Tip

Using T/C (title/chapter)

1. Press **T/C** (title/chapter) and select the appropriate title using ▲ or ▼ .
   Ensure that the 'T'(Title) icon is selected in the menu bar.
2. Using **T/C** you can select chapters within the title. Press **T/C** and select the 'C' (Chapter) icon using ▶ .
   Select the appropriate chapter using ▲ or ▼ .

Searching a disc

You can search the disc for a recording at 4x or 32x playback speed. Additional playback speeds are available via menu bar (▶▶).

1. During playback, press and hold I◀◀ (reverse) or ▶▶I (forwards) to switch to the search feature. You can switch between the playback speeds using I◀◀ / ▶▶I .
2. To continue playback press **PLAY/PAUSE ▶II** twice at your chosen location.

Problem

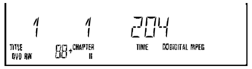
× No sound

✓ The sound is switched off in search mode. This is not a fault in your machine.

Tip

Search function via menu bar

1. During playback press **SYSTEM-MENU** on the remote control. The menu bar will appear at the top of the screen.
2. Select the '▶▶' icon using ▶ or ◀ and confirm with ▼ .
3. Using ◀ or ▶ you can now select different speeds forwards or backwards.
4. If necessary hide the menu bar using **SYSTEM-MENU** .
5. To continue playback, press **PLAY/PAUSE ▶II** .



Still picture

❶ During playback, press **PLAY/PAUSE ►II** to stop the disc and display a still picture.

Frame-by-frame playback via menu bar

❶ During the still picture press **SYSTEM-MENU** on the remote control. The menu bar will appear at the top of the screen.
❷ Select the '◂▯▸' icon using ▶ or ◀ and confirm with ▼ button.
❸ Using ◀ or ▶ you can now scroll back or forwards one frame at a time.
❹ If necessary hide the menu bar using **SYSTEM-MENU**.
❺ To continue playback, press **PLAY/PAUSE ►II** .

Tip

Slow motion

❶ During playback, press **PLAY/PAUSE ►II** on the remote control. Then hold down **I◀◀** or **▶▶I** to switch to slow motion.

❷ You can choose between the various speeds using **I◀◀** or **▶▶I** .

Slow motion over the menu bar

❶ During playback, press **PLAY/PAUSE ►II** on the remote control and then press **SYSTEM-MENU** The menu bar will appear at the top of the screen.
❷ Select the '▷' symbol using ▶ or ◀ and confirm with ▼ .
❸ Using ◀ or ▶ you can now select various slow motion speeds backwards or forwards.
❹ If necessary hide the menu bar using **SYSTEM-MENU**.

Tip

❸ To continue playback, press **PLAY/PAUSE ►II** twice.

Search by time

Using this feature you can select where playback should start (select elapsed time).

❶ During playback press **SYSTEM-MENU** on the remote control. The menu bar will appear at the top of the screen.

❷ Select the '⌚' symbol using ▶ or ◀ and confirm with ▼ . Playback is stopped and a box appears on the screen showing the elapsed time.

❸ Enter the start time with the digit keys **0..9** from where playback should start.

❹ Confirm with **OK** .

× **The time entered will flash**
✓ The selected title is shorter than the time entered. Enter a new time or end the function using **SYSTEM-MENU** .

Problem

❺ Playback starts before the time entered.

Repeat/Shuffle play

You can mark entire sections or the whole disc for endless playback. Depending on the type of disc (DVD video, DVD+RW, video CD) you can select a chapter, title or the entire disc.

❶ Select the desired chapter, title or the entire disc and start playback.

❷ During playback, press **PLAY MODE**. By pressing **PLAY MODE** again you can chose from the following options:
•) 'chapter': repeat chapter – DVD only
•) 'title': repeat title/track
•) 'repeat': repeat entire disc (Video CD, Audio CD only)
•) 'shuffle': Shuffle play
•) display disappears: no repeat

❸ To switch off the repeat, press **STOP ■** .
You can also press **PLAY MODE** repeatedly until the icons disappear.

Repeat sequence (A-B)

You can repeat a certain sequence within a title/chapter. You have to mark the start and end of the desired sequence.

❶ During playback press at the start of the sequence **PLAY/PAUSE ►II** .
You see a still picture.

❷ Press **PLAY MODE** until the 'A-' icon appears on the screen. This marks the start point.
Press **PLAY/PAUSE ►II** to start playback.

❸ At the desired end point, press **OK** . 'A-B' appears on the TV screen. The disc will only play between the selected points.

❹ To switch off the repeat, press **STOP ■** .
You can also press **PLAY MODE** repeatedly until the icons disappear.

Scan feature

This feature plays back the first 10 seconds of each chapter (DVD) or track (CD).

❶ During playback, press **PLAY MODE** . Select 'scan' using **PLAY MODE** .

❷ After 10 seconds the DVD recorder switches to the next chapter/index. To start playback at the corresponding chapter/index, press **STOP ■** and then **PLAY/PAUSE ►II** .

Zoom feature

The Zoom feature allows you to enlarge the video image and pan through the enlarged image.

❶ During playback, press **PLAY/PAUSE ►II** . The DVD recorder switches to 'PAUSE'. You will see a still picture.

❷ Press **SYSTEM-MENU** and select the '🔍' icon using ▶ .

❸ Select the required zoom factor using ▼ or ▲ .

❹ When '***press OK to pan***' appears on the screen, the zoom process is complete.

❺ Press **OK** . Using ▲ , ▼ , ▶ , ◀ select the part of the image you wish to view.

❻ Confirm with **OK** .

❼ To stop the feature, press **PLAY/PAUSE ►II** and then **SYSTEM-MENU** .

Camera angle

If a DVD video contains sequences recorded from different camera angles you can change the camera angle for playback.

❶ During playback, press **PLAY/PAUSE ►II** . You will see a still picture.

❷ Press **SYSTEM-MENU** and select the '🎥' icon using ▶ .

Problem

× The '🎥' icon is not visible

✓ The selected scene was not recorded from different camera angles. That is why you cannot select this feature. For more information please read the 'cover text' on your DVD video disc.

❸ Select the required camera angle using ▼ or ▲ . You can also enter the number directly using the number buttons **0..9** .

❹ After a short delay, playback changes to the new camera angle. The '🎥' icon remains displayed until multiple angles are no longer available.

Changing the audio language

Pre-recorded DVD videos often come with multiple audio languages. Playback uses the language you selected during initial installation. You can change the audio language of the current disc at any time.
You can change the audio language either using the menu of the inserted disc (**DISC-MENU** button) or the menu bar (**SYSTEM-MENU** button). The audio languages for DVD playback in the two menus may be different.

❶ During playback press **SYSTEM-MENU** and select the '🗨' icon using ▶ .

❷ Select the required audio language using ▼ or ▲ . You can also enter the number directly using the number buttons **0..9** .

❸ Play continues in the new audio language.

Subtitles

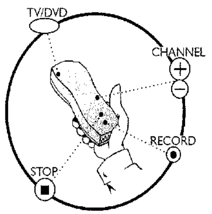
Pre-recorded DVD videos often come with subtitles in several languages. Playback uses the language you selected during initial installation. You can change the subtitle language of the current disc at any time.
You can change the subtitle language either using the menu of the inserted disc (**DISC-MENU** button) or the menu bar (**SYSTEM-MENU** button). The subtitle languages in the menus may differ.

❶ During playback press **SYSTEM-MENU** and select the '💬' icon using ▶ .

❷ Select the required subtitle language using ▼ or ▲ . You can also enter the number directly using the number buttons **0..9** .
You can switch off subtitles again with **0** or by pressing '***off***'.

❸ Playback continues in the new subtitle language.

7 Manual recording



General information

Which discs can I use for recording?
With this DVD recorder, you can record on two types of DVD:
DVD+RW
This disc can be written to and then the contents deleted.
DVD+R
This type of disc can only be recorded once.
If you want to play this DVD in a DVD player it must be finalized using the '***Finalise disc***' function. It is not possible to make further recordings using this disc.
If this disc is to be played in a DVD recorder it must not be finalised. Recordings can be added and deleted. The disc space (playback time) from the deleted recording cannot be recovered for further recordings

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ENGLISH

Use the 'Manual recording' feature to spontaneously start recording (e.g. to record a TV show already in progress).
In the 'Index Picture screen' select the title to be overwritten or '***Empty title***' using ▼ and ▲ .
If you want to record between existing recordings, check the length of the old recording and the length of the new recording. If the new recording is too long, the following recording (title/chapter) will be overwritten.

Insert new recordings at the end of all existing recordings (Safe Record)
To add a new recording at the end of the last recording on the disc, hold down the **REC/OTR ●** button until the message 'SAFE RECO' appears on the display.
For DVD+R discs each new recording is always added at the end of all previous recordings as existing recordings cannot be overwritten.

Tip

If you want to start and stop a recording manually, read **'Recording without automatic switch-off'**.

If you want to start a recording manually but stop it automatically, read **'Recording with automatic switch-off'**. (e.g. not to record to the end of the disc)

Read **'Automatic recording from a satellite receiver'**, if you want a recording to be controlled automatically by a satellite receiver.

Read **'Direct record'** if you want to record a programme currently being shown.

Recording without automatic switch-off

❶ Switch on the TV set. If required, select the programme number for the DVD recorder.

❷ Insert a disc to be used for the recording. The system and content of the disc will be checked. 'READING' will appear on the display.

× **Index display**
✓ A DVD+RW disc was inserted that already contains recordings. Use ▲ and ▼ to select a location where the recording should be started.

× **'EMPTYDISC' appears in the display**
✓ The inserted DVD disc is empty.

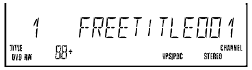
× **A dialog box appears asking if the contents should be erased or the disc should be ejected**
✓ The inserted disc is a DVD+RW disc whose contents are not compatible with DVD Video (e.g. a data disc). This disc cannot be used for recordings until the entire disc is erased using the **REC/OTR ●** button.

× **'*Too many titles*' appears on the screen when a recording is attempted**
✓ A disc can only contain a max. of 48 titles (including the empty titles). Erase the titles or change the disc.

Problem

❸ If necessary, switch to the internal tuner on the DVD recorder using the **MONITOR** button on the remote control.

❹ Select the programme number (station name) you wish to record using **CHANNEL +** or **CHANNEL −** . The following will appear on the display:

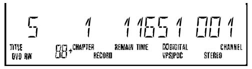


Station name
If a TV station transmits a station name it will be shown in the display.
Programme number of the external inputs:

'EXT1'	Scart socket at the back **EXT 1 TO TV-I/O**
'EXT2'	Scart socket at the back **EXT 2 AUX I/O**
'CAM1'	SVHS-/Audio front sockets **S-VIDEO / left AUDIO right**
'CAM1'	Video/audio front sockets A/V **VIDEO / left AUDIO right** Switching between sockets **S-VIDEO** and **VIDEO** is done automatically. In case both sockets are used, the signal received at socket **S-VIDEO** is treated with priority.
'CAM2'	Digital Video (i Link) front socket **DV**

Tip

❺ To start recording, press **REC/OTR ●** on the remote control or **RECORD** on the DVD recorder. If you want to start the recording at the end of the existing recordings, hold down the **REC/OTR ●** button until the message '*SAFE RECD*' appears on the display.
For DVD+R discs each new recording is always added at the end of all previous recordings as existing recordings cannot be overwritten.
On the display will appear e.g.:



Inserting chapter markers
During recording it is possible to mark scenes that you want to see or hide later.
During recording press **EDIT** at the relevant location. The screen displays '***Inserting marker***'. The 'CHAPTER' number is increased by one in the display box.
For more information on titles and chapters please see the section 'Changing to another title/chapter' in the chapter 'Playback'.

Tip

❻ You can stop recording by pressing **STOP ■** on the remote control or **■STOP** on the recorder. '*MENU UPDT*' will appear on the display. The DVD player is preparing the list of contents. Wait until this message disappears in the display, then the recording is completed.

× **The display will read '*DISC ERR*'**
✓ The recording could not be completed correctly because of a disc error. Check and, if necessary, clean the inserted disc.

Problem

Making recordings on DVD+R discs compatible
If you want to play back the recording on a DVD player, you need to finalise the disc in the DVD recorder. You can prepare your DVD for use in a DVD player using the '***Finalising***' feature. See the section 'Finalising DVD+R discs' in chapter 'Managing the disc contents'.

Tip

Interrupt recording (Pause)

❶ During recording press **PLAY/PAUSE ►II** , for example to avoid recording the commercials.

❷ To continue recording, press **REC/OTR ●** .

End recording
To end the recording, press the **STOP ■** button. Wait until '*MENU UPDT*' disappears from the display.

Tip

Recording with automatic switch-off (OTR – One Touch Recording)

❶ Insert a disc.

❷ Use **CHANNEL +** or **CHANNEL –** to select the programme number (channel name) you want to record.

❸ Press **REC/OTR ●** on the remote control.

❹ Each time you press **REC/OTR ●** you will add 30 minutes to the recording time.

How can I cancel the recording time I have just set?
To cancel the entry, press the **CLEAR** button while the recording time is displayed.

?

Protecting the disc against accidental recording

To prevent an important recording from being accidentally erased, you can protect the entire disc. You can only protect the disc as a whole. It is not possible to protect an individual recording.

What happens with DVD+R discs?
As long as these discs are not finalised, they can be protected against accidental erasure in the same way as DVD+RW discs.

?

❶ Insert the disc you wish to protect.

❷ Press **DISC-MENU** . The Index Picture Screen appears.

❸ While the Index Picture Screen is displayed, press the **STOP ■** button on the remote control. The first title is marked.

❹ Press **▲** . This takes you to the disc info screen.

❺ Press the **▶** button.
Select '***Protection***'.
Confirm with **▶** .

❻ Select '***Protected***' using **▼** and confirm with **OK** .

❼ Quit using **◀** and then **DISC-MENU** .

The entire disc is now protected. If you try to record onto this disc the message 'DISC LOCK' will appear in the display and '***Disc locked***' on the screen.

Lining up recordings within a title (assemble cut)

You can add further recordings to a title already contained on a DVD+RW disc. This recording will be added to the title as a so-called 'chapter'. Existing information will be overwritten from this location onward. Depending on the length of the recording, this will also overwrite titles that follow the current title. The recording mode (quality) is automatically transferred from the current title.
To play back this recording, press **SYSTEM-MENU** and select 'C' (chapter) using ▶ . You can also use **T/C** .

For more information, read section 'Changing to a different title/chapter' in chapter 'Playback'.

What happens with DVD+R discs?
New recordings on 'DVD+R' discs can only be added after existing recordings.
It is not possible to overwrite existing recordings on 'DVD+R' discs.

❶ Find the title in the Index Picture Screen where you want to insert the new recording.

❷ Look at the last minute of the old recording (playback)

❸ Press **PLAY/PAUSE ▶II** on the remote control at the position where the new recording is to go. '**II** ' will appear on the display.

❹ To monitor the recording you can switch to the internal tuner using **MONITOR** .

❺ Now start recording as usual by pressing **REC/OTR ●** on the remote control.
The new recording will be inserted.

❻ Stop recording with **STOP ■** .

Selecting the recording mode (quality)

By selecting a recording mode, you define the picture quality of recordings and the maximum recording time for a disc.
You can check the quality by switching to a recording mode and then watch the picture via the built-in tuner (**MONITOR** button).
For playback, the correct picture quality will automatically be selected.

❶ Switch on the TV set. If required, select the programme number for the DVD recorder.

❷ On the front of the DVD recorder select the recording quality using **REC MODE** .
You can also use the button **REC. MODE** on the remote control.

Which recording types can I choose?

'HQ/***HQ***': **H**igh**Q**uality offers the best picture quality and a recording time of 60 minutes.

'SP+/***SP+***': **S**tandard**P**lay (pre-recorded DVD quality) offers excellent picture quality with a recording time of 150 minutes.

'EP/***EP***': **E**xtended**P**lay (better than VHS quality). Recording time 240 minutes.

'EP+***EP+***': **6 hours (VHS picture quality). Recording time 360 minutes.**

Can I select the recording type via a menu as well?

❶ Press the **SYSTEM-MENU** button.
❷ Select '⚒' symbol with ◀ or ▶ .
❸ Select '***Record settings***' using ◀ or ▶ and confirm with ▶ .
❹ In the line '***Rec Mode***' select the recording type with ▼ or ▲ .
❺ Confirm using **OK** and **SYSTEM-MENU** .
❻ If you have selected the recording type 'EP/***EP***' or 'EP+/***EP+***', you can select the settings '***Stndrd***' (Standard) or '***Sport***' (fast movements) in the '***Filter mode***' line.

Tip

Automatic recording from a satellite receiver (Sat Recording)

You can use this feature if you own a satellite receiver that can control other devices via a scart cable and a programming feature (Timer). For more information, please see the operating instructions for the satellite receiver.

❶ Switch on the TV set. If required, select the programme number for the DVD recorder.

❷ Press **SYSTEM-MENU** on the remote control. The menu bar appears.

❸ Select '⚒' using ◀ or ▶ .

❹ Select line '***Record settings***' using ▼ or ▲ and confirm with ▶ .

❺ Select '***Sat record***' using ▼ or ▲ .

❻ Select '***EXT2***' with ◀ or ▶ .

Switching off 'Sat Recording'
To switch off the feature, select '***Off***' using ▶ or ◀ .

Tip

❼ Confirm with **OK** .

❽ Use a scart cable to connect the scart socket **EXT 2 AUX I/O** on the DVD recorder to the corresponding scart socket on the satellite receiver.

❾ Quit using **SYSTEM-MENU** .

❿ Insert a disc that you want to use for recording.

⓫ Programme the satellite receiver with the required information (programme number of the TV channel, start time, end time).
If necessary, please see the operating instructions for your satellite receiver.

⓬ Switch off the DVD recorder with **STANDBY** ⏻ . '⏲ ' appears in the display to show the activated feature.

The DVD recorder is now ready to record. The beginning and end of the recording is controlled via the scart socket **EXT 2 AUX I/O** .

'Direct Record'

Can I instantly record the TV channel I want, even though the DVD recorder is switched off? No problem. If recording is started manually, the DVD recorder, when it is **switched off** , is set to the current TV channel on the TV set using the scart cable.
You will find more information on how to switch 'Direct record' on or off in the next section 'Direct Record'.

How does Direct Record work?
The DVD recorder uses the scart cable to compare the TV channel selected on the TV set with its stored TV channels. If the same TV channel is found, the DVD recorder switches to the corresponding programme number and starts recording.
During this search please do not change the TV channel on the TV. This may affect the tuning of the DVD recorder.

?

❶ On the TV set, select the programme number you want make the recording from.

❷ Press **REC/OTR** ● with the DVD recorder **switched off**.

×'WAIT' will appear on the display.
✓ The DVD recorder is comparing its stored TV channels with those on the TV set. Please do not change the TV channel on the TV set while 'WAIT' is displayed.

×'NOTV' appears in the display
✓ This TV channel could not be found in the DVD recorder's memory. Check that all the TV channels stored on the TV set are available on the DVD recorder. If necessary, store any missing channels. Please read paragraph 'Manual TV channel search' in the chapter 'Installing your DVD Recorder'.
✓ Check the connectors at both ends of the scart cable.
✓ Check your TV's operating instructions to see which scart socket is used for video signals.
✓ If the problem persists, you won't be able to use this feature.

Problem

❸ Stop recording with **STOP** ■ .

Switching 'Direct Record' on or off

❶ Switch on the TV set. If required, select the programme number for the DVD recorder.

❷ Press **SYSTEM-MENU** on the remote control. The menu bar appears.

❸ Select '⚒' using ◀ or ▶ .

❹ Select '***Record settings***' using ▼ or ▲ and confirm with ▶ .

❺ Select '***Direct Record***' using ▼ or ▲ .

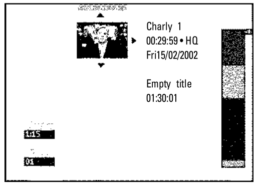
❻ Select '***On***' (Direct Record on) or '***Off***' (Direct Record off) using ◀ or ▶ .

❼ Confirm with **OK** .

❽ Quit using **SYSTEM-MENU** .

❾ Switch off with **STANDBY** ⏻ .

8 Managing the disc contents



General Information

When a recording is made to disc, the following additional information is also stored at the beginning of the recording:
•) Name of the recording
If the TV station does not transmit a name, only the channel number and time will be stored as the name
•) Length of the recording
•) Record type (Quality)
•) Date of the recording
•) Index picture of the recording

ENGLISH

A marker will be set every 5-6 minutes if the '***Auto chapters***' function is activated in the '***Record settings***' menu. This marker is known as a 'chapter'.
These markers can be changed when the recording has finished.

Can markers be set on a DVD+R disc?
Markers can be set on these discs if they have not been finalised. ?

It is also possible to add 'chapters' later. This means that scenes you do not want to see during playback, such as commercials, can be hidden or skipped. During playback you can watch your recording as a continuous sequence without the hidden chapters.

Read section '**Disc settings**', to change general settings of the disc.

Read **'Editing recording titles (name)'**to find out how to change a name.

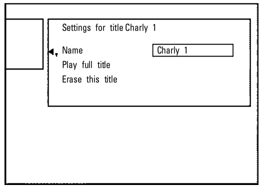
Read **'Playing back titles'**to find out how to play back the entire recording including the hidden chapters

Read **'Erasing a recording/title'**to find how to erase titles and the accompanying recording.

Read **'Favourite scene selection'**to find out how to split the title into chapters and how to manage the chapters.

Editing recording titles (name)

Some TV stations transmit the title (name) of a programme. In this case, the name will be included automatically (e.g. 'ROCKY'). Otherwise, the channel number and time of the recording are stored as the name. The name of the recording can only be changed after the recording has been completed.



Settings for title Charly 1
Name Charly 1
Play full title
Erase this title

① Press the **STOP ■** button or during playback press **DISC-MENU** .

② Using ▲ or ▼ select the title whose name you want to edit and confirm with ▶ . The menu for editing names appears.

③ Select '***Name***' using ▲ or ▼ and confirm with ▶ .

④ Using ▶ or ◀ select the position where the letter/number/icon is to be changed/re-entered.

⑤ Change the icon using ▲ or ▼ . You can switch between upper and lowercase using **SELECT** . You can delete the character using **CLEAR** .

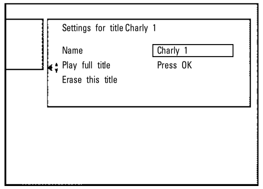
⑥ Repeat ④ and ⑤ until you have made the changes you want.

⑦ Save the new name with **OK** . '***Storing name***' appears on the TV screen for confirmation.

⑧ To end, press ◀ .

Playing back titles

If you have hidden certain chapters of a title, with this setting you can view the entire title including the hidden chapters. Proceed as follows:



Settings for title Charly 1
Name Charly 1
Play full title Press OK
Erase this title

① Press the **STOP ■** button or during playback press **DISC-MENU** .

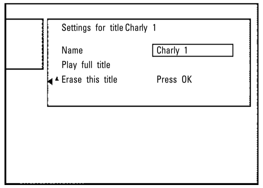
② Using ▲ or ▼ select the title that you want to play back and confirm with ▶ . The menu for editing titles appears.

③ Select '***Play full title***' using ▲ or ▼ and confirm with **OK** .

④ Playback begins automatically. The full title – including the hidden chapters - is played back.

Erasing a recording/title

You can erase individual recordings from a disc. Follow the instructions below:



❶ Press the **STOP ■** button or during playback press **DISC-MENU** .

❷ Using ▲ or ▼ select the title to be erased and confirm with ▶ . The menu for editing titles appears.

❸ Using ▲ or ▼ select '***Erase this title***' and confirm with **OK** . The screen will show '***This will completely erase this title***'. '***Press OK to confirm***'.

❹ If you want to erase the title press **OK** . To end, press ◀ .

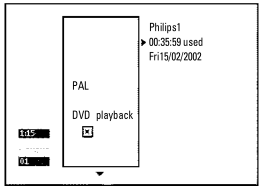
❺ The screen will show '***Erasing title***'.

❻ '***Empty title***' will now appear in this position in the Index Picture Screen. A new recording can now be made at this position.
If the deleted title was very short (shorter than 1 minute) no '***Empty title***' will be displayed.

Can titles be deleted from a DVD+R disc?
Titles on DVD+R discs are only marked as deleted. '***Deleted title***' will appear in the display instead of '***Empty title***'. During playback the 'deleted' title is skipped. The space used for this title cannot be used again as the title has not been physically deleted. Once the disc has been finalised no further changes can be made.

?

Disc settings



This screen appears **before**the first title and contains general information about the current disc.

You can:
•) change the name of the disc
•) activate or deactivate write protection on the disc
•) Finish editing (make edits DVD compatible)
•) Finalising DVD+Rs
•) Erasing DVD+RWs

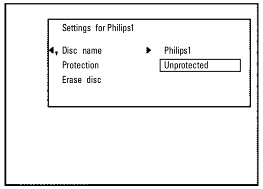
Follow the instructions to get to this screen:

❶ Press the **STOP ■** button or during playback press **DISC-MENU** .

❷ Select the first title using ▲ or press **STOP ■** .

❸ Press the ▲ button. The Disc Info screen will appear.

Changing the disc name



❶ In the Disc Info screen press ▶ . The '***Settings for***' menu appears on the TV screen.

❷ Select '***Disc name***' using ▲ or ▼ and confirm with ▶ .

❸ Using ▶ or ◀ select the position where the letter/number/icon is to be changed/re-entered.

❹ Change the icon using ▲ or ▼ . You can switch between upper and lowercase using **SELECT** . You can delete the character using **CLEAR** .

❺ Repeat ❸ and ❹ until you have made the changes you want.

❻ Save the new title with **OK** . '***Storing name***' appears on the TV screen for confirmation.

❼ To end, press ◀ .

Finalising a disc

Even if one or more titles have been edited, a DVD player may still show the original title. You can prepare your disc so that a DVD player will be able to read the edited title.

❶ In the Disc Info screen press ▶ . The '***Settings for***' menu will appear on the screen.

❷ Select '***Make edits compatible***' using ▲ or ▼ and confirm with **OK** .

× '***Make edits compatible***' **does not appear**
✓ Your disc is already compatible. No conversion is necessary.
To end, press **SYSTEM-MENU** .

Problem

❸ The screen displays '***This will take...***' to show how long the process will last.

❹ To confirm press **OK** . The screen will show '***Working...***'. A bar will move from left to right indicating the progress of the conversion.

Finalising DVD+R discs

This feature is required to play back a DVD+R disc in a DVD player. Once the disc has been finalised no further recordings or changes can be made.

❶ In the Disc Info screen press ▶ . The '***Settings for***' menu appears on the TV screen.

❷ Select '***Finalise disc***' using ▲ or ▼ . and confirm with **OK** .

× '***Finalise disc***' **does not appear**

✓ Either there is no DVD+R disc inserted or the disc is already finalised. To end, press **SYSTEM-MENU** .

× '***Settings for***' **does not appear**

✓ If the disc has been recorded on another DVD recorder, the menu may not appear. In this case, use the '***Finalise disc***' feature in the '⚒' menu, under '***Features***'.

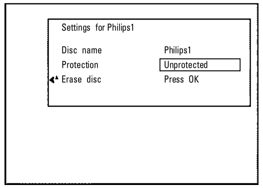
Problem

❸ The screen displays '***This will take***' to show how long the process will last.

❹ To confirm press **OK** . '***Working***' appears on the TV screen. A bar will move from left to right indicating progress.

Erasing DVD+RW disks

❶ In the Disc Info screen press ▶ . The '***Settings for***' menu will appear on the screen.



Settings for Philips1

Disc name Philips1

Protection Unprotected

Erase disc Press OK

❷ Select '***Erase disc***' using the menu buttons ▲ or ▼ . Confirm with the menu button **OK** . The screen will show '***This will erase all titles Press OK to confirm***'.

❸ If you want to erase all titles press **OK** . Otherwise press ◀ to end.

❹ The screen will show '***Erasing disc***'.

❺ Once the disc has been successfully erased the Index Picture Screen will show the empty area of the disc.

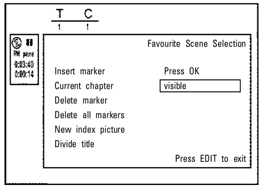
Favourite Scene Selection

In this menu, you can adjust a title to your personal preferences. You can insert/delete chapter markers, hide chapters, select a new index screen, or split the title. Display this menu during playback using **EDIT** on the remote control.

Inserting chapter markers

During playback you can set and erase chapter markers within a title.
The maximum number of chapters per disc is 124 and 99 per title. If one of these numbers are reached, the following message appears: '***Too many chapters***'. Some markers must be erased before new markers can be added.

❶ During playback press **EDIT** on the remote control at the appropriate position. The '***Favourite Scene Selection***' menu will appear on the screen.



T C

0:03:40 0:00:14

Favourite Scene Selection

Insert marker Press OK

Current chapter visible

Delete marker

Delete all markers

New index picture

Divide title

Press EDIT to exit

❷ Confirm '***Insert marker***' using **OK** . The screen displays '***Inserting marker***'.

'X' will appear on the screen:

This DVD is write-protected or the disc is a finalised DVD-R. Subsequent changes cannot be made.

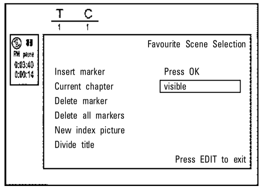
Tip

❸ To stop the feature, press **EDIT** .

Hiding chapters

By default all chapters are visible. Chapters (such as commercials) can be hidden during playback or made visible again. In editing mode, hidden chapters are shown greyed out.

❶ During playback of the appropriate chapter press **EDIT** on the remote control. The '***Favourite Scene Selection***' menu will appear on the screen.



T C

0:03:40 0:00:14

Favourite Scene Selection

Insert marker Press OK

Current chapter visible

Delete marker

Delete all markers

New index picture

Divide title

Press EDIT to exit

How do I select other chapters?

❶ Press ' **T/C** ' on the remote control. The title and chapters are shown at the top of the screen.

❷ Using ▶ or ◀ select Title(T) or Chapter (C).

❸ Using ▲ or ▼ select the title or chapter you wish to edit.

Tip

❷ Select '***Current chapter***' using ▼ .

❸ Using ▶ select '***hidden***'. The picture is shown darker.

Switching quickly

You can switch between show chapters ('***visible***') and hide chapters ('***hidden***') quickly and easily using **SELECT**.

Tip

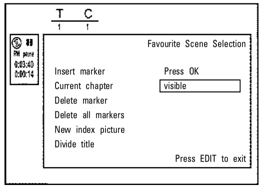
❹ To end, press **EDIT**.

During playback this chapter will be skipped.
If the chapter is not visible, select '***visible***' in step ❸ with ▶ .

Erasing chapter markers

You can erase all or some of the markers within a title .

❶ During playback of the appropriate chapter press **EDIT** on the remote control. The '***Favourite Scene Selection***' menu will appear on the screen


T C
0:03:40
0:00:14
Favourite Scene Selection
Insert marker
Current chapter
Delete marker
Delete all markers
New index picture
Divide title
Press OK
visible
Press EDIT to exit

How do I select other chapters?

❶ Press ' **T/C** ' on the remote control. The title and chapters are shown at the top of the screen.
❷ Using ▶ or ◀ select Title(T) or Chapter (C).
❸ Using ▲ or ▼ select the title or chapter you wish to edit.

Tip

❷ Using ▼ select '***Delete marker***' for this chapter or '***Delete all markers***' for all chapters within the selected title.

❸ Confirm with **OK**.

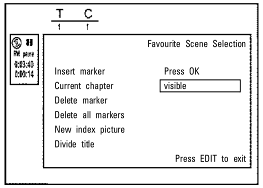
❹ To end, press **EDIT**.

Changing the index picture

Normally the first picture of a recording is used as the index picture. You can however choose any picture from the recording as the index picture.

❶ During playback, search for location of the new index picture. Press the **PLAY/PAUSE ▶II** button.

❷ Press the **EDIT** button. The '***Favourite Scene Selection***' menu appears on the TV screen.


T C
0:03:40
0:00:14
Favourite Scene Selection
Insert marker
Current chapter
Delete marker
Delete all markers
New index picture
Divide title
Press OK
visible
Press EDIT to exit

❸ Select line '***New index picture***' and confirm with **OK**.

❹ Start the change with **OK**. '***Updating menu***' appears on the TV screen.

Once the revision has been completed successfully the DVD recorder reverts to the index overview.

Dividing titles

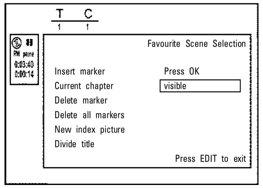
It is possible to divide a title into several separate parts (titles). Each of these parts (titles) is indicated by a separate index picture.
Please note: This division cannot be reversed

Can I also divide titles on DVD+R discs?

As recordings on DVD+R discs cannot be overwritten, it is not possible to divide titles.

?

❶ During playback of the appropriate title press **EDIT** on the remote control. The '***Favourite Scene Selection***' menu will appear on the screen


T C
0:03:40
0:00:14
Favourite Scene Selection
Insert marker
Current chapter
Delete marker
Delete all markers
New index picture
Divide title
Press OK
visible
Press EDIT to exit

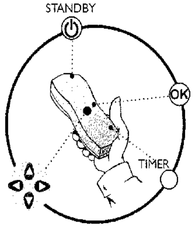
❷ Select '***Divide title***' and confirm with **OK**.

❸ If you are sure, start the process by pressing **OK**. The screen will show '***Dividing title***'.

❹ Wait until the new title appears with an index picture in the Index Picture overview.

The title is now successfully divided.

9 Programming a recording (TIMER)



General information

Use programmed recording (TIMER) to automatically start and stop a recording at a later date. The DVD recorder will switch to the right program number and begin recording at the correct time.
With this DVD recorder, you can pre-program up to 6 recordings within a period of one month.

To make a programmed recording, your DVD recorder needs to know:
* the date you want to make the recording
* the program number of the TV channel
* the start and stop time of the recording
* VPS or PDC on or off
* the recording mode ('*HQ*/*SP+*/*LP*/*EP+*').

This information is saved in a TIMER block.

ENGLISH

What is 'VPS/PDC'?

'VPS' (Video Programming System)/ 'PDC'(Programme Delivery Control) are used to control the start and duration of TV channel recordings. If a TV programme starts earlier or ends later than was scheduled, the DVD recorder will still switch itself on and off and the correct times.

What do I need to know about 'VPS/PDC'?

Usually the start time is the **same** as the VPS or PDC time. But if your TV guide gives a VPS or PDC time which is different from the programme's start time, e.g. '20.15 (VPS/PDC 20.14)', you must enter the **VPS/PDC time** '20.14' **exact to the minute** as the start time.
If you want to programme a time that is different from the VPS or PDC time, you must switch off VPS or PDC.

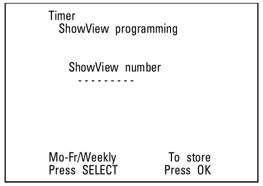
Only one TV programme on a TV channel can be controlled using 'VPS/PDC' at a time. If you want to record two or more TV programmes on a TV channel using 'VPS/PDC', you will need to programme these as two separate recordings.

Programming a recording (with 'ShowView ®')

SHOWVIEW®

Thanks to this programming system, you no longer need to tediously enter the date, programme number, start and end times. All the information needed by the DVD recorder for programming is contained in the ShowView® - programming number. This 9-digit ShowView® - number is found in most TV listings magazine.

1. Switch on the TV set. If required, select the programme number for the DVD recorder.
2. Press **TIMER** on the remote control.
   The programming method last selected is marked.
3. Select '***ShowView programming***' using ▼ or ▲ and confirm with ▶ .
4. Enter the entire ShowView number. This number is up to 9 digits long and can be found next to the start time of the TV programme in your TV listings magazine.
   e.g.: 5-312-4 or 5 312 4
   Enter 53124 for the ShowView number.
   If you make a mistake, you can clear it with **CLEAR** .



```
Timer
  ShowView programming

    ShowView number
      ---------

Mo-Fr/Weekly          To store
Press SELECT          Press OK
```

Selecting daily/weekly recordings
Using **SELECT** , select from the following options:
'***Mo-Fr***': Repeated daily recordings from Monday to Friday.
'***Weekly***': Repeated weekly recordings (every week on the same day).

Tip

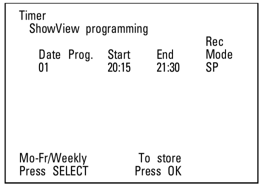
5. Confirm with **OK** .

×**The following message appears on the screen: '*Please enter programme number*'**
✓ The programme number of the TV channel has not yet been assigned to the ShowView number. Using ▶ and ◀ or the number buttons **0..9** on the remote control, select the corresponding programme number (name) of the TV channel and confirm with **OK** .

×**The following message appears on the screen: '*ShowView number wrong*'**
✓ The ShowView number entered is incorrect. Correct your entry or cancel using the **SYSTEM-MENU** button.
✓ Check the time/date (see 'Setting the time and date' in 'Installing your DVD recorder'.

×**The following message appears on the screen: '*Weekend programming not possible*'**
✓ A daily recording was entered for the wrong day. Daily programming can only be used for recordings to be made from Monday to Friday.

Problem



```
Timer
  ShowView programming
                                  Rec
    Date  Prog.   Start    End    Mode
    01            20:15    21:30  SP



Mo-Fr/Weekly         To store
Press SELECT         Press OK
```

❻ The decoded information appears after confirmation. You can go back at any time to change the information. Select the appropriate input field using ▶ or ◀. If required, change the information using **CHANNEL +** , **CHANNEL −** or the number buttons **0..9** .

Switching on 'VPS/PDC' in the '*Start*' input field
Select the '*Start*' input field using ▶ . Using **SELECT** switch on 'VPS/PDC' ('*' lights up). If you press **SELECT** again, you will switch 'VPS/PDC' off ('*' disappears).

Changing the recording quality in the '*End*' input field
Select the '*End*' input field using ▶ . Using **SELECT** , select the recording mode '***HQ***, ***SP+***, ***EP***, ***EP+***'.

Tip

❼ If all the information is correct, press the **OK** button. The programming information is stored in a TIMER block.

❽ To end, press **TIMER** .

❾ Load a DVD (unprotected) ready for recording.
The current disc is checked.

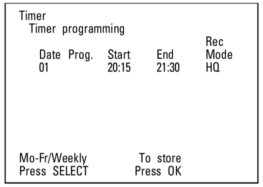
❿ Switch off with **STANDBY** ⏻ .
The programmed recording will only function properly if the DVD recorder has been **switched off**using the **STANDBY** ⏻ button.

If any of the TIMER blocks are in use, '⏲' will light up on the display.

Programming a recording (without ShowView®)

❶ Switch on the TV set. If required, select the programme number for the DVD recorder.

❷ Press **TIMER** on the remote control.
The programming method last selected is marked.



```
Timer
  Timer programming
                                  Rec
    Date  Prog.   Start    End    Mode
    01            20:15    21:30  HQ



Mo-Fr/Weekly         To store
Press SELECT         Press OK
```

❸ Select '***Timer programming***' with ▼ or ▲ . and confirm with ▶ .
The current information will appear on the screen.

❹ Select the input field with ◀ or ▶ .

❺ Enter information with ▼ or ▲ or with the number buttons **0..9** .

Selecting daily/weekly recordings
In '***Date***' use **SELECT** to select from the following options:
'***Mo-Fr***': Repeated daily recordings from Monday to Friday
'***Mo***': Repeated weekly recordings (every week on the same day, e.g. Monday).

Programme numbers of scart sockets '*EXT1*' and '*EXT2*'
You can also programme recordings from external sources via scart socket **EXT 1 TO TV-I/O** ('***EXT1***') or **EXT 2 AUX I/O** ('***EXT2***').

'Switching on 'VPS/PDC' in the '*Start*' input field
Select the '***Start***' input field using **TIMER** . Using **SELECT** switch on 'VPS/PDC' ('*' lights up). If you press **SELECT** again, you will switch 'VPS/PDC' off ('*' disappears).

Changing the recording quality in the '*End*' input field
Select the '***End***' input field using **TIMER** .
Using **SELECT** , select the recording mode '***HQ***, ***SP+***, ***EP***, ***EP+***'.

Tip

❻ If all the information is correct, press **OK** . The programming information is stored in a TIMER block.

❼ To end, press **TIMER** .

❽ Load a DVD (unprotected) ready for recording.
The cassette is being checked.

❾ Switch off with **STANDBY** ⏻ .
The programmed recording will only function properly if the DVD recorder has been **switched off**using the **STANDBY** ⏻ button.

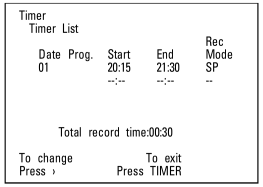
If any of the TIMER blocks are in use, '⏲' will light up on the display.

How to check, change or delete a programmed recording (TIMER)

❶ Switch on the TV set. If required, select the programme number for the DVD recorder.

❷ Press **TIMER** on the remote control.
The programming mode last selected is marked.

❸ Select '***Timer List***' with ▼ or ▲ . and confirm with ▶ .



```
Timer
  Timer List
                                       Rec
    Date  Prog.   Start     End       Mode
    01            20:15     21:30     SP
                  --:--     --:--     --

         Total  record  time:00:30

To  change                To  exit
Press ›               Press  TIMER
```

❹ Select the programmed recording (TIMER) you want to check, change or delete with ▼ or ▲ .

Tip

Delete programmed recording

❶ Press the **CLEAR** button.

❷ Confirm with **OK** . '***Timer Cleared***' will briefly appear on the TV screen.
'-- ---' appears rather than the displayed values

❸ To end, press **TIMER** .

❺ Press ▶ .
Select the input field with ◀ or ▶ .
If required, change the information with **CHANNEL +** , **CHANNEL −** or the number buttons **0..9** .

❻ Confirm with **OK** .

❼ To end, press **TIMER** .

❽ Switch off with **STANDBY** ⏻ .

'NexTView Link'

This DVD recorder is equipped with the 'NexTView Link' function. If your television is also equipped with this feature, you can mark TV programmes on the television for programming. These TV programmes will automatically be transmitted to a TIMER block on the DVD recorder. If you clear this marking on the television, the corresponding TIMER block on the DVD recorder will also be cleared.
For more information, read the instruction manual for your TV set.

Problem solving for programmed recordings

PROBLEM	SOLUTION
DVD recorder is not responding	✓While a programmed recording is being made, you cannot operate your recorder manually. If you want to cancel the programmed recording, press **STANDBY** ⏻ .
'*Switch off, timer recording*' flashes on the TV screen.	✓The DVD recorder was switched on several minutes before the start of a programmed recording. Switch off the DVD recorder with **STANDBY** ⏻ . A programmed recording (timer) will only function if the DVD recorder is switched off (button **STANDBY** ⏻).
Error message: '*Insert recordable disc*'	✓Either no disc has been inserted or you cannot record to this disc. Insert a disc that you can record onto. Switch off the DVD recorder using **STANDBY** ⏻ .
The error message '*Disc locked*' appears briefly on the screen.	✓A write-protected disc has been inserted. Cancel the protection (see 'Preventing accidental erasing of discs' in 'Manual Recording') or insert a different disc.
Error message: '*Memory full*'	✓If this error message appears after pressing **TIMER** , then all the TIMER blocks are already programmed. No more recordings can be programmed. Press the ▶ button. If you want to clear or check a programmed recording (TIMER block), select it with **CHANNEL +** or **CHANNEL −** .
The '*Data error*' message appears on the screen.	✓The data for the recording could not be transferred. Please check the date, start time and end time of the programmed recording.
'*Collision*' appears on the screen.	✓The information for two programmed recordings overlap. ✓If you ignore this error message the TV programme with the earlier start time will be recorded first. You will miss the start of the second programme. ✓Change the information for one of the recordings. ✓Delete one of the recordings

10 User preferences

In this section you will learn how to set your user preferences on the DVD recorder. The symbols have the following meanings:

- **Picture setting**
- **Sound setting**
- **Language setting**
- **Additional settings**
- **Remote control settings**
- **Recording settings**
- **Installation**

ENGLISH

❶ Switch on the TV set. If required, select the programme number for the DVD recorder.

❷ Press **SYSTEM-MENU** on the remote control. The menu bar appears.

❸ Select the '🛠' icon using ◀ or ▶ and confirm with ▼ .

❹ Select the appropriate feature using ▼ or ▲ and confirm with ▶ .

❺ Select the corresponding line using ▼ or ▲ and confirm with ▶ .

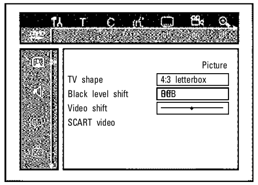
❻ Select the appropriate feature using ▼ or ▼ or the setting using ◀ or ▶ .

❼ Confirm the setting with **OK** .

❽ Quit the menu item using ◀ .

Picture settings

You can choose the following features in this menu:



TV shape: 4:3 letterbox
Black level shift: BBB

'TV shape'

The picture signal from your DVD Recorder can be set to match your TV screen:

'***4:3 letterbox***' : for a 'wide-screen' picture with black bars at the top and bottom

'***4:3 panscan***' : for a full-height picture with the sides trimmed

'***16:9***' : for a wide-screen TV set (screen edge ratio 16:9)

'Black level shift'

Adapts the colour dynamics for NTSC playback

'Video shift'

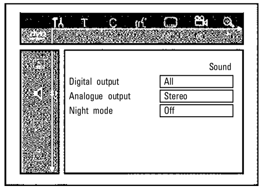
Use this feature to adjust the position of the picture on your TV left or right using ◀ , ▶ to suit your TV set.

'SCART video'

By default the recorder is set to '***RGB***'. Select '***S-Video***' if you want to connect an S-VHS recorder.

Sound settings

Depending on which audio outputs are used, you can select the settings in this menu.
If you only use the analogue audio output (**OUT L AUDIO R**), select the settings '***Off***' in the '***Digital output***' menu.



Digital output: All
Analogue output: Stereo
Night mode: Off

'Digital output'

For devices connected to the **DIGITAL AUDIO OUT** socket, you can select from the following settings.

'***All***': Dolby Digital and DTS signals are fed unaltered to the digital output. MPEG-2 multi-channel signals are converted to PCM (Pulse Code Modulation).
For receivers/amplifiers **with digital multi-channel sound decoders**.

'***PCM only***': Dolby Digital and MPEG-2 multi-channel signals are converted to PCM (Pulse Code Modulation).
For receivers/amplifiers **without digital multi-channel sound decoders**.

'***Off***': Digital output switched off.
For devices **with analogue audio input**.

'Analogue output'

For devices connected to the analogue audio output (**OUT L AUDIO R**), you can select from the following settings.

'***Stereo***': For devices without DolbySurround or TruSurround. Use this setting if the DVD recorder is only connected to a stereo TV set.

'***Surround***': Dolby Digital and MPEG-2 multi-channel are mixed down to a DOLBY surround-compatible two-channel output signal. For recorders**with Dolby Surround Pro Logic decoder** .

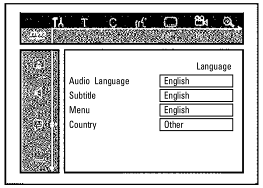
'***3D sound***': The six channels of the digital surround sound (Dolby Digital, MPEG-2) are mixed down to a two-speaker output signal. All original audio information is retained
The result is an impression of being surrounded by several loudspeakers.
For TruSurround compatible devices.

'Night mode'

Night mode optimises the sound for playback at low volume. You are therefore less likely to disturb your neighbours. This only works for Dolby Digital audio on DVD video discs.

Language settings

You can choose the following settings in this menu:



Audio Language English
Subtitle English
Menu English
Country Other

'*Audio Language*'

Playback audio language*Audio Language*',

'*Subtitle*'

Subtitle language

'*Menu*'

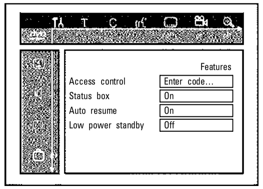
Screen menu language

'*Country*'

'*Country*'

Additional settings

You can select the following functions in this menu:



Access control Enter code...
Status box On
Auto resume On
Low power standby Off

'*Access control*'

Please read the next chapter 'Access control (child lock)'

'*Status box*'

Along with the on screen menu, the OSD (On Screen Display) also displays information on the current operating status (counter, playback, recording, TV channel, etc.) on the TV screen. You can switch off the information about the operating status to avoid recording it when recording from additional devices.

'***On***': The OSD information appears in every selected mode for a few seconds and disappears again.

'***Off***': The OSD information is switched off. It is **no longer** displayed on the screen.

Auto resume

If playback of a pre-recorded DVD video disc or video CD is interrupted (button **STOP ■** or **OPEN/CLOSE**) when the disc is reloaded (disc is started) playback starts at the precise location where it stopped. This applies not only to the current disc but to the last 20 discs played.

This feature can be switched off if not required.

Low power standby

To save power, you can switch off the clock display on the DVD recorder. Programmed (TIMER) recordings will still take place.

'***On***': If the DVD-Recorder is switched off (button **STANDBY ⏻**), the clock display is also switched off.

'***Off***': If the DVD-Recorder is switched off (button **STANDBY ⏻**), the clock display is visible.

'*PBC*'

This line appears only if a VCD is loaded.
This function lets you activate or deactivate the PBC menu (Playback Control) for video CDs. See 'Playing a (Super) Video CD'.

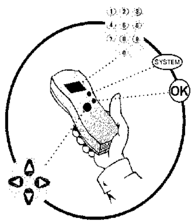
Remote Control settings

In this menu you can set the remote control type to which your DVD recorder should respond to.

'***DVD player***': The DVD recorder responds to a DVD player remote control.
The DVD recorder also responds to the remote control of a DVD player (remote control code RC-6). Choose this setting if your Philips TV remote supports DVD functions.

'***DVD recorder***': The DVD recorder only responds to the supplied remote control.

11 Access control (Child Lock)



Child lock (DVD and VCD)

This feature enables discs to be locked for children.
When Child Lock is on, a 4-digit code (PIN) needs to be entered before a disc can be played.
You can also decide whether the inserted disc should always be played or should be played only once, despite the child lock

•)'*Play always*':
This disc is stored in a memory with space for 50 child-safe discs. If more than 50 discs are stored, the last disc in the list is removed and the new disc is added. The screen shows 'Child safe' at the start of playback.

•)'*Play once*':
This disc is only authorised for single playback. If the recorder is switched off, the PIN code must be re-entered.

Activating/deactivating child lock

❶ Switch on the TV set. If required, select the programme number for the DVD recorder.

❷ Switch on the DVD recorder using **STANDBY/ON** .

❸ Press **SYSTEM-MENU** . The menu bar appears

❹ Select the '⚒' icon using ◀ or ▶ .

❺ Select '***Features***' using ▼ or ▲ and confirm with ▶ .

❻ Confirm '***Access control***' using ▶ .

❼ Enter a 4-digit code of your choice. Enter the same code again as confirmation.

❽ Select '***Child lock***' using ▲ or ▼ and confirm with ▶ .

❾ Select the '🔒' icon using ▼ or ▲ .

❿ Confirm with **OK** .

⓫ Quit the feature using ◀ and **SYSTEM-MENU** .

Unauthorised discs can only be played by entering the four-digit PIN code.
To deactivate the child lock, select the '🔓' icon in ❾ .

Authorising a disc

❶ Insert a disc. The access control box will appear after a short delay.

❷ Using ▲ or ▼ select '***Play once***' or '***Play always***'.

❸ Enter your PIN code using the number buttons **0..9** .

Double-sided DVDs may have a different ID for each side. For these discs, each side must be authorised. Multi-volume video CDs may have a different ID for each volume. For these CDs, each volume must be authorised.

Locking unlocked discs

To lock a disc that was formerly authorised follow the instructions below

❶ Insert a disc. Playback starts automatically. If the playback does not start automatically, press **PLAY/PAUSE ▶II** .

❷ Press the **STOP ■** button while the 'safe' icon is visible. The icon changes to 'locked'. The disc is now locked.

Parental level control (DVD video only)

Films on pre-recorded DVD discs may contain scenes not suitable for children. Therefore, some discs may contain 'Parental Control' rating information that applies to the entire disc or to certain scenes on the disc.

If the disc is rated, scenes are rated from 1 to 8 If such a scene is detected during playback, it compares the scene with the filter value set on the DVD recorder. If the filter value is higher that the setting, an alternative scene is played back where possible.

Activating/deactivating parental level control

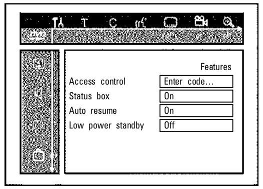
❶ Switch on the TV set. If required, select the programme number for the DVD recorder.

❷ Switch on the DVD recorder using **STANDBY/ON** .

❸ Press **SYSTEM-MENU** . The menu bar appears

❹ Select the '⚒' icon using ◀ or ▶ .

❺ Select '***Features***' using ▼ or ▲ and confirm with ▶ .


Features

Access control: Enter code...
Status box: On
Auto resume: On
Low power standby: Off

❻ Confirm '***Access control***' using ▶ .

❼ Enter a 4-digit code of your choice. If the code is new, you may have to enter the code a second time as confirmation.

❽ Select the '***Parental level***' using ▲ or ▼ and confirm with ▶ . A bar appears to select the parental level.

❾ Select the appropriate rating using ▼ , ▲ or the number buttons **0..9** .

What do the ratings mean?
Rating 0 (displayed as '--') parental control not active.
Rating 1 (suitable for children)
Rating 8 (only suitable for adults)

What happens if a DVD scene contains a higher level than the rating set?
If the recorder does not find a suitable alternative, playback will stop and you must enter the four-digit code.

Tip

❿ Confirm with **OK** . Quit using ◀ and **SYSTEM-MENU** .

Changing the country

The set filter values depend on the respective country. It is therefore necessary to enter the country to which these filter values apply.

❶ Switch on the TV set. If required, select the programme number for the DVD recorder.

❷ Switch on the DVD recorder using **STANDBY/ON** .

❸ Press **SYSTEM-MENU** . The menu bar appears

❹ Select the 'T⅄' icon using ◀ or ▶ .

❺ Select line '***Features***' using ▼ or ▲ and confirm with ▶ .

❻ Confirm the line '***Access control***' using ▶ .

❼ Enter your four-digit code.

❽ Select '***Change country***' using ▼ or ▲ and confirm with ▶ .

❾ Select the corresponding country using ▲ or ▼ and confirm with **OK** .

❿ To end, press ◀ and then **SYSTEM-MENU** .

Changing the PIN code

❶ Switch on the TV set. If required, select the programme number for the DVD recorder.

❷ Switch on the DVD recorder using **STANDBY/ON** .

❸ Press **SYSTEM-MENU** . The menu bar appears

❹ Select the 'T⅄' icon using ◀ or ▶ .

❺ Select '***Features***' using ▼ or ▲ and confirm with ▶ .

❻ Confirm '***Access control***' using ▶ .

❼ Enter your four-digit PIN code.

❽ Select '***Change code***' using ▲ or ▼ and confirm with ▶ .

❾ Enter the new code using the number buttons **0..9** . Enter the same code again as confirmation.

❿ Quit using ◀ and **SYSTEM-MENU** .

I have forgotten my code
Press **STOP ■** four times, then press **OK** . Access control is now switched off. You can now enter a new code as described above.

Tip

12 Before you call an engineer

If you have any problems using this DVD recorder, the reason may be one of the following. You can also call the **customer service centre**in your country.
The telephone numbers can be found on the back of this instruction manual.
Have the model number (MODEL NO) and the production number (PROD.NO) of your recorder ready.
The serial number (PROD. NO.) is printed on the type plate at the back.

ENGLISH

PROBLEM	SOLUTION
Your recorder does not respond to any button being pressed and the display shows 'TV ON ':	✓Recorder in initial installation mode: Switch on the TV, switch over to the DVD recorder socket. Now the menu for language selection should appear. Please read paragraph 'Initial Installation' in the chapter 'Installing your DVD Recorder'.
The device does not react when you press a button, although the remote control works:	✓'Dealer-Mode' is switched on: All buttons on the front of the set are locked. Switch off the function: ❶ Pull out the mains plug from the wall outlet. ❷ Press and hold down **■STOP** and **OPEN/CLOSE** and put back the mains plug into the wall outlet. ❸ As soon as the time or '--:--' appears in the display (ca. 6 - 10 seconds), release **■STOP** and **OPEN/CLOSE** .
Your DVD recorder does not respond to any button being pressed:	✓There is no power supply: check the power supply ✓A programmed recording (Timer) is currently being made: If desired, cancel the programmed recording (Timer) with **STANDBY** ⏻ . ✓There is a technical problem: disconnect from the mains power supply for 30 seconds, then connect again. If this doesn't help, you can reset your DVD recorder to the default factory settings.
Resetting the machine to the default factory settings	✓**Important:** All the information stored (TV channels, time and date, TIMER) will be lost. ❶ Disconnect from the mains power supply. ❷ Press and hold down the **STANDBY/ON** button on the device and reconnect to the mains power supply. ❸ Release the **STANDBY/ON** button when 'TV ON ' appears on the display. All the information stored (TV channels, time and date, TIMER) will be lost. Please read paragraph 'Initial Installation' in the chapter 'Installing your DVD Recorder'.
Remote control does not work:	✓Remote control not pointed toward the DVD recorder: Point the remote control at the machine. ✓There is a technical problem: Take out the batteries, wait for 10 seconds and put them in again. ✓Batteries are flat: Change the batteries.

PROBLEM	SOLUTION
No playback on DVD recorder:	✓There is no recording on the disc: Change disc. ✓You inserted the wrong disc type: Your recorder can play back the following disc types: DVD Video, (Super)Video CD, DVD+R(W), Audio CD, , MP3 CDs ✓You inserted the disc the wrong way: Insert the disc with the label facing upwards ✓Disc is dirty: Clean the disc ✓Wrong region code: The region code of the DVD and the DVD recorder must match. ✓Parental control is on: Read chapter 'Access control (child lock)' ✓You have selected the wrong programme number for the DVD recorder on the TV: on the TV, select the correct programme number for the DVD recorder. ✓The cable connecting the TV set and the DVD recorder has come loose: check the cable.
I cannot playback (Super) Video CDs	✓It is possible that this (Super) Video CD contains a menu and the 'PBC' is switched off. You can see this in status field '***PBC OFF***'. To activate this function, proceed as follows: ❶ Press **SYSTEM-MENU** while the (Super) Video-CD is inserted . ❷ Select 'T⅄' using ◀ or ▶ . ❸ Select line '***Features***' using ▼ or ▲ and confirm with ▶ . ❹ Select '***On***' in line '***PBC***' using ▼ or ▲ . ❺ Confirm with **OK** and end with **SYSTEM-MENU** .
Poor playback on DVD recorder: (distorted picture/distorted sound)	✓Your TV set is not properly adjusted. ✓Disc is dirty: Clean the disc ✓Sometimes the picture may be temporarily distorted. This is not a defect of your DVD recorder.
No recording possible:	✓The TV channel you want to record is not stored or you selected the wrong programme number: Check TV channels stored. ✓Disc write-protected (recording protected): Remove write-protection or change the disc. For more information, please see 'Preventing accidental erasing of discs' in chapter 'Manual Recording'. ✓An already finalised DVD+R has been inserted: Change disc.
Programmed recording does not work:	✓You have programmed the wrong time or date: Check time/date. ✓You have not set the TIMER properly: Check the programmed recordings (TIMER block). ✓Locked disc inserted: Remove disc lock. ✓An already finalised DVD+R has been inserted: Change disc. ✓'VPS/PDC' switched on but 'VPS/PDCtime' wrong: 'Enter 'VPS/PDCtime exactly to the minute. Check the aerial.
The wrong TV channel was decoded (entered) after you programmed a recording using ShowView.	❶ Enter the ShowView programming number of the TV channel you want. ❷ Confirm with **OK** . ❸ Check the programme number/channel name in the '***Prog.***' input field ❹ If this does not correspond to the TV channel you want, select the input field and change the programme number/channel name. ❺ Confirm with **OK** .
There is picture or sound interference on TV reception:	✓Switch to recording mode 'HQ' with **REC MODE** during playback from the internal TV tuner (**MONITOR** button). This will help achieve the best possible picture quality. Before recording, select the recording mode as described in chapter 'Manual Recording', section 'Selecting the recording mode (quality)'. ✓Have your aerial checked. ✓You will find information on how to change the TV system in 'Manual TV channel search' in 'Installing your DVD recorder'.

PROBLEM	SOLUTION
Distorted sound coming from a connected hi-fi amplifier	✓The DVD recorder is connected to the 'Phono-input' of your amplifier: This socket is provided only for record players without a preamplifier. Select a different audio input.
The picture is distorted or black-and-white during playback	✓The TV system of the disc does not match that of your TV set (PAL/NTSC). ✓The recording can be made in colour only when the TV channels or the connected additional device send a colour signal. Black-and-white signals containing no color information (colour subcarriers) cannot be recorded.
No sound signal at the digital output	✓Check whether the sound settings match the selected inputs and connected additional devices. ✓Check whether you have inserted an MP3 CD: In accordance with SDMI (Secure Digital Music Initiative), the digital audio output is turned off during MP3 playback. This is not a defect of your DVD recorder.
A DVD+RW disc cannot be played on certain DVD players	✓If a recording is too short, it is possible that a DVD player cannot detect it: Please observe the following 'Minimum recording times': Recording mode '***HQ***': 5 minutes, '***SP+***': 15 minutes, '***EP***': 20 minutes, '***EP+***': 30 minutes ✓Some DVD players cannot play back DVD+RW recordings. You can solve this problem by using a special function. You can solve this problem by using a special function: ❶ Open the disc tray with **OPEN/CLOSE** . Insert the disc but do not close the tray. ❷ Hold down the number button **2** on the remote control until the tray closes. The disc is modified. ❸ If this fails to produce the desired result, repeat the procedure using the number button **3** on the remote control. ❹ You can restore the disc to its original condition by pressing **1** . **Warning!** There is a risk that you can no longer play the disc on other DVD players after this procedure. Therefore, apply this function with particular care.
Other disc errors	✓If it is impossible to play back a disc, you can try and repair it for new recordings using the following function. This will only prepare the disc for erasing. It will not be erased, however, until the recording has been completed. ❶ Clean the disc ❷ Open the disc tray with **OPEN/CLOSE** . Insert the disc but do not close the tray. ❸ Hold down **CLEAR** on the remote control until the tray closes. The disc is prepared for erasing. ❹ Start recording as with an empty disc.

4. Mechanical Instructions

4.1 Service Positions

4.1.1 Front

Front

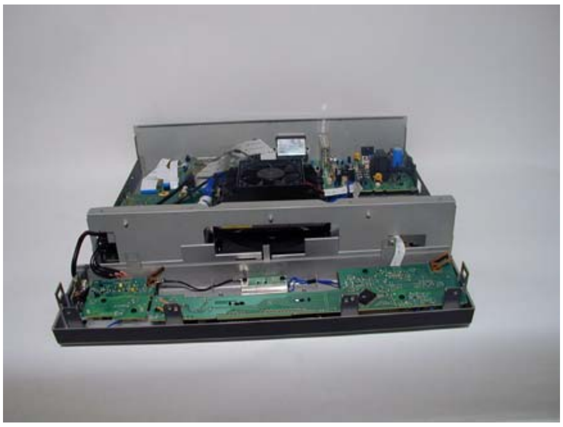


Figure 4-1

4.1.2 DVIO board

To put the DVIO board in a service position, an extender board must be used. This extender board can be ordered with codenumber 3104 128 07770.

DVIO Extender

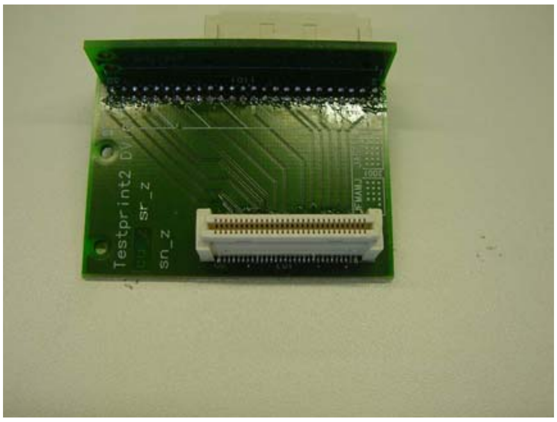


Figure 4-2

DVIO 1

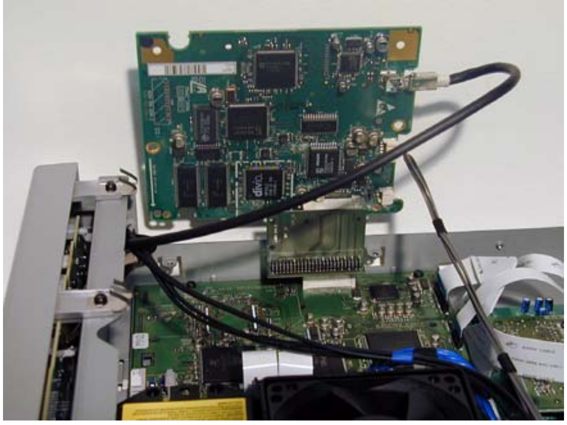


Figure 4-3

DVIO 2

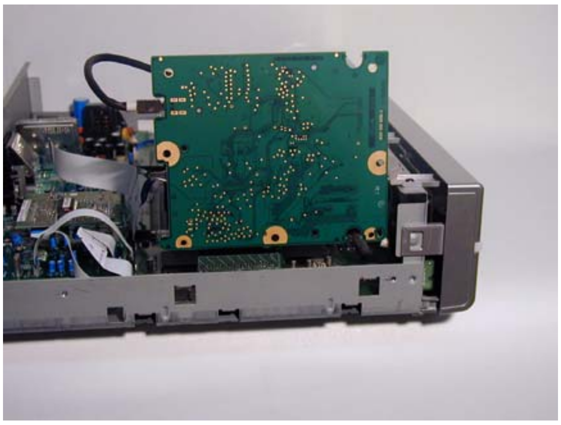


Figure 4-4

4.1.3 Digital board

After demounting of DVIO board, the top side of the digital board is in reach. To reach the bottom side of the digital board, the DVDR module must be demounted together with the digital board. Connected to each other, the assembly can be set in a service position. In this position, the bottom side of the digital board and the servo board are in reach to be serviced.

Digital 1

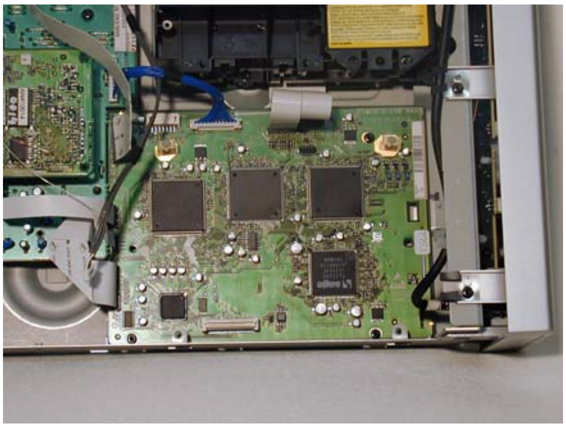


Figure 4-5

Digital 2

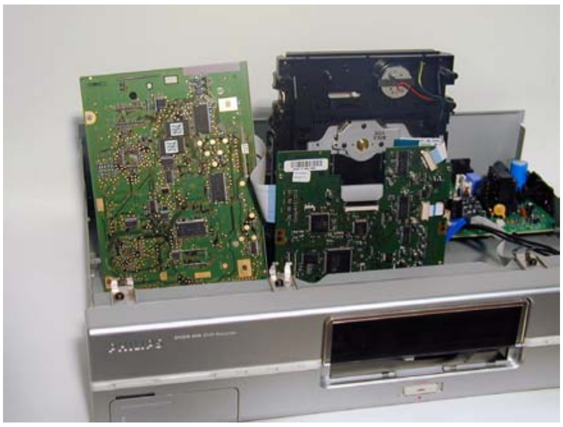


Figure 4-6

4.1.4 Analog board

To put the analog board in service position, demount the assembly of analog board and backplate as follows:

1. Remove the screw from the backplate to the mains inlet of the power supply
2. Remove the screw safety holder
3. Remove the 3 screws of the analog board to the frame
4. Release the snap of the spacer of the analog board to the frame.

Turn the assembly of the back plate and the analog board against the loader.

Analog Europe

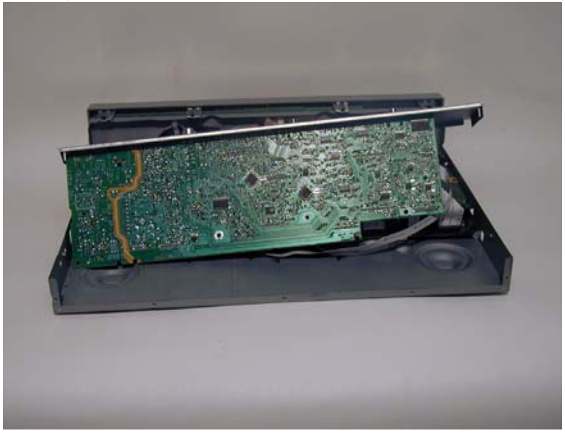


Figure 4-7

Analog NAFTA

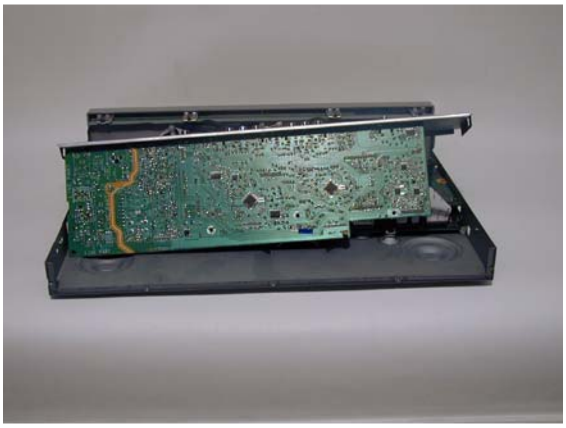


Figure 4-8

4.1.5 Cable Routing

Take care of the correct cable routing. See pictures below.

Europe

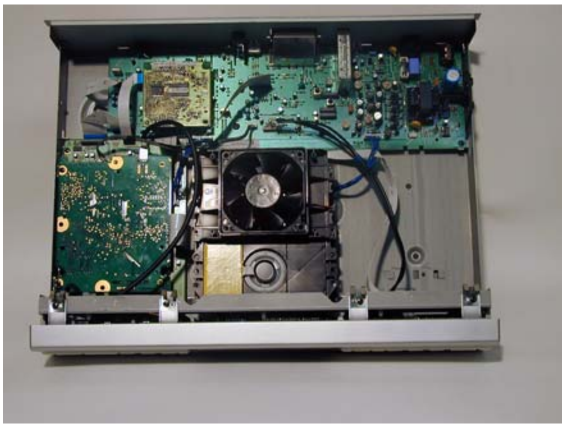


Figure 4-9

NAFTA

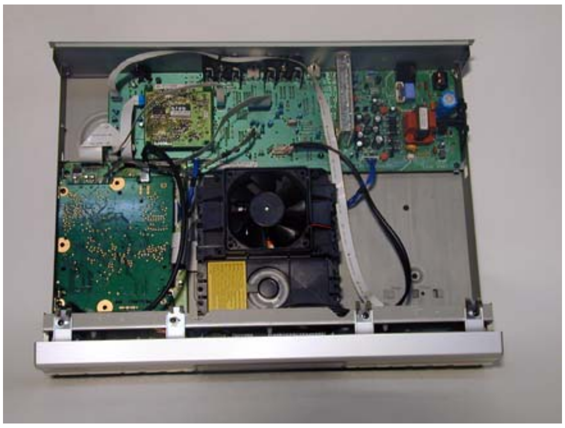
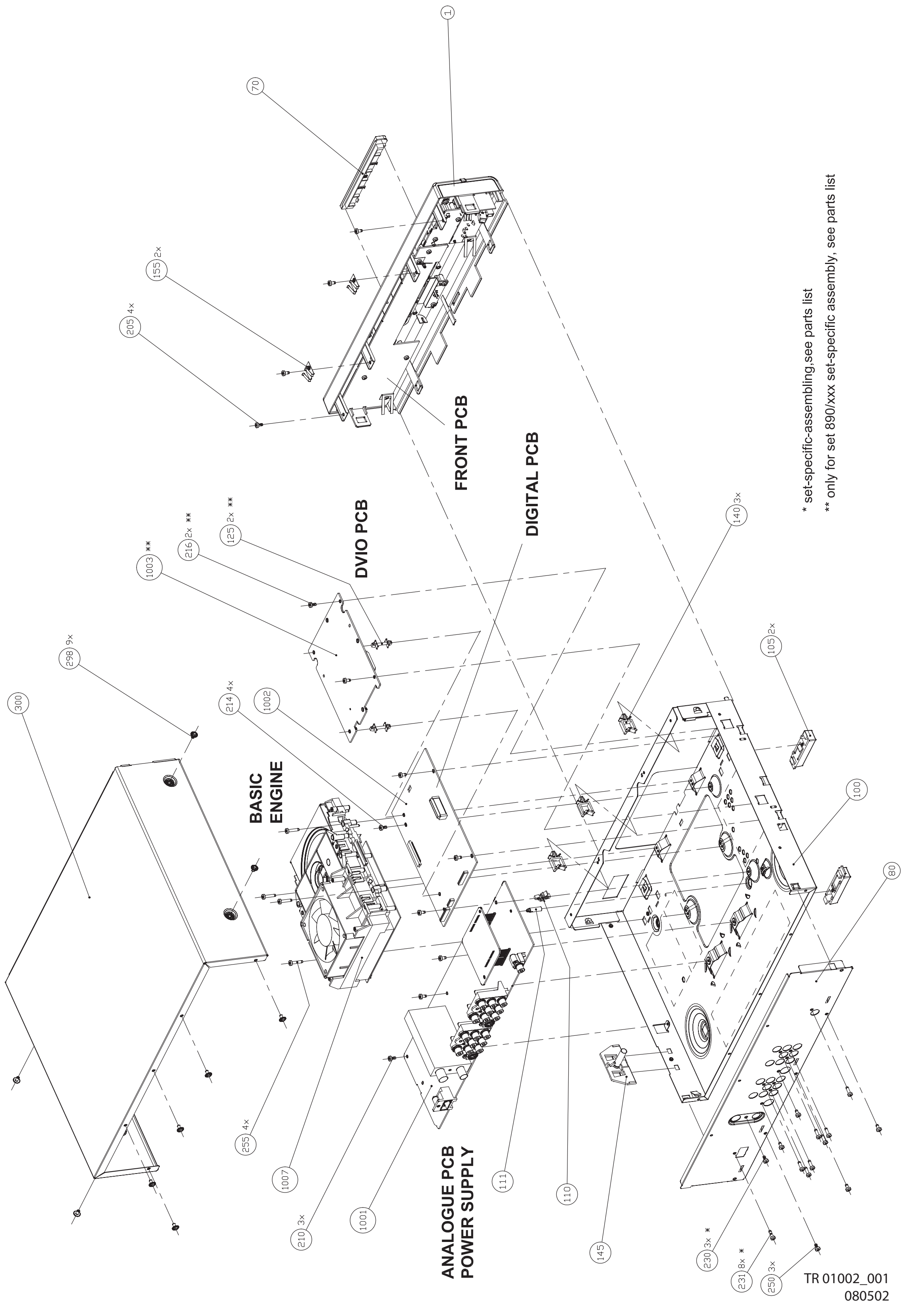


Figure 4-10

4.2 Exploded View of the Set


1
70
155 2×
205 4×
FRONT PCB
DIGITAL PCB
DVIO PCB
125 2× **
216 2× **
1003 **
298 9×
300
214 4×
1002
BASIC ENGINE
140 3×
105 2×
100
80
255 4×
1007
210 3×
1001
ANALOGUE PCB
POWER SUPPLY
111
110
145
230 3× *
231 8× *
250 3×

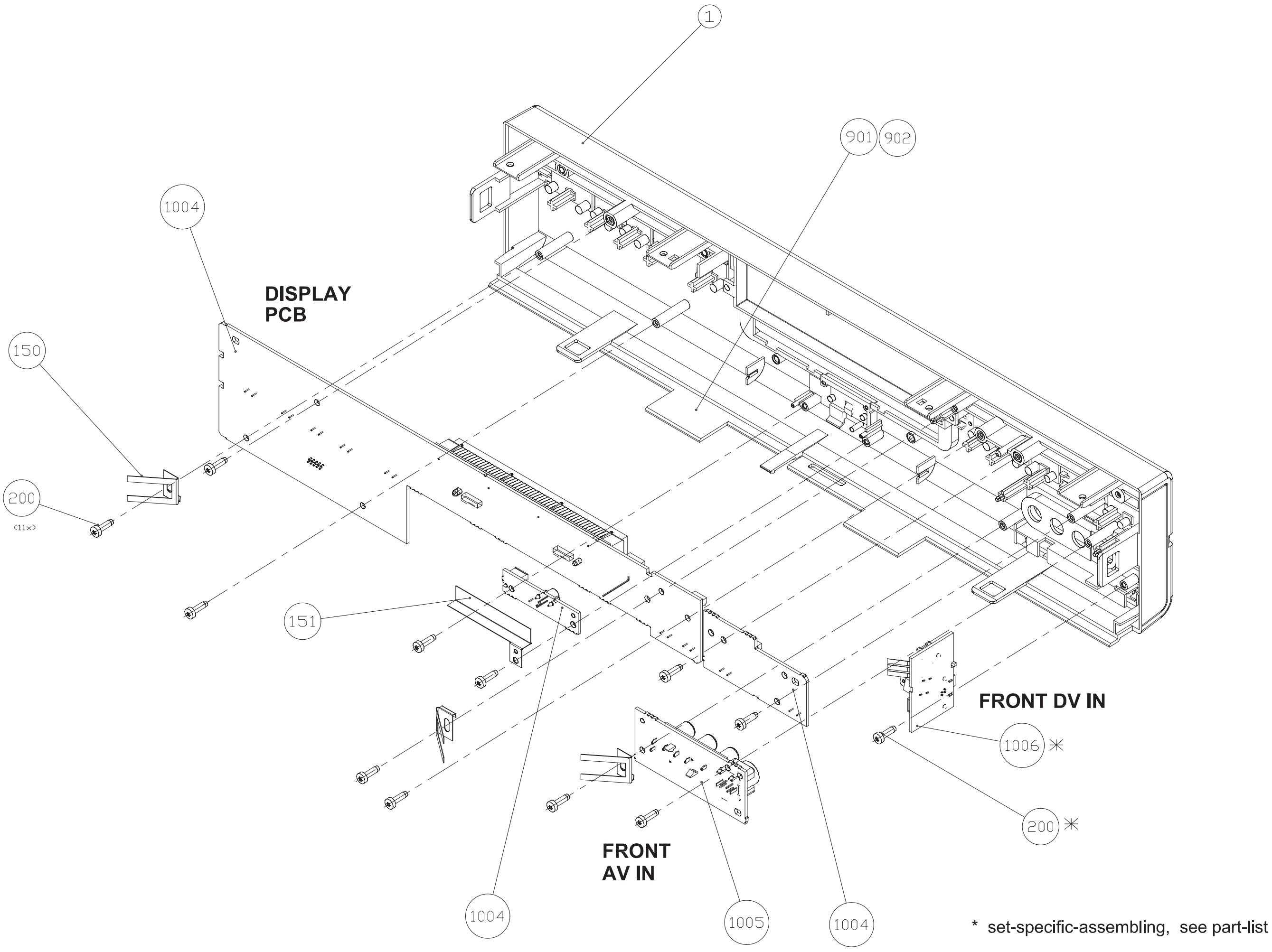
* set-specific-assembling,see parts list

** only for set 890/xxx set-specific assembly, see parts list

TR 01002_001
080502

Figure 4-11

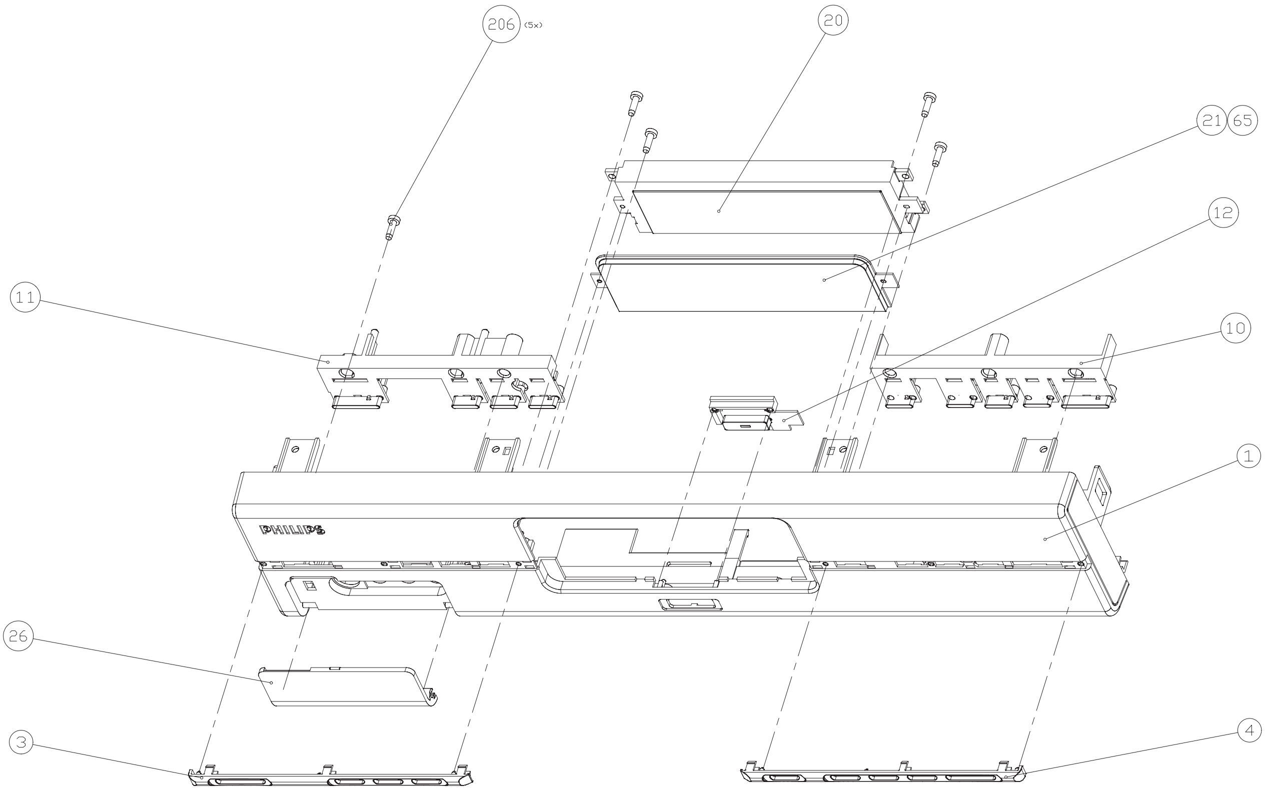
4.3 Exploded View of the complete Front Panel


1
901
902
1004
DISPLAY PCB
150
200
(11×)
151
FRONT DV IN
1006 ✳
200 ✳
FRONT AV IN
1004
1005
1004
* set-specific-assembling, see part-list

TR 01003_001
080502

Figure 4-12

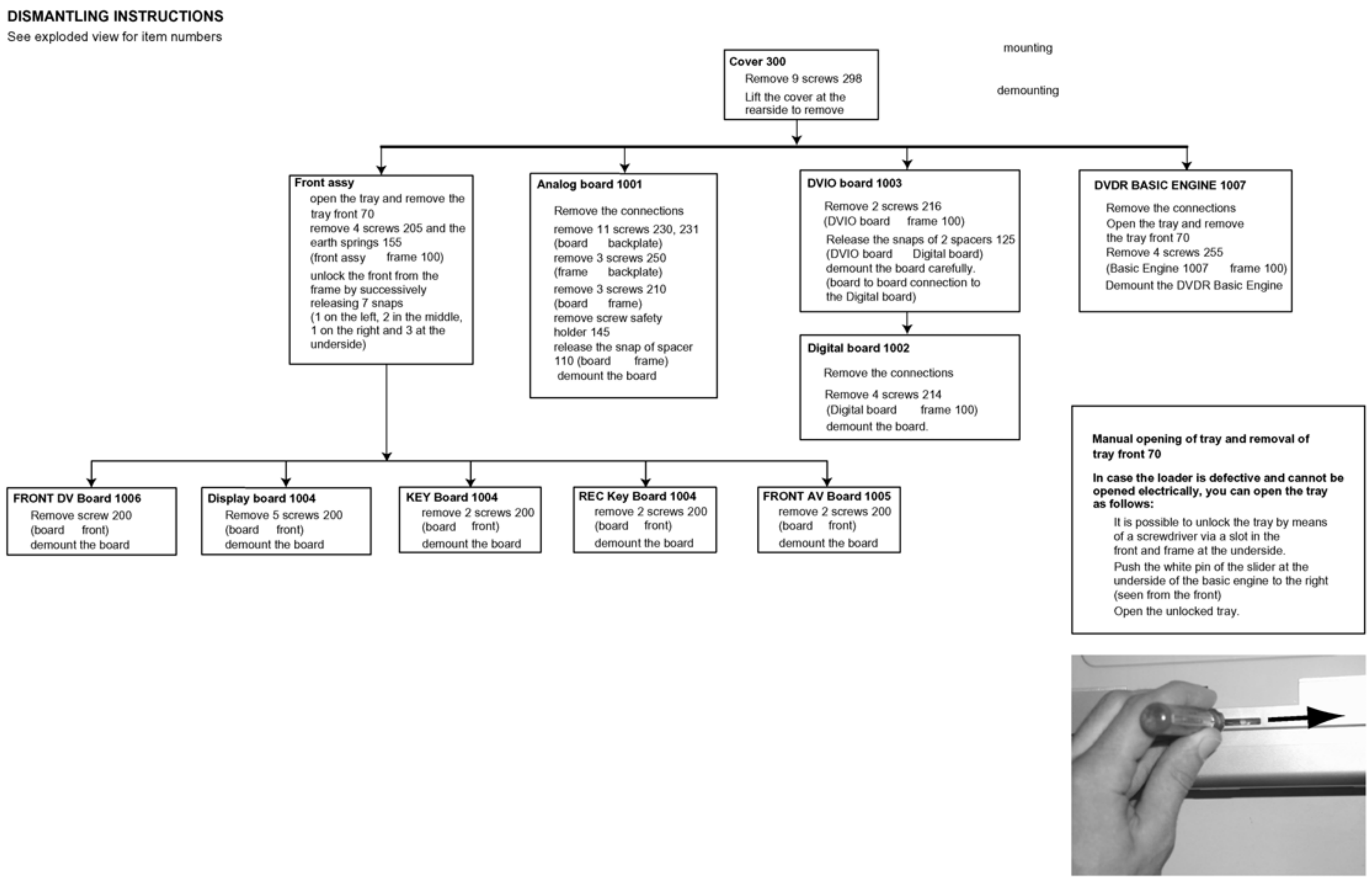
4.4 Exploded View of the Front without PWBs


206
(5x)
20
21
65
12
11
10
1
PHILIPS
26
3
4

TR 01004_001
080502

Figure 4-13

4.5 Dismantling Instructions



DISMANTLING INSTRUCTIONS
See exploded view for item numbers

Cover 300
Remove 9 screws 298
Lift the cover at the rearside to remove

Front assy
open the tray and remove the tray front 70
remove 4 screws 205 and the earth springs 155
(front assy frame 100)
unlock the front from the frame by successively releasing 7 snaps
(1 on the left, 2 in the middle, 1 on the right and 3 at the underside)

Analog board 1001
Remove the connections
remove 11 screws 230, 231
(board backplate)
remove 3 screws 250
(frame backplate)
remove 3 screws 210
(board frame)
remove screw safety holder 145
release the snap of spacer 110 (board frame)
demount the board

DVIO board 1003
Remove 2 screws 216
(DVIO board frame 100)
Release the snaps of 2 spacers 125
(DVIO board Digital board)
demount the board carefully.
(board to board connection to the Digital board)

Digital board 1002
Remove the connections
Remove 4 screws 214
(Digital board frame 100)
demount the board.

DVDR BASIC ENGINE 1007
Remove the connections
Open the tray and remove the tray front 70
Remove 4 screws 255
(Basic Engine 1007 frame 100)
Demount the DVDR Basic Engine

FRONT DV Board 1006
Remove screw 200
(board front)
demount the board

Display board 1004
Remove 5 screws 200
(board front)
demount the board

KEY Board 1004
remove 2 screws 200
(board front)
demount the board

REC Key Board 1004
remove 2 screws 200
(board front)
demount the board

FRONT AV Board 1005
remove 2 screws 200
(board front)
demount the board

Manual opening of tray and removal of tray front 70

In case the loader is defective and cannot be opened electrically, you can open the tray as follows:
It is possible to unlock the tray by means of a screwdriver via a slot in the front and frame at the underside.
Push the white pin of the slider at the underside of the basic engine to the right (seen from the front)
Open the unlocked tray.

TR01005_001
090502

Figure 4-14

5. Diagnostic Software

Due to the complexity of the DVD recorder, the time to find a defect in the recorder can become long. To reduce this time, the recorder has been equipped with Diagnostic and Service software (DS). The DS offers functionality to diagnose the DVDR hardware and tests the following:

- Interconnections between components
- Accessibility of components
- Functionality of the audio and video paths

This functionality can be accessed via several interfaces:

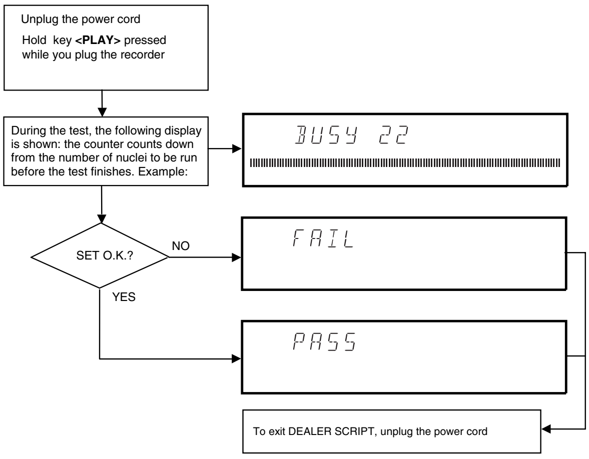
1. End user/Dealer script interface
2. Player script interface
3. Menu and command interface

5.1 End User/Dealer Script Interface

5.1.1 Description

The End user/Dealer script interface gives a diagnosis on a stand alone DVD recorder; no other equipment is needed. During this mode, a number of hardware tests (nuclei) are automatically executed to check if the recorder is faulty. The diagnosis is simply a "fail" or "pass" message. If the message "FAIL" appears on the display, there is apparently a failure in the recorder. If the message "PASS" appears, the nuclei in this mode have been executed successfully. There can be still a failure in the recorder because the nuclei in this mode don't cover the complete functionality of the recorder.

5.1.2 Contents


Unplug the power cord
Hold key <PLAY> pressed while you plug the recorder
During the test, the following display is shown: the counter counts down from the number of nuclei to be run before the test finishes. Example:
BUSY 22
SET O.K.?
NO
YES
FAIL
PASS
To exit DEALER SCRIPT, unplug the power cord

CL 16532095_068.eps
150801

Figure 5-1

The End use/Dealer script executes all diagnostic nuclei that do not need any user interaction and are meaningful on a standalone DVD recorder. The nuclei called in the End user/ Dealer script are the following:

Counter	Nucleus	Name	Description
22	104	HostdSdramWrR	checks all memory locations of the 4MB SDRAM
21	106	HostdDramWrR	checks all the DRAM connected to the microprocessor of the digital board
20	123	HostdI2cNvram	checks the data line (SDA) and the clock line (SCL) of the I2C bus between the host decoder and NVRAM
19	202	SAA7118I2c	checks the interface between the Host I2C controller and the AVENC SAA7118 Video Input Processor
18	200	VideoEncI2c	checks the interface between the host I2C controller and Empress SAA6752
17	207	AudioEncI2c	checks the I2C connection between the host decoder and Empress SAA6752
16	204	AudioEncAccess	tests the HIO8 interface lines between the host decoder and the audio encoder
15	203	AudioEncSramAccess	checks the access of the SRAM by the audio encoder (address and data lines).
14	205	AudioEncSramWrR	tests the SRAM connected to the audio encoder
13	206	AudioEncInterrupt	tests the interrupt line between the host decoder and the audio encoder
12	300	VsmAccess	checks whether the VSM interrupt controllers and DRAM are accessible
11	303	VsmInterrupt	checks both interrupt lines between the VSM and the host decoder
10	302	VsmSdramWrR	tests the entire SDRAM of the VSM
9	1400	Clock11_289MHz	switches the A_CLK of the micro clock to 11.2896 MHz
8	1401	Clock12_288MHz	switches the A_CLK of the micro clock to 12.288 MHz
7	601	BeS2Bengine	checks the S2B interface with the Basic Engine by sending an echo command
6	500	DisplayEcho	checks the interface between the host processor and the slave processor on the display board
5	700	AnalogueEcho	checks the interface between the host processor and the microprocessor on the analogue board
4	711	AnalogueNvram	checks the NVRAM on the analogue board
3	706	AnalogueTuner	checks whether the tuner on the analogue board is accessible
2	901	LoopAudioUserDealer	This nucleus tests the components on the audio signal path The host decoder - The analogue board - The audio encoder - The VSM On the analogue board the audio is internally looped back to the digital board
1	906	LoopVideoUserDealer	Nucleus for testing the components on the video signal system path: - The VIP - The video encoder - The VSM - The host decoder - The analogue board On the analogue the video signal is internally routed back to the digital board.

5.2 Player Script Interface

5.2.1 Description

The Player script will give the opportunity to perform a test that will determine which of the DVD recorder's modules are faulty, to read the error log and to perform an endurance loop test. To successfully perform the tests, the DVD recorder must be connected to a TV set.
To be able to check results of certain nuclei, the player script expects some interaction of the user (i.e. to approve a test picture or a test sound). Some nuclei (e.g. nuclei that test functionality of the DVDR module) require that a DVD+RW disc is inserted.
Only tests within the scope of the diagnostic software will be executed hence only faults within this scope can be detected.

5.2.2 Structure of the Player Script

The player script consists of a set of nuclei testing the hardware modules in the DVD recorder: the Display PWB, the Digital PWB, the Analogue In/Out PWB and the DVDR module. Nuclei run by the player test need some user interaction; in the next table this interaction is described. The player test is done in two phases:

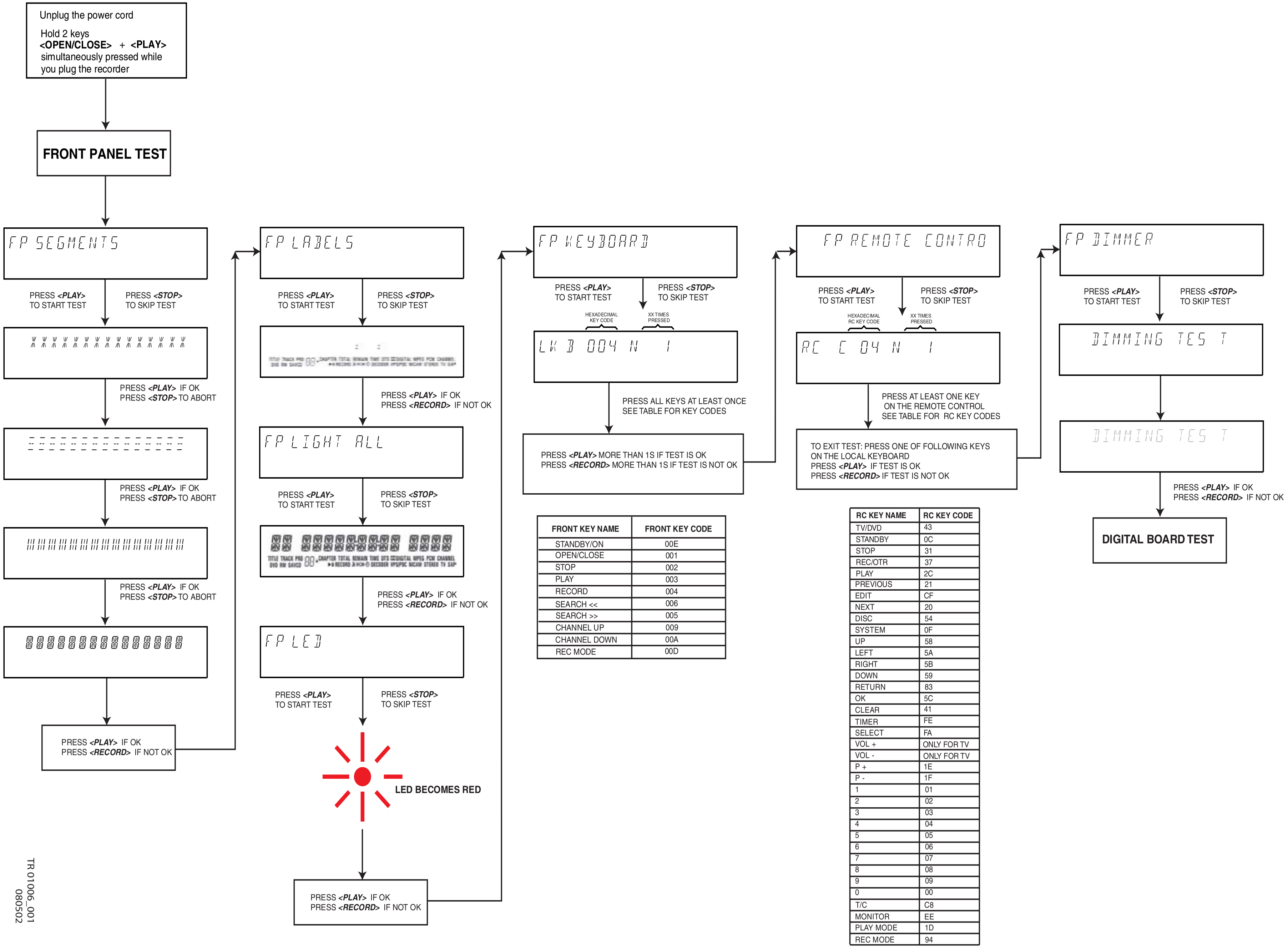
- Interactive tests: this part of the player test depends strongly on user interaction and input to determine nucleus results and to progress through the full test. Reading the error log information can be useful to determine any errors that occurred recently during normal operation of the DVD player.
- The loop test will perform the same nuclei as the dealer test, but it will loop through the list of nuclei indefinitely.

STEP	DESCRIPTION	NUCLEUS
1	Press **OPEN/CLOSE** and **PLAY** at the same time and POWER ON the recorder to start the playerscript	2
2	The local display shows **FPSEGMENTS**. Press **PLAY** to start the test. First the *starburst pattern* is lit, then the *horizontal segments* are lit, followed by the *vertical segments* and the last test is *light all segments* test. After each of the 4 tests the user has to confirm that the correct pattern was lit. Press **PLAY** to confirm that the correct pattern was lit (four times if the FPSEGMENTS test was successful). Press **RECORD** to indicate that the correct pattern was not successfully lit. Press **STOP** to skip this nucleus.	502
3	The local display shows **FPLABELS**. Press **PLAY** to start the test. Press **PLAY** to confirm that all labels are lit. Press **RECORD** to indicate that not all labels are lit. Press **STOP** to skip this nucleus.	503
4	The local display shows **FPLIGHT ALL**. Press **PLAY** to start the test. Press **PLAY** to confirm that everything was lit. Press **RECORD** to indicate that not all patterns are lit. Press **STOP** to skip this nucleus.	520
5	The local display shows **FPLED**. Press **PLAY** to start the test. Press **PLAY** to confirm that the led is lit. Press **RECORD** to indicate that the led is not lit. Press **STOP** to skip this nucleus.	504
6	The local display shows **FPFLAP OPEN**. Press **PLAY** to start the test. Press **PLAY** to confirm that the flap has opened. Press **RECORD** to indicate that the flap did not open. Press **STOP** to skip this nucleus.	522
7	The local display shows **FPKEYBOARD**. Press **PLAY** to start the test. Attention all keys have to be pressed to get a positive result! Press **PLAY** for more than one second to confirm that all the keys were pressed and shown on the local display. If not all the keys were pressed, a FAIL message will appear on the local display. Press **RECORD** for more than one second to indicate that not all keys were pressed and shown on the local display. Press **STOP** for more than one second to skip this nucleus.	505
8	The local display shows **FPREMOTE CONTROL**. Press **PLAY** to start the test. Press **PLAY** to confirm that a key on the remote control was pressed and shown on the local display. Only one key has to be pressed to get a successful result. Press **RECORD** to indicate that the key on the remote control was pressed but not shown on the local display. Press **STOP** to skip this nucleus.	506
9	The local display shows **FPDIMMER**. Press **PLAY** to start the test. Press **PLAY** to confirm that the text on the local display was dimmed. Press **RECORD** to indicate that the text on the local display was not dimmed. Press **STOP** to skip this nucleus.	518
10	The local display shows **FPBEEPER**. Press **PLAY** to start the test. Press **PLAY** to confirm that the beeper on the front panel sounded. Press **RECORD** to indicate that the beeper on the front panel did not sound. Press **STOP** to skip this nucleus.	514
11	The local display shows **FPFLAP CLOSE**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	523
12	The local display shows **ROUTE VIDEO**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	712
13	The local display shows **ROUTE AUDIO**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	713
14	The local display shows **COLOUR-BAR ON**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	120

STEP	DESCRIPTION	NUCLEUS
15	The local display shows **PINK NOISE ON**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	115
16	The local display shows **PINK NOISE OFF**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	116
17	The local display shows **SINE ON**. Press **PLAY** to start the test. Press **STOP** to stop the sine. Press **STOP** to skip this nucleus.	117
18	The local display shows **COLOUR-BAR OFF**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	121
19	The local display shows **BERESET**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	603
20	The local display shows **BETRAY OPEN**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	616
21	The local display shows **BETRAY CLOSE**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	615
22	The local display shows **BEWRITE READ**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	617
23	The local display shows **BETRAY OPEN**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	616
24	The local display shows **BETRAY CLOSE**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus.	615
25	The local display shows **READ ERRORLOG**. Press **PLAY** to start the test. Press **STOP** to skip this nucleus. If the player test succeeded, the user/dealer script will start in an endless loop. If the player test failed, the local display will display FAIL and the error code	633

Remark

In case of failure, the display shows " FAIL XXXXXX ". The description of the shown error code can be retrieved in the survey of Nuclei Error Codes (paragraph 5.4). Once an error occurs, it is not possible to continue the player script. Unplug the set and restart the player script. By pressing the STOP key, it is possible to jump over the failure and to continue the player script.


Unplug the power cord
Hold 2 keys <OPEN/CLOSE> + <PLAY> simultaneously pressed while you plug the recorder
FRONT PANEL TEST
FP SEGMENTS
PRESS <PLAY> TO START TEST
PRESS <STOP> TO SKIP TEST
PRESS <PLAY> IF OK
PRESS <STOP> TO ABORT
PRESS <PLAY> IF OK
PRESS <STOP> TO ABORT
PRESS <PLAY> IF OK
PRESS <STOP> TO ABORT
PRESS <PLAY> IF OK
PRESS <RECORD> IF NOT OK
FP LABELS
PRESS <PLAY> TO START TEST
PRESS <STOP> TO SKIP TEST
PRESS <PLAY> IF OK
PRESS <RECORD> IF NOT OK
FP LIGHT ALL
PRESS <PLAY> TO START TEST
PRESS <STOP> TO SKIP TEST
PRESS <PLAY> IF OK
PRESS <RECORD> IF NOT OK
FP LED
PRESS <PLAY> TO START TEST
PRESS <STOP> TO SKIP TEST
LED BECOMES RED
PRESS <PLAY> IF OK
PRESS <RECORD> IF NOT OK
FP KEYBOARD
PRESS <PLAY> TO START TEST
PRESS <STOP> TO SKIP TEST
HEXADECIMAL KEY CODE
XX TIMES PRESSED
LK B 004 N 1
PRESS ALL KEYS AT LEAST ONCE
SEE TABLE FOR KEY CODES
PRESS <PLAY> MORE THAN 1S IF TEST IS OK
PRESS <RECORD> MORE THAN 1S IF TEST IS NOT OK
FP REMOTE CONTRO
PRESS <PLAY> TO START TEST
PRESS <STOP> TO SKIP TEST
HEXADECIMAL RC KEY CODE
XX TIMES PRESSED
RC C 04 N 1
PRESS AT LEAST ONE KEY
ON THE REMOTE CONTROL
SEE TABLE FOR RC KEY CODES
TO EXIT TEST: PRESS ONE OF FOLLOWING KEYS
ON THE LOCAL KEYBOARD
PRESS <PLAY> IF TEST IS OK
PRESS <RECORD> IF TEST IS NOT OK
FP DIMMER
PRESS <PLAY> TO START TEST
PRESS <STOP> TO SKIP TEST
DIMMING TES T
DIMMING TES T
PRESS <PLAY> IF OK
PRESS <RECORD> IF NOT OK
DIGITAL BOARD TEST
TR 01006_001
080502

FRONT KEY NAME	FRONT KEY CODE
STANDBY/ON	00E
OPEN/CLOSE	001
STOP	002
PLAY	003
RECORD	004
SEARCH <<	006
SEARCH >>	005
CHANNEL UP	009
CHANNEL DOWN	00A
REC MODE	00D

RC KEY NAME	RC KEY CODE
TV/DVD	43
STANDBY	0C
STOP	31
REC/OTR	37
PLAY	2C
PREVIOUS	21
EDIT	CF
NEXT	20
DISC	54
SYSTEM	0F
UP	58
LEFT	5A
RIGHT	5B
DOWN	59
RETURN	83
OK	5C
CLEAR	41
TIMER	FE
SELECT	FA
VOL +	ONLY FOR TV
VOL -	ONLY FOR TV
P +	1E
P -	1F
1	01
2	02
3	03
4	04
5	05
6	06
7	07
8	08
9	09
0	00
T/C	C8
MONITOR	EE
PLAY MODE	1D
REC MODE	94

Figure 5-2

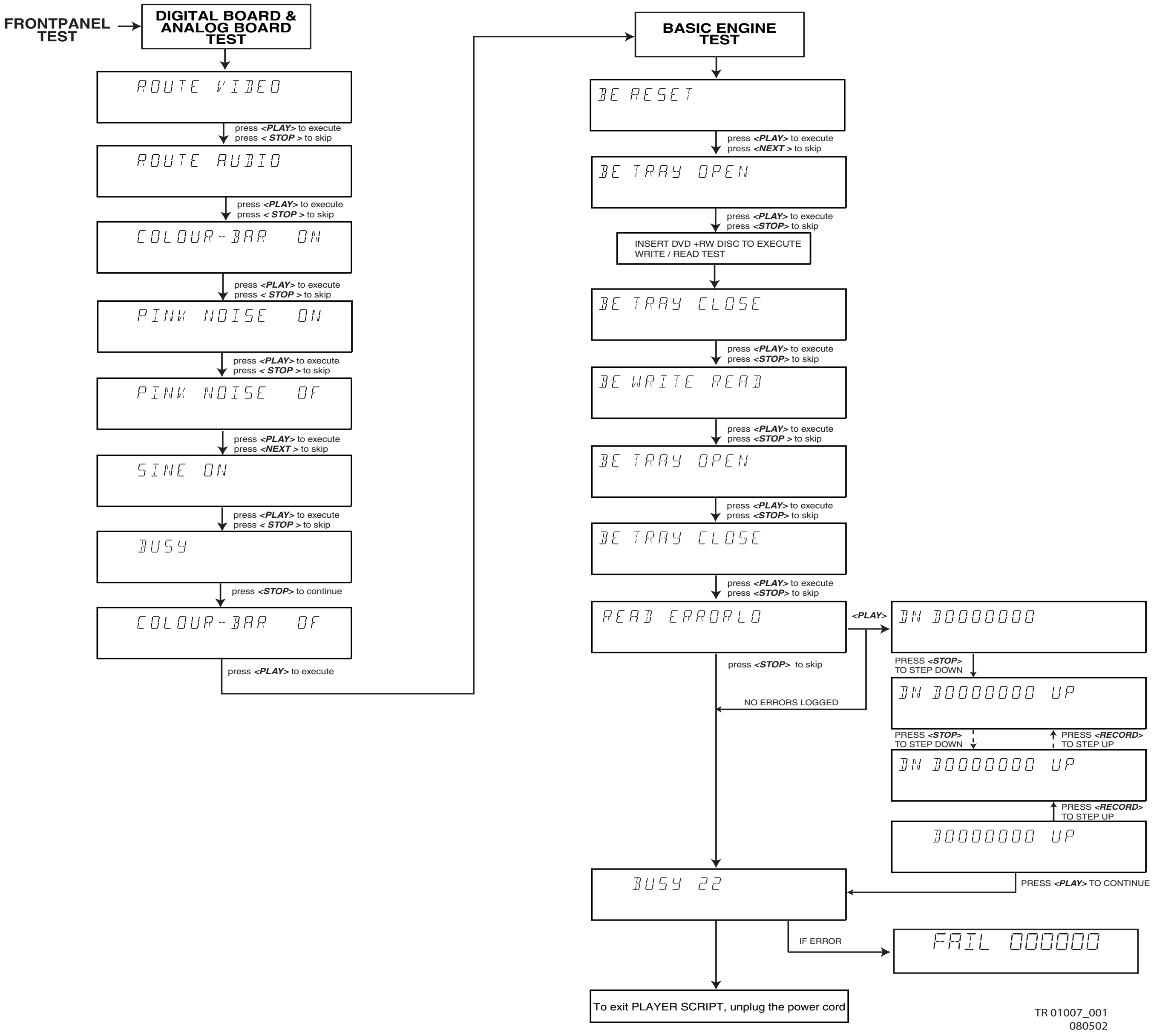
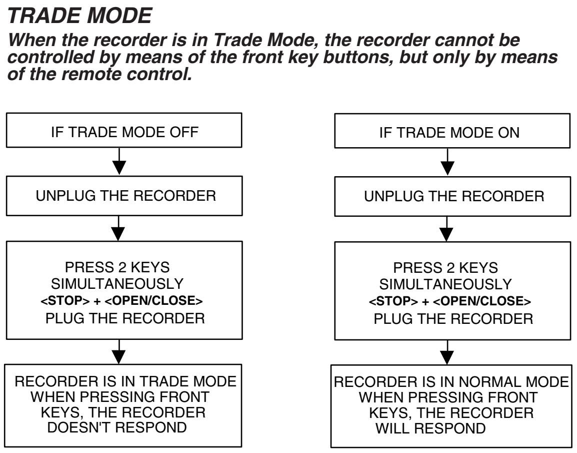

FRONTPANEL TEST
DIGITAL BOARD & ANALOG BOARD TEST
ROUTE VIDEO
press <PLAY> to execute
press < STOP > to skip
ROUTE AUDIO
press <PLAY> to execute
press < STOP > to skip
COLOUR-BAR ON
press <PLAY> to execute
press < STOP > to skip
PINK NOISE ON
press <PLAY> to execute
press < STOP > to skip
PINK NOISE OF
press <PLAY> to execute
press <NEXT > to skip
SINE ON
press <PLAY> to execute
press < STOP > to skip
BUSY
press <STOP> to continue
COLOUR-BAR OF
press <PLAY> to execute
BASIC ENGINE TEST
BE RESET
press <PLAY> to execute
press <NEXT > to skip
BE TRAY OPEN
press <PLAY> to execute
press <STOP> to skip
INSERT DVD +RW DISC TO EXECUTE WRITE / READ TEST
BE TRAY CLOSE
press <PLAY> to execute
press <STOP> to skip
BE WRITE READ
press <PLAY> to execute
press <STOP > to skip
BE TRAY OPEN
press <PLAY> to execute
press <STOP> to skip
BE TRAY CLOSE
press <PLAY> to execute
press <STOP> to skip
READ ERRORLO
<PLAY>
DN D0000000
PRESS <STOP> TO STEP DOWN
press <STOP> to skip
NO ERRORS LOGGED
DN D0000000 UP
PRESS <STOP> TO STEP DOWN
PRESS <RECORD> TO STEP UP
DN D0000000 UP
PRESS <RECORD> TO STEP UP
D0000000 UP
PRESS <PLAY> TO CONTINUE
BUSY 22
IF ERROR
FAIL 000000
To exit PLAYER SCRIPT, unplug the power cord
TR 01007_001
080502

Figure 5-3

5.2.3 Error Log

Explanation:
The application errors will be logged in the NVRAM. The maximum number of error bytes that will be visible is 19. The last reported error is shown as DN D0000000, the oldest visible error as D0000000 UP and the errors in between as DN D0000000 UP. DN stands for DOWN, UP stands for UPWARDS. The shown D error codes are identical to the Nuclei Error Codes (paragraph 5.4).

5.2.4 Trade Mode


TRADE MODE
When the recorder is in Trade Mode, the recorder cannot be controlled by means of the front key buttons, but only by means of the remote control.
IF TRADE MODE OFF
UNPLUG THE RECORDER
PRESS 2 KEYS SIMULTANEOUSLY <STOP> + <OPEN/CLOSE> PLUG THE RECORDER
RECORDER IS IN TRADE MODE WHEN PRESSING FRONT KEYS, THE RECORDER DOESN'T RESPOND
IF TRADE MODE ON
UNPLUG THE RECORDER
PRESS 2 KEYS SIMULTANEOUSLY <STOP> + <OPEN/CLOSE> PLUG THE RECORDER
RECORDER IS IN NORMAL MODE WHEN PRESSING FRONT KEYS, THE RECORDER WILL RESPOND

CL 16532095_071.eps
150801

Figure 5-4

5.2.5 Virgin mode

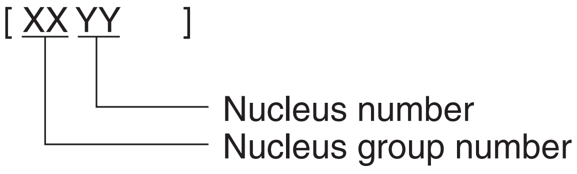
If you want that the recorder starts up in Virgin mode, follow this procedure:

- Unplug the recorder
- plug the recorder again while you keep the STAND BY/ON key pressed
- the set starts up in Virgin mode.

5.3 Menu and Command Mode Interface

5.3.1 Nuclei Numeration

Each nucleus has a unique number of four digits. This number is the input of the command mode.


[XX YY]
Nucleus number
Nucleus group number

CL 06532152_012.eps
051200

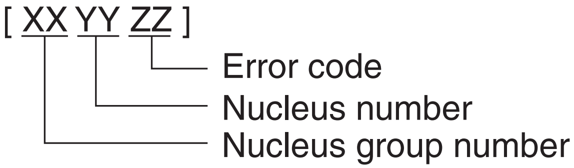
Figure 5-5

The following groups are defined:

Group number	Group name
0	Basic / Scripts
1	Host decoder (Sti5505 and memory)
2	Audio / video encoder (DVDR only)
3	VSM (DVDR only)
4	NVRAM
5	Front Panel
6	Basic Engine
7	Analogue board (DVDR only)
8	DVIO (DVDR only)
9	Loop nuclei (DVDR only)
10	Library sub nuclei (I2C nuclei)
11	User interface
12	Furore (SACD only)
13	DAC (SACD only)
14	Miscellaneous

5.3.2 Error Handling

Each nucleus returns an error code. This code contains six numerals, which means:


[XX YY ZZ]
Error code
Nucleus number
Nucleus group number

CL 06532152_013.eps
051200

Figure 5-6

The nucleus group numbers and nucleus numbers are the same as above.

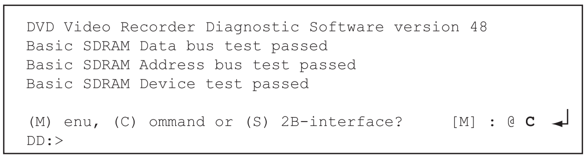
5.3.3 Command Mode Interface

Set-Up Physical Interface Components
Hardware required:

- Service PC
- one free COM port on the Service PC
- special cable to connect DVD recorder to Service PC

The service PC must have a terminal emulation program (e.g. OS2 WarpTerminal or Procomm) installed and must have a free COM port (e.g. COM1). Activate the terminal emulation program and check that the port settings for the free COM port are: 19200 bps, 8 data bits, no parity, 1 stop bit and no flow control. The free COM port must be connected via a special cable to the RS232 port of the DVD recorder. This special cable will also connect the test pin, which is available on the connector, to ground (i.e. activate test pin).
Code number of PC interface cable: 3122 785 90017

Activation
Plug the recorder to the mains and the following text will appear on the screen of the terminal (program):



```
DVD Video Recorder Diagnostic Software version 48
Basic SDRAM Data bus test passed
Basic SDRAM Address bus test passed
Basic SDRAM Device test passed

(M) enu, (C) ommand or (S) 2B-interface?     [M] : @ C ↵
DD:>
```

CL 16532095_073.eps
150801

Figure 5-7

The first line indicates that the Diagnostic software has been activated and contains the version number. The next lines are the successful result of the SDRAM interconnection test and the basic SDRAM test. The last line allows the user to choose between the three possible interface forms. If pressing C has made a choice for Command Interface, the prompt ("DD>") will appear. The diagnostic software is now ready to receive commands. The commands that can be given are the numbers of the nuclei.

Command Overview

We provide an overview of the nuclei and their numbers. This overview is preliminary and subject to modifications.

Host Decoder [01]

[xx yy] Number	Nuclei
100	Checksum Flash
101	Flash Write Access 1
102	Flash Write Access 2
103	Flash Write Read
104	SdRam Write Read
105	SdRam Write Read Fast
106	Dram Write Read
107	Dram Write Read Fast
108	Hardware Version
109	Mute On
110	Mute Off
115	Pink Noise On
116	Pink Noise Off
117	Sine On
118	Sine Burst 1kHz
119	Sine Burst 12kHz
120	Colour-bar On Note: Use nuclus 712 with parameter 07 to route the signals to the analogue board output
121	Colour-bar Off
122	NvramWrR
123	NvramI2c
130	Boot Version
131	Application Version
132	Diagnostics Version
133	Download Version
134	Write / read I2C message to / from digital board
135	Video Test Signal OnNote: Use nuclus 712 with parameter 07 to route the signals to the analogue board output. Input: 135 [a] [b] a: Number of test image, 0. Horizontal colour-bar 1. White 2. Yellow 3. Light blue 4. Green 5. Magenta 6. Red 7. Blue 8. Black 9. Colour triangle (execution time is 12 seconds) 10. Test image for progressive scan (execution time is 6 seconds) b: Video standard, 0. PAL BDGHI 1. NTSC
136	Video Test Signal Off
137	Macrovision Off

Audio Video Decoder [02]

[xx yy] Number	Nuclei
200	Video Encoder I2C
202	SAA7118 I2C
203	Audio Encoder SRAM Access
204	Audio Encoder Access
205	Audio Encoder SRAM Write Read
206	Audio Encoder Interrupts
207	Audio Encoder I2C
208	SAA7118 select input
209	Empress Version

VSM [03]

[xx yy] Number	Nuclei
300	Register Access
301	SDRAM Access
302	SDRAM Write Read
303	Interrupt lines
304	VSM Interconnection
305	UART

NVRAM [04]

[xx yy] Number	Nuclei
400	Reset
401	Read
402	Modify
403	UniqueNr Read
404	Read Error Log
407	Reset Error Log
409	Line2 Region-Code Reset
410	UniqueNr Store

Front Panel [05]

[xx yy] Number	Nuclei
500	Echo
501	Version
502	Segment
503	Label
504	Led
505	Keyboard
506	Remote-Control
507	Segment Starburst
508	Segment Vertical
509	Segment Horizontal
514	Beeper
515	Discbar
516	Discbar Dots
517	Vu / Grid
518	Dimmer
519	Blinking
520	Light All Segments
522	Flap Open
523	Flap Close

Basic Engine [06]

[xx yy] Number	Nuclei
600	S2B Pass
601	S2B Echo
602	Version
603	Reset
604	Focus On
605	Focus Off
606	Disc Motor On
607	Disc Motor Off
608	Radial On

[xx yy] Number	Nuclei
609	Radial Off
615	Tray In
616	Tray Out
617	Write Read
618	Write Read Endless Loop
619	Selftest
620	BE Test
621	Laser Test
622	Spindle (Disc) Motor Test
623	Focus Test
624	Sledge Motor Test
625	Sledge Motor Slow
626	Tilt
627	EEPROM Read
628	EEPROM Write
629	Optimise Jitter
630	Radial ATLS Calibration
631	Get Statistics Information
632	Reset Statistics Information
633	BE Read Error Log
634	BE Reset Error Log
638	Get Self Test Result
639	Radial Initialisation
640	Get OPU info

Analog Board [07]

[xx yy] Number	Nuclei
700	Echo
703	Boot Version
704	Hardware Version
705	Clock Adjust
706	Tuner
707	Frequency Download
708	Data Slicer
709	Sound Processor
710	AV Selector
711	Nvram
712	Route Video
713	Route Audio
715	Set Slash Version
716	Application Version
717	Diagnostics Version
718	Download Version
720	Bargraph Level Adjustment
721	Clock correction
722	Clock reference
723	Re-virginise Recorder
724	Flash Checksum
725	Tuner frequency selection Europe: To make video and audio signals from the tuner available on Scart2, send command "712 08". For Nafta/Apac: To make the black/white Video available on Y/C Rear Out connector, send command “712 08” Input: 725 [frequency in MHz*16] [system] System: NTSC=16, PAL BG=16, PAL I=32, PAL DK=48, SEC L=64, SEC LS=80, SEC BG=96, SEC DK=112
727	Set virgin bit
728	Clear Virgin Bit
729	Write / read I2C message to / from analogue board
730	Store external presets
731	Get slash version
732	AFC Reference Voltage Tuner

DVIO [08]

[xx yy] Number	Nuclei
800	Check DVIO board presence
801	Reset DVIO
802	DVIO Access
803	Get DVIO error codes
804	Get DVIO module Ids
805	Execute DVIO module SelfTestInput: 805 [a] [b]Parameters: a=1/0…full Ram test, b=1/0…cable connected
806	Set DVIO led on.
807	Set DVIO led off.

Loop Nuclei [09]

[xx yy] Number	Nuclei
900	Digital Audio Loop(no function in Gen. 1.5 and Lead)
901	User / Dealer Audio Loop
902	Digital Video Loop
903	Digital Video VBI Loop
904	System Video Loop
905	System Video VBI Loop
906	User / Dealer Video Loop
907	User / Dealer Video VBI Loop
908	System Audio Loop SCART
909	System Audio Loop CINCH
910	Digital DVIO Video Loop
911	System Video Vip

Miscellanious [14]

[xx yy] Number	Nuclei
1400	Clock 11.289 MHz
1401	Clock 12.288 MHz
1412	Progressive Scan I2C
1413	Progressive Scan test image on
1414	Progressive Scan test image off
1415	Progressive Scan Route Enable
1416	Progressive Scan Route Disable

Scripts [00]

[xx yy] Number	Nuclei
1	UserDealer Script
2	Player Script

Routing Audio and Video

Route Video
Nucleus Number: 712
Description
This nucleus routes the video signals on the analogue board to the destination determined by the input parameters

The paths that are available for video routing and their description(Europe version):

Path ID	Description
00	Input signal is VIDEO(CVBS) from digital board and will be re-routed back to the digital board.
01	Input signal is from FRONT VIDEO(CVBS) IN and will be routed to the digital board.
02	No Routing.
03	Input signal is from FRONT S-VIDEO(Y/C) and will be routed to the digital board.
04	No Routing.
05	Input signal is CVBS from SCART1 and will be routed to the digital board.
06	Input signal is CVBS from SCART2 and will be routed to the digital board.
07	Input Signal is CVBS from Digital Board and it will be routed to Scart1 and Scart2.
08	Input signal is VIDEO(CVBS) from ANTENNA IN and will be routed to SCART2.
09	Input signal is VIDEO(CVBS) from SCART1 and will be routed to SCART2.
10	Input signal is VIDEO(CVBS) from SCART2 and will be routed to SCART1.
11	Signal path is routed Fast Blank from Scart2 pin16 and will be routed Scart1 pin16
12	Input Signal is YC from Digital Board and it will be routed to Scart1.
13	No Routing.
14	No Routing.
15	Input Signal is CVBS from TUNER and it will be routed to Digital .
16	No Routing.
17	Input Signal is routed from digital board YC to REAR S-VIDEO(YC) OUT
18	Signal path is routed from digital board RGB to RGB SCART1 and from digital board CVBS to digital board CVBS.
19	No Routing.
20	Input RGB Signal is routed from Digital Board to SCART1(RGB),Input CVBS Signal from Digital Board to Digital Board and Fast Blanking Signal from Scart 2 to Scart1.
21	Input Y/C Signal from Digital Board is routed to Rear Y/C Connector and Input Y/c Signal from Front Y/C connector is routed to Digital Board.

The paths that are available for video routing and their description (Nafta region):

PATH ID	DESCRIPTION
00	Input signal is VIDEO(CVBS) from digital board and will be re-routed back to the digital board.A Cinch Cable need to be connected from Rear Cinch Out to Front Cinch In for this Test.(Direct routing on analogue board from YUV In to YUV Out is not Possible)
01	Input signal is from FRONT VIDEO(CVBS) IN and will be routed to the digital board.This routing is same as the above path id.
02	Input signal is from REAR VIDEO(CVBS) IN and will be routed to the digital board.
03	Input signal is from FRONT S-VIDEO(Y/C) IN and the signal received will be routed to the digital board.
04	Input signal is from REAR S-VIDEO(Y/C) IN and will be routed to the digital board.
05	No Routing.
06	No Routing.
07	No Routing.
08	Input signal is VIDEO(CVBS) from TUNER and will be routed to Y Pin of Rear Y/C Connector.This will give only black/White Picture .
09	Input signal is from YUV IN and will be routed to YUV OUT.This is possible only if Digital Board routes back YUV signal received back to the Analogue board(DENC)
10	No Routing.
11	No Routing.
12	No Routing.
13	No Routing.
14	No Routing
15	Input CVBS Signal from Tuner is routed to Digital Board..
16	No Routing
17	Input RGB Signal is routed from Digital Board to RGB Rear Out and Input CVBS Signal is routed from Rear Cinch In 1 to Digital Board(This second step is for routing Input CVBS Signal from Digital Board to Digital Board again - A Cinch cable need to be connected from Rear Cinch Out1 to Rear Cinch In 1)
18	Input Signal from CVBS Rear In is routed to Digital Board.This is same as path id 02.
19	Input Y/C signal from Digital Board is routed to Y/C Rear Out Connector and Input signal from Y/C Rear In Connector is routed to Y/C Digital Board.

23	The Video signal received from the Digital board will be outputted on Modulator channel 3. Please use command 120 for testing Video because Nuclei 120 will generate the Colour Bar signal on the digital Board.
24	The Audio signal received from the Digital board will be outputted on Modulator channel 4. Please use command 120 for testing Video because Nuclei 120 will generate the Colour Bar signal on the digital Board.

Example
DD:> 712 01
71200: Video routing on the Analogue Board OK.
Test OK @

Route Audio

Nucleus Number: 713

Description
This nucleus routes the audio on the analogue board to the destination determined by the input parameters
The paths that are available for audio routing and their description (Europe version)

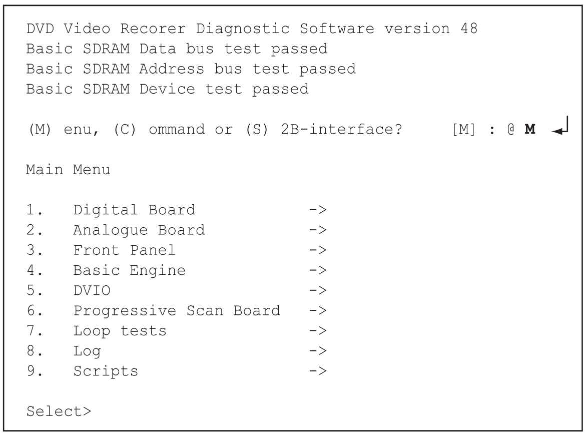
PATH ID	DESCRIPTION
00	No Routing.
01	Input signal is from FRONT AUDIO IN and will be routed to the digital board.
02	Input signal is from REAR AUDIO IN 2 and will be routed to the digital board.
03	Input Audio Signal is routed from FRONT Cinch In to Digital Board.(This is same as path id 01)
04	Input Signal is from Rear Cinch In1 and it will be routed to Digital Board..
05	No routing.
06	No routing.
07	No routing.
08	No Routing.
09	No routing.
10	No Routing.
11	No Routing.
12	No Routing.
13	Input Signal is from Digital Board and it will be routed to the digital board.
14	No routing.
15	Input is Audio Signal from TUNER and it will be routed to Digital Board.
16	Input signal is AUDIO from dvio board and will be routed to Digital Board.
17	No routing.
18	No routing.
19	No routing.
20	Input signal is from REAR AUDIO IN 2 and will be routed to the digital board.
21	Input signal is from REAR AUDIO IN 1 and will be routed to the digital board.
22	Input signal is from REAR AUDIO IN 1 and will be routed to the digital board.
23	The Audio signal received from the Digital board will be outputted on Modulator channel 3. Please use command 117 for testing audio because Nuclei 117 will generate the Audio signal on the digital Board.
24	The Audio signal received from the Digital board will be outputted on Modulator channel 4. Please use command 117 for testing audio because Nuclei 117 will generate the Audio signal on the digital Board.

EXAMPLE
DD:> 713 00
71300: Audio routing on the Analogue Board OK.
Test OK @

5.3.4 Menu Mode Interdace

Activation

Plug the recorder to the mains and the following text will appear on the screen of the terminal (program):



```
DVD Video Recorer Diagnostic Software version 48
Basic SDRAM Data bus test passed
Basic SDRAM Address bus test passed
Basic SDRAM Device test passed

(M) enu, (C) ommand or (S) 2B-interface?     [M] : @ M ↵

Main Menu

1.   Digital Board            ->
2.   Analogue Board           ->
3.   Front Panel              ->
4.   Basic Engine             ->
5.   DVIO                     ->
6.   Progressive Scan Board   ->
7.   Loop tests               ->
8.   Log                      ->
9.   Scripts                  ->

Select>
```

Figure 5-8

The first line indicates that the Diagnostic software has been activated and contains the version number. The next lines are the successful result of the SDRAM interconnection test and the basic SDRAM test. The last line allows the user to choose between the three possible interface forms. If pressing M has made a choice for Menu Interface, the Main Menu will appear.

Menu Structure

The following menu structure is given after starting up the DVD recorder in menu mode. The symbol -> indicates that the current menu choice will invoke the display of a submenu.

Main Menu
1.Digital Board ->
2.Analogue Board ->
3.Front Panel ->
4.Basic Engine ->
5.DVIO ->
6.Progressive Scan Board ->
7.Loop Tests ->
8.Log ->
9.Scripts ->

Digital Board Menu
1.Host Decoder ->
2.VSM ->
3.AVENC ->
4.NVRAM ->

Host Decoder Menu
1.Flash Checksum
2.Flash1 Write Access
3.Flash2 Write Access
4.Flash Write/Read
5.Host SDRAM Write/Read
6.Host SDRAM Fast Write/Read
7.Host DRAM Write/Read
8.Host DRAM Fast Write/Read
9.I2C NVRAM
10.NVRAM Write/Read
11.Engine S2B Echo
12.Versions ->
13.Audio Mute ->
14.Colourbar ->
15.Pink Noise ->
16.Sine Generate ->

Digital Board Versions Menu
1.Hardware Version
2.Bootcode version
3.Applications Version
4.Diagnostics Version
5.Download Version

Audio Mute Menu
1.Audio Mute On
2.Audio Mute Off

Colourbar Menu
1.Colourbar On
2.Colourbar Off

Pink Noise Menu
1.Pink Noise On
2.Pink Noise Off

Sine Generate Menu
1.Sine On
2.Sine Burst 1kHz
3.Sine Burst 12kHz

VSM Menu
1.Register Access
2.SDRAM Access
3.VSM SDRAM Write/Read
4.Interrupt Lines
5.VSM Interconnection
6.UART

AVENC Menu
1.Empress ->
2.Video Input Processors ->

Empress Menu
1.Version number

Video Input Processors Menu
1.SAA7118 I2C Access

NVRAM Menu
1.Read Error Log
2.Reset Error Log
3.Read DVIO Unique ID

Analogue Board Menu
1.Echo
2.Obsolete
3.Route Video Input back to Digital board
4.Route Audio Input back to Digital board
5.Flash Checksum
6.Versions ->
7.Components ->
8.Re-virginize Recorder ->

Analogue Board Versions Menu
1.Hardware Version
2.Bootcode version
3.Application version
4.Diagnostics version
5.Download version

Analogue Components Menu
1.Tuner
2.Data Slicer
3.Sound Processor
4.AV Selector
5.NVRAM

Analogue Board Re-virginize Menu
1.Re-virginize Recorder
2.Set Virgin-bit
3.Clear Virgin-bit
4.Store external presets

Front Panel Menu
1.Echo
2.Version
3.Flap Control ->
4.Segment Test ->
5.Light Labels
6.Led test
7.Keyboard test
8.Remote Control
9.Beep
10.Disc Bar
11.Disc Bar Dots
12.Vu Grid
13.Dimmer
14.Blink
15.Light All Segments

Flap Control Menu
1.Open Flap
2.Close Flap

Segment Test Menu
1.Starburst
2.Light Horizontal Segments
3.Light Vertical Segments
4.Light All Segments

Basic Engine Menu
1.Reset
2.S2B Pass-through
3.S2B Echo
4.Focus On
5.Focus Off
6.Version
7.Self Test
8.Get Self Test Result
9.Basic Engine Test
10.Laser Test
11.Focus Test
12.Tilt Test
13.Optimise Jitter
14.Statistics Info
15.Log ->
16.Spindle Motor ->
17.Radial ->
18.Sledge ->
19.Tray ->

Basic Engine Error Log
1.Read Error Log
2.Reset Error Log

Basic Engine Spindle Motor Menu
1.Spindle Motor On
2.Spindle Motor Off
3.Spindle Motor Test

Basic Engine Radial Menu
1.Radial On
2.Radial Off
3.Radial Initialisation
4.Radial ATLS Calibration

Basic Engine Sledge Menu
1.Sledge test
2.Sledge test slow

Basic Engine Tray Menu
1.Tray In
2.Tray Out

DVIO Menu
1.Check Presence
2.Reset
3.Access
4.Error Codes
5.Module Identifiers
6.Led ->

DVIO Led Menu
1.Led On
2.Led Off

Progressive Scan Board Menu
1.I2C Access
2.Test Image On
3.Test Image Off

Loop Tests Menu
1.Digital Board Loops ->
2.User/Dealer Loops ->
3.System Loops ->
4.Basic Engine Loops ->

Digital Board Loops Menu
1.Obsolete
2.Digital Video Loop
3.Digital Video Loop VBI

User/Dealer Loops Menu
1.User/Dealer Audio Loop
2.User/Dealer Video Loop
3.User/Dealer Video Loop VBI

System Loops Menu
1.System Video Loop
2.System Video Loop VBI
3.System Audio Loop SCART(EURO)
4.System Audio Loop CINCH (NAFTA)

Basic Engine Loops Menu
1.Basic Engine write read
2.Basic Engine write read endless loop

Log Menu
1.Read Error Log
2.Reset Error Log

Script Menu
1.User/Dealer Script
2.Player Script

5.4 Nuclei Error Codes

In the following table the error codes will be described.

Error Nr	Error String
10000	"Checksum is OK"
10001	"segment name Checksum doesn't match" or "segment name segment not found"
10100	""
10101	"FLASH 1 Write access test failed"
10200	""
10201	"FLASH 2 Write access test failed"
10300	""
10301	"FLASH write test failed"
10302	"FLASH write command failed"
10303	"FLASH write test done max. number of times"
10400	""
10401	"HostDec SDRAM Memory data bus test goes wrong."
10402	" HostDec SDRAM Memory address bus test goes wrong."
10403	" HostDec SDRAM Physical memory device test goes wrong."
10500	""
10501	" HostDec SDRAM Memory data bus test goes wrong."
10502	" HostDec SDRAM Memory address bus test goes wrong."
10503	" HostDec SDRAM Physical memory device test goes wrong."
10600	""
10601	"HostDec DRAM Memory data bus test goes wrong."
10602	"HostDec DRAM Memory address bus test goes wrong."
10603	"HostDec DRAM Physical memory device test goes wrong."
10700	""
10701	"HostDec DRAM Memory data bus test goes wrong."
10702	"HostDec DRAM Memory address bus test goes wrong."
10703	"HostDec DRAM Physical memory device test goes wrong."

Error Nr	Error String
10800	"Host Decoder version(cut) number: version number""Digital hardware version"
10801	"Can not find version in FLASH."
10900	""
10901	"Error muting audio"
11000	""
11001	"Error demuting audio"
11500	""
11501	"Init of I2C failed"
11502	"The selection of the clock source failed"
11504	"The demute of the audio failed"
11600	""
11601	"Init of I2C failed"
11602	"The mute of the audio failed"
11700	""
11701	"Init of I2C failed"
11702	"The muting of the audio failed"
11703	"The demute of the audio failed"
11704	"The selection of the clock source failed"
11707	"Setup of Front panel failed"
11708	"Sine on Front panel keyboard failed"
11800	""
11801	"Init of I2C failed"
11802	"The muting of the audio failed"
11803	"The demute of the audio failed"
11804	"The selection of the clock source failed"
11805	"Error cannot start VSM audio in port"
11900	""
11901	"Init of I2C failed"
11902	"The muting of the audio failed"
11903	"The demute of the audio failed"
11904	"The selection of the clock source failed"
11905	"Error cannot start VSM audio in port"
12000	""
12001	"Invalid input
12100	""
12200	""
12201	"I2C bus busy before start"
12202	"NVRAM access time-out"
12203	"No NVRAM acknowledge"
12204	"NVRAM time-out"
12205	"NVRAM Write/Read back failed"
12300	""
12301	"I2C bus busy before start"
12302	"NVRAM read access time-out"
12303	"No NVRAM read acknowledge"
12304	"NVRAM read failed"
13000	"Bootcode application version : bootversion"
13001	"Can not find version in FLASH."
13100	"Recorder application version : recorderversion"
13101	"Can not find version in FLASH."
13200	"Diagnostics application version : diagversion"
13201	"Can not find version in FLASH."
13300	"Download application version : downloadversion"
13301	"Can not find version in FLASH."
13700	""
13701	"Turning off MacroVision failed"
20000	""
20001	"I2C bus busy before start"
20002	"Video Encoder access time-out"
20003	"No acknowledge from Video Encoder"
20004	"No data send/received to or from Video Encoder"
20005	"SAA7118 VIP can not be initialised"
20200	""
20201	"I2C bus busy before start"
20202	"SAA7118 VIP access time-out"
20203	"No acknowledge from SAA7118 VIP"
20204	"No data received from SAA7118 VIP"
20300	""
20301	"Error audio encoder SRAM access cannot initialise I2C"
20302	"Error audio encoder SRAM access cannot reset DSP through I2C"
20303	"Error audio encoder SRAM access cannot download boot"
20304	"Error audio encoder cannot download test code"
20305	"Error audio encoder cannot obtain result of test"
20306	"Error audio encoder SRAM access stuck-at-zero data line "
20307	"Error audio encoder SRAM access stuck-at-one data line "
20308	"Error audio encoder SRAM access stuck-at-one address line "
20309	"Error audio encoder SRAM access address line address line x is connected to data line data line y"
20310	"Error audio encoder SRAM access address lines address line x and address line y are connected "
20311	"Error audio encoder SRAM access data lines data line x and data line y are connected "
20312	"Error audio encoder SRAM access illegal data received"
20400	""
20401	"Error audio encoder access cannot initialise I2C"
20402	"Error audio encoder access cannot reset DSP through I2C"
20403	"Error audio encoder accessing ICR register"
20404	"Error audio encoder access stuck-at-zero of data line "
20405	"Error audio encoder access stuck-at-one of data line "
20406	"Audio encoder access data lines data line x and data line y are interconnected "
20500	""
20501	"Error audio encoder SRAM WRR cannot initialise I2C"
20502	"Error audio encoder SRAM WRR cannot reset DSP through I2C"
20503	"Error audio encoder WRR cannot download boot"
20504	"Error audio encoder cannot download test code"
20505	"Error audio encoder SRAM WRR cannot obtain result of test"
20506	"Error audio encoder WRR SRAM stuck-at-zero data bit "
20507	"Error audio encoder WRR SRAM stuck-at-one data bit "
20508	"Error audio encoder WRR SRAM data lines data line x and data line y are connected"
20509	"Error audio encoder WRR SRAM illegal data received"
20600	""
20601	"Error audio encoder interrupt cannot initialise I2C"
20602	"Error audio encoder interrupt cannot reset DSP through I2C"
20603	"Error audio encoder cannot download test code"
20604	"Error occurred accessing VSM"
20605	"Audio encoder interrupt not received"

Error Nr	Error String
20606	"Error occurred while activating the encoder"
20607	"Error audio encoder interrupt cannot initialise empress"
20608	"Error occurred while getting interrupt reason"
20700	""
20701	"Error audio encoder I2C cannot reset DSP through I2C"
20702	"Error audio encoder cannot download boot"
20703	"Error audio encoder cannot download TEST code"
20704	"Error audio encoder I2C bus busy"
20705	"Error audio encoder I2C cannot write slave adress"
20706	"Error audio encoder I2C no acknowledge received"
20707	"Error audio encoder I2C cannot send/receive data"
20708	"Error audio encoder received data through I2C was invalid"
20800	""
20801	"I2C access failed."
20802	"SAA7118 VIP can not be initialised."
20803	"Invalid input"
20900	"B1.B2. B3.B4. B5.B6. B7.B8. B9.B10. B11.B12."
20901	"Firmware download of EMPRESS failed"
20902	"I2C bus busy before start"
20903	"EMPRESS access time-out"
20904	"No acknowledge from the EMPRESS"
20905	"No data send to the EMPRESS"
20906	"No data received from the EMPRESS"
30000	""
30001	"VSM SDRAM Bank1 Memory databus test goes wrong."
30002	"VSM SDRAM Bank1 Memory addressbus test goes wrong."
30003	"VSM SDRAM Bank1 Physical memory device test goes wrong."
30004	" VSM SDRAM Bank2 Memory databus test goes wrong."
30005	" VSM SDRAM Bank2 Memory addressbus test goes wrong."
30006	" VSM SDRAM Bank2 Physical memory device test goes wrong."
30007	"VSM SDRAM Bank1 VSM interrupt register A has a -stuck at- error for value:"
30008	"VSM SDRAM Bank2 VSM interrupt register A has a -stuck at- error for value:"
30100	""
30101	"VSM SDRAM Bank1 Memory databus test goes wrong."
30102	"VSM SDRAM Bank1 Memory addressbus test goes wrong."
30103	"VSM SDRAM Bank1 Physical memory device test goes wrong."
30104	" VSM SDRAM Bank2 Memory databus test goes wrong."
30105	" VSM SDRAM Bank2 Memory addressbus test goes wrong."
30106	" VSM SDRAM Bank2 Physical memory device test goes wrong."
30200	""
30201	"VSM SDRAM Bank1 Memory databus test goes wrong."
30202	"VSM SDRAM Bank1 Memory addressbus test goes wrong."
30203	"VSM SDRAM Bank1 Physical memory device test goes wrong."
30204	" VSM SDRAM Bank2 Memory databus test goes wrong."
30205	" VSM SDRAM Bank2 Memory addressbus test goes wrong."
30206	" VSM SDRAM Bank2 Physical memory device test goes wrong."
30300	""
30301	"VSM interrupt register A has a -stuck at- error for value:"
30302	"VSM interrupt register B has a -stuck at- error for value:"
30303	"Interrupt A wasn't raised."
30304	"Interrupt B wasn't raised."
30305	"Interrupts A and B were raised."
30400	""
30401	"VSM SDRAM Bank1 Memory databus test goes wrong."
30402	"VSM SDRAM Bank1 Memory addressbus test goes wrong."
30403	"VSM SDRAM Bank1 Physical memory device test goes wrong."
30404	" VSM SDRAM Bank2 Memory databus test goes wrong."
30405	" VSM SDRAM Bank2 Memory addressbus test goes wrong."
30406	" VSM SDRAM Bank2 Physical memory device test goes wrong."
30500	""
30501	"Communication with the analogue board fails."
30502	"Echo test to analogue board returned wrong string."
40000	""
40001	"NVRAM Reset; I2C failed"
40100	"NVRAM address = 0xaddress -> Byte value = 0xvalue"
40101	"NVRAM Read; I2C failed"
40102	"NVRAM Read; Invalid input"
40200	""
40201	"NVRAM Modify; I2C failed"
40202	"NVRAM Modify; Invalid input"
40300	"DV Unique ID = id"
40301	"NVRAM Read DV Unique ID; I2C failed"
40400	"\r\n Error log:\r\n errorString \r\n Ö "
40401	"NVRAM error log; I2C failed"
40402	"NVRAM error log is invalid"
40403	"Front panel failed"
40700	""
40701	"NVRAM error log reset; I2C failed"
40900	"Region code Change counter is reset"
40901	"NVRAM region code reset; I2C failed"
41000	""
41001	"NVRAM Store DV Unique ID; I2C failed"
41002	"NVRAM Store DV Unique ID; Invalid input"
50000	""
50007	"Execution of the command on the analogue board failed."
50008	"The frontpanel could not be accessed by the analogue board."
50009	"The echo from the frontpanel processor was not correct."
50100	" Front panel version: FPversion "

Error Nr	Error String
50102	"Execution of the command on the analogue board failed."
50103	"The frontpanel could not be accessed by the analogue board."
50200	""
50204	"Execution of the command on the analogue board failed."
50205	"The frontpanel could not be accessed by the analogue board."
50206	"The frontpanel did not show a starburst."
50207	"The user skipped the FP-which pattern test."
50208	"The user returned an unknown confirmation: confirmation "
50209	"The frontpanel did not show horizontal segments."
50210	"The frontpanel did not show vertical segments."
50300	""
50304	"Execution of the command on the analogue board failed."
50305	"The frontpanel could not be accessed by the analogue board."
50306	"The frontpanel did not light all labels."
50307	"The user skipped the rest of the FP-label test."
50308	"The user returned an unknown confirmation: confirmation"
50400	""
50404	"Execution of the command on the analogue board failed."
50405	"The frontpanel could not be accessed by the analogue board."
50406	"The LED's could not be turned on."
50407	"The user skipped the rest of the FP-LED test."
50408	"The user returned an unknown confirmation: confirmation"
50500	""
50502	"Front panel Keyboard; test failed"
50503	"Front panel Keyboard; test aborted"
50504	"Front panel Keyboard; not all keys were pressed"
50505	"Front panel keyboard I2C connection failed"
50506	"Unable to get slashversion"
50600	""
50602	"Front panel Remote control; test failed"
50603	"Front panel Remote control; test aborted"
50604	"Front panel remote control; can not access FP"
50605	"Front panel remote control; no user input received"
50700	""
50701	"Execution of the command on the analogue board failed."
50702	"The frontpanel could not be accessed by the analogue board."
50703	"The frontpanel did not show a starburst."
50704	"The user skipped the FP-starburst test."
50705	"The user returned an unknown confirmation: confirmation "
50800	""
50801	"Execution of the command on the analogue board failed."
50802	"The frontpanel could not be accessed by the analogue board."
50803	"The frontpanel did not show vertical segments."
50804	"The user skipped the FP-vertical segments test."
50805	"The user returned an unknown confirmation: confirmation "
50900	""

Error Nr	Error String
50901	"Execution of the command on the analogue board failed."
50902	"The frontpanel could not be accessed by the analogue board."
50903	"The frontpanel did not show horizontal segments."
50904	"The user skipped the FP-horizontal segments test."
50905	"The user returned an unknown confirmation: confirmation "
51400	""
51401	"Execution of the command on the analogue board failed."
51402	"The frontpanel could not be accessed by the analogue board."
51403	"The beeper did not sound."
51404	"The user skipped the FP-Beep test."
51405	"The user returned an unknown confirmation: confirmation"
51500	""
51501	"Execution of the command on the analogue board failed."
51502	"The frontpanel could not be accessed by the analogue board."
51503	"The discbar did not display properly."
51504	"The user skipped the discbar test."
51505	"The user returned an unknown confirmation: confirmation"
51600	""
51601	"Execution of the command on the analogue board failed."
51602	"The frontpanel could not be accessed by the analogue board."
51603	"The discbar dots did not display properly."
51604	"The user skipped the discbar dots test."
51605	"The user returned an unknown confirmation: confirmation"
51700	""
51701	"Execution of the command on the analogue board failed."
51702	"The frontpanel could not be accessed by the analogue board."
51703	"The VU grid did not display properly."
51704	"The user skipped the VU gridtest."
51705	"The user returned an unknown confirmation: confirmation"
51800	""
51801	"Execution of the command on the analogue board failed."
51802	"The frontpanel could not be accessed by the analogue board."
51803	"The frontpanel could not be dimmed."
51804	"The user skipped the FP-Dim test."
51805	"The user returned an unknown confirmation: confirmation"
51900	""
51901	"Execution of the command on the analogue board failed."
51902	"The frontpanel could not be accessed by the analogue board."
51903	"The frontpanel did not show segments blinking."
51904	"The user skipped the FP-blinking test."
51905	"The user returned an unknown confirmation: confirmation"
52000	""

Error Nr	Error String
52001	"Execution of the command on the analogue board failed."
52002	"The frontpanel could not be accessed by the analogue board."
52003	"The frontpanel did not show all segments lit."
52004	"The user skipped the FP-light all segments test."
52005	"The user returned an unknown confirmation: confirmation"
52200	""
52201	"Communication with Analogue Board fails."
52202	"Frontpanel can not be accessed by the Analogue Board."
52300	""
52301	"Communication with Analogue Board fails."
52302	"Frontpanel can not be accessed by the Analogue Board."
60000	""
60100	""
60101	"Basic Engine returned error number 0xerrornumber"
60102	"Parity error from Basic Engine to Serial"
60103	"Communication time-out error"
60104	"Unexpected response from Basic Engine"
60105	"Echo loop could not be closed"
60106	"Wrong echo pattern received"
60200	"Version: nr1.nr2.nr3"
60201	"Basic Engine returned error number 0xerrornumber"
60202	"Parity error from Basic Engine to Serial"
60203	"Communication time-out error"
60204	"Unexpected response from Basic Engine"
60205	"Front Panel failed."
60300	""
60301	"Basic-Engine time-out error"
60400	""
60401	"Basic Engine returned error number 0xerrornumber"
60402	"Parity error from Basic Engine to Serial"
60403	"Communication time-out error"
60404	"Unexpected response from Basic Engine"
60405	"Focus loop could not be closed"
60500	""
60501	"Basic Engine returned error number 0xerrornumber"
60502	"Parity error from Basic Engine to Serial"
60503	"Communication time-out error"
60504	"Unexpected response from Basic Engine"
60600	""
60601	"Basic Engine returned error number 0xerrornumber"
60602	"Parity error from Basic Engine to Serial"
60603	"Communication time-out error"
60604	"Unexpected response from Basic Engine"
60700	""
60701	"Basic Engine returned error number 0xerrornumber"
60702	"Parity error from Basic Engine to Serial"
60703	"Communication time-out error"
60704	"Unexpected response from Basic Engine"
60800	""
60801	"Basic Engine returned error number 0xerrornumber"
60802	"Parity error from Basic Engine to Serial"

Error Nr	Error String
60803	"Communication time-out error"
60804	"Unexpected response from Basic Engine"
60805	"Radial loop could not be closed"
60900	""
60901	"Basic Engine returned error number 0xerrornumber"
60902	"Parity error from Basic Engine to Serial"
60903	"Communication time-out error"
60904	"Unexpected response from Basic Engine"
61500	""
61501	"Basic Engine returned error number 0xerrornumber"
61502	"Parity error from Basic Engine to Serial"
61503	"Communication time-out error"
61504	"Unexpected response from Basic Engine"
61600	""
61601	"Basic Engine returned error number 0xerrornumber"
61602	"Parity error from Basic Engine to Serial"
61603	"Communication time-out error"
61604	"Unexpected response from Basic Engine"
61700	""
61701	"BE tray-in command failed"
61702	"BE read-TOC command failed"
61703	"BE VSM interrupt initialisation failed"
61704	"BE set irq command failed"
61705	"BE no disc or wrong disc inserted"
61706	"BE rec-pause command failed"
61707	"BE VSM BE out DMA initialisation failed"
61708	"BE VSM BE out initialisation failed"
61709	"BE VSM BE out DMA start failed"
61710	"BE VSM BE out start failed"
61711	"BE rec command failed"
61712	"BE VSM out underrun error occurred"
61713	"BE record complete interrupt not raised"
61714	"BE get irq command failed"
61715	"BE no interrupt was raised by BE"
61716	"BE VSM DMA out not finished"
61717	"BE stop command after writing failed"
61718	"BE VSM Sector processor initialisation failed"
61719	"BE VSM sector processor DMA initialisation failed"
61720	"BE VSM sector processor DMA start failed"
61721	"BE VSM sector processor start failed"
61722	"BE seek command failed"
61723	"BE VSM sector processor error occurred"
61724	"BE read timeout occurred"
61725	"BE stop command after reading failed"
61726	"BE difference found in data at disc sector 0xdiscsector"
61727	"This nucleus cannot be executed because the Self-Test failed"
61800	""
61801	"BE i2c initialisation failed"
61802	"This nucleus cannot be executed because the Self-Test failed"
61900	""
61901	"The SelfTest failed with result: 0xnr1 0xnr2 0xnr3"
61902	"Basic Engine returned error number 0xerrornumber"
61903	"Parity error from Basic Engine to Serial"
61904	"Communication time-out error"

Error Nr	Error String
61905	"Unexpected response from Basic Engine"
62000	""
62001	"Self-Test : errorstring1 Laser-Test : errorstring2 SpindleM-Test: errorstring3 SledgeM-Test : errorstring4 Focus-Test : errorstring5"
62100	"The forward sense level is 0xlevel"
62101	"Basic Engine returned error number 0xerrornumber"
62102	"Parity error from Basic Engine to Serial"
62103	"Communication time-out error"
62104	"Unexpected response from Basic Engine"
62200	""
62201	"The BE-self-diagnostic-spindle-motor-test failed"
62202	"Basic Engine returned error number 0xerrornumber"
62203	"Parity error from Basic Engine to Serial"
62204	"Communication time-out error"
62205	"Unexpected response from Basic Engine"
62300	""
62301	"The BE-focus-test failed"
62302	"Basic Engine returned error number 0xerrornumber"
62303	"Parity error from Basic Engine to Serial"
62304	"Communication time-out error"
62305	"Unexpected response from Basic Engine"
62400	""
62401	"The BE-self-diagnostic-sledge-motor-test failed"
62402	"Basic Engine returned error number 0xerrornumber"
62403	"Parity error from Basic Engine to Serial"
62404	"Communication time-out error"
62405	"Unexpected response from Basic Engine"
62500	""
62600	""
62700	"BE EEPROM address = address -> Byte value = 0xvalue"
62701	"Basic Engine returned error number 0xerrornumber"
62702	"Parity error from Basic Engine to Serial"
62703	"Communication time-out error"
62704	"Unexpected response from Basic Engine"
62705	"BE read EEPROM; invalid input"
62800	""
62801	"Basic Engine returned error number 0xerrornumber"
62802	"Parity error from Basic Engine to Serial"
62803	"Communication time-out error"
62804	"Unexpected response from Basic Engine"
62805	"BE write EEPROM; invalid input"
62900	""
62901	"Basic Engine returned error number 0xerrornumber"
62902	"Parity error from Basic Engine to Serial"
62903	"Communication time-out error"
62904	"Unexpected response from Basic Engine"
62905	"Radial loop could not be closed"
63000	""
63001	"Basic Engine returned error number 0xerrornumber"
63002	"Parity error from Basic Engine to Serial"
63003	"Communication time-out error"
63004	"Unexpected response from Basic Engine"

Error Nr	Error String
63100	" Number of times Tray went Open/Closed : nr1"" Total hours the CD laser was on : nr2"" Total hours the DVD laser was on : nr3"" Total hours the write laser was on : nr4"
63101	"Basic Engine returned error number 0xerrornumber"
63102	"Parity error from Basic Engine to Serial"
63103	"Communication time-out error"
63104	"Unexpected response from Basic Engine"
63200	""
63201	"Basic Engine returned error number 0xerrornumber"
63202	"Parity error from Basic Engine to Serial"
63203	"Communication time-out error"
63204	"Unexpected response from Basic Engine"
63300	Momentary errors (Byte 1 - Byte 7) : 0xb1 0xb2 0xb3 0xb4 0xb5 0xb6 0xb7 Cumulative errors (Byte 1 - Byte 7): : 0xb1 0xb2 0xb3 0xb4 0xb5 0xb6 0xb7 Fatal errors (Oldest - Youngest) : : 0xb1 0xb2 0xb3 0xb4 0xb5
63301	"Basic Engine returned error number 0xerrornumber"
63302	"Parity error from Basic Engine to Serial"
63303	"Communication time-out error"
63304	"Unexpected response from Basic Engine"
63400	""
63401	"Basic Engine returned error number 0xerrornumber"
63402	"Parity error from Basic Engine to Serial"
63403	"Communication time-out error"
63404	"Unexpected response from Basic Engine"
63500	""
63501	"Basic Engine returned error number 0xerrornumber"
63502	"Parity error from Basic Engine to Serial"
63503	"Communication time-out error"
63504	"Unexpected response from Basic Engine"
63505	"errorstring ÕThe basic engine will reject all player commands"
63900	""
63901	"Basic Engine returned error number 0xerrornumber"
63902	"Parity error from Basic Engine to Serial"
63903	"Communication time-out error"
63904	"Unexpected response from Basic Engine"
64000	"BE OPU number = opunumber"
64001	"Basic Engine returned error number 0xerrornumber"
64002	"Parity error from Basic Engine to Serial"
64003	"Communication time-out error"
64004	"Unexpected response from Basic Engine"
64100	"The data was successfully written on and read from a DVD disc"
64101	"The tray-in command failed"
64102	"The read-TOC command failed"
64103	"The VSM interrupt initialisation failed"
64104	"The set irq command failed"
64105	"No disc or wrong disc inserted"
64106	"The rec-pause command failed"
64107	"The VSM BE out DMA initialisation failed"
64108	"The VSM BE out initialisation failed"
64109	"The VSM BE out DMA start failed"
64110	"The VSM BE out start failed"
64111	"The rec command failed"

Error Nr	Error String
64112	"The VSM out underrun error occurred"
64113	"The record complete interrupt was not raised"
64114	"The get irq command failed"
64115	"There was no interrupt raised by BE"
64116	"The VSM DMA did not finished"
64117	"The stop command after writing failed"
64118	"The VSM Sector processor initialisation failed"
64119	"The VSM sector processor DMA initialisation failed"
64120	"The VSM sector processor DMA start failed"
64121	"The VSM sector processor start failed"
64122	"The seek command failed"
64123	"The VSM sector processor error occurred"
64124	"The read timeout occurred"
64125	"The stop command after reading failed"
64126	"There was a difference found in data at a specific disc sector"
64127	"The result of the self test contains errors"
64128	"An error interrupt was raised by BE"
64129	"The calibrate-record command failed"
64130	"To many retries"
64131	"BE update RAI command after writing failed"
64132	"BE find first recordable address command failed"
64133	"DVD+R disc is full"
64200	""
64201	"BE i2c initialisation failed"
64202	"This nucleus cannot be executed because the Self-Test failed"
70000	"Echo test OK"
70001	"Echo test returned wrong string."
70002	"Communication with Analogue Board fails"
70300	"SoftwareVersion"
70301	"Can not find segment in FLASH ROM on the Analogue Board"
70302	"Communication with Analogue Board fails"
70400	"HardwareVersion"
70401	"Can not find segment in FLASH ROM on the Analogue Board"
70402	"Communication with Analogue Board fails"
70500	"Clock adjusted OK"
70501	"Can not adjust the clock on the Analogue Board."
70502	"Wrong date/time text size."
70503	"Communication with Analogue Board fails"
70600	"Tuner accessibility test OK"
70601	"Can not access tuner on the Analogue Board."
70602	"Communication with Analogue Board fails"
70700	"Frequency download OK"
70701	"Wrong frequency table size."
70702	"Can not download the frequency table into the analogue NVRAM."
70703	"Can not download the frequency table into the analogue NVRAM."
70704	"Communication with Analogue Board fails"
70800	"Data slicer test OK"
70801	"Test of the Data slicer on the Analogue Board fails."
70802	"Communication with Analogue Board fails"
70900	"Sound Processor test OK"
70901	"Test of the Sound Processor on the Analogue Board fails."
70902	"Communication with Analogue Board fails"
71000	"AV Selector test OK"
71001	"Test of the AV Selector on the Analogue Board fails."
71002	"Communication with Analogue Board fails"
71100	"NVRAM test OK"
71101	"Test of the NVRAM on the Analogue Board fails."
71102	"Communication with Analogue Board fails"
71200	"Video routing on the Analogue Board OK"
71201	"Routing the video on the Analogue Board fails."
71202	"Invalid input."
71203	"Communication with Analogue Board fails"
71300	"Audio routing on the Analogue Board OK"
71301	"Routing the audio on the Analogue Board fails."
71302	"Invalid input."
71303	"Communication with Analogue Board fails"
71500	""
71501	"Invalid slash version, default slash version is set."
71502	"Setting the slash version on the Analogue Board fails."
71503	"Communication with Analogue Board fails"
71600	"ApplicationVersion"
71601	"Can not find segment in FLASH ROM on the Analogue Board"
71602	"Communication with Analogue Board fails"
71700	"DiagnosticsVersion"
71701	"Can not find segment in FLASH ROM on the Analogue Board"
71702	"Communication with Analogue Board fails"
71800	"DownloadVersion"
71801	"Can not find segment in FLASH ROM on the Analogue Board"
71802	"Communication with Analogue Board fails"
72300	""
72000	""
72001	"Adjusting BarGraphLevel failed"
72002	"Communication with Analogue Board fails"
72100	""
72101	"Storing clock correction failed"
72102	"Value out of range : default value stored "
72103	"Invalid input."
72104	"Communication with Analogue Board fails"
72200	""
72201	"Initialising the 1Hz signal on the Clock IC failed"
72202	"Communication with Analogue Board fails"
72301	"Clearing the NVRAM on the Analogue Board fails"
72302	"Communication with Analogue Board fails"
72400	"segment checksum is : checksum which is correct" for every segment
72401	"segment could not be found" or "segment checksum is : checksumC ,however it should be : checksumE" for every segment
72402	"Communication with Analogue Board fails"
72900	"Date received"
72901	"Data returned"
72902	"Communication on I2C-bus failed on the Analogue Board fails."
72903	"Communication with Analogue Board fails"
73000	""
73001	"Storing the external presets on the Analogue Board fails"
73002	"Communication with Analogue Board fails"
73100	"0xslashversion" where slashversion is the slash version read from the analogue board
73101	"Error while reading out slash version."

Error Nr	Error String
73102	"I2C Write error."
73103	"I2C Read error."
73104	"Communication with Analogue Board fails"
73200	""
73201	"Storing the Reference Voltage for the Tuner failed"
73202	"Invalid input."
73203	"Communication with Analogue Board fails"
80000	"The DVIO module is present in the system."
80001	"The DVIO module is not present in the system."
80100	"The DVIO module has been reset OK."
80101	"The DVIO module is not present in the system."
80102	"The DVIO module could not be reset."
80103	"Could not initialise I2C before Reset."
80200	"The accessibility of the DVIO module is OK."
80201	"The DVIO board is not present in this DVDR."
80202	"Could not initialise I2C."
80203	"Unable to reset the DVIO module."
80204	"Unable to receive the reset indication from the DVIO module."
80205	"Unable to send the configuration to the DVIO module."
80206	"Unable to download the chip ID to the DVIO module."
80207	"Unable to set the mode of the DVIO module to IDLE."
80208	"Software Error in function HandleStateAwaitingReply !!"
80209	"Maximal number of retries reached by HandleStateSending !!"
80210	"Maximal number of retries (NACKs) reached (HandleStateSending)"
80211	"We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times !!"
80212	"We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times !!"
80213	"We tried to receive an Ack for DVIO_MAX_RETRIES_ACK times!!"
80214	"VSM UART error timeout transmitting command"
80215	"VSM UART error timeout receiving reply"
80216	"VSM UART frame error occurred receiving from DVIO board"
80217	"VSM UART parity error occurred receiving from DVIO board"
80218	"The confirmation/indication from the DVIO module is invalid."
80300	"The accessibility of the DVIO module is OK."
80301	"The DVIO board is not present in this DVDR."
80302	"Could not initialise I2C."
80303	"Unable to reset the DVIO module."
80304	"Unable to receive the reset indication from the DVIO module."
80305	"Unable to send the configuration to the DVIO module."
80306	"Unable to download the chip ID to the DVIO module."
80307	"Unable to set the mode of the DVIO module to IDLE."
80308	"Software Error in function HandleStateAwaitingReply !!"
80309	"Maximal number of retries reached by HandleStateSending !!"
80310	"Maximal number of retries (NACKs) reached (HandleStateSending)"
80311	"We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times !!"
80312	"We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times !!"
80313	"We tried to receive an Ack for DVIO_MAX_RETRIES_ACK times!!"
80314	"VSM UART error timeout transmitting command"
80315	"VSM UART error timeout receiving reply"
80316	"VSM UART frame error occurred receiving from DVIO board"
80317	"VSM UART parity error occurred receiving from DVIO board"
80318	"The confirmation/indication from the DVIO module is invalid."
80400	"The accessibility of the DVIO module is OK."
80401	"The DVIO board is not present in this DVDR."
80402	"Could not initialise I2C."
80403	"Unable to reset the DVIO module."
80404	"Unable to receive the reset indication from the DVIO module."
80405	"Unable to send the configuration to the DVIO module."
80406	"Unable to download the chip ID to the DVIO module."
80407	"Unable to set the mode of the DVIO module to IDLE."
80408	"Software Error in function HandleStateAwaitingReply !!"
80409	"Maximal number of retries reached by HandleStateSending !!"
80410	"Maximal number of retries (NACKs) reached (HandleStateSending)"
80411	"We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times !!"
80412	"We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times !!"
80413	"We tried to receive an Ack for DVIO_MAX_RETRIES_ACK times!!"
80414	"VSM UART error timeout transmitting command"
80415	"VSM UART error timeout receiving reply"
80416	"VSM UART frame error occurred receiving from DVIO board"
80417	"VSM UART parity error occurred receiving from DVIO board"
80418	"The confirmation/indication from the DVIO module is invalid."
80500	""
80501	"The DVIO board is not present in this DVDR."
80502	"The I2C could not be initialised."
80503	"The DVIO module could not be reset."
80504	"Unable to receive the reset indication from the DVIO module."
80505	"Unable to send the configuration to the DVIO module."
80506	"Unable to download the chip ID to the DVIO module."
80507	"Unable to set the mode of the DVIO module to IDLE."
80508	"Software Error in HandleStateAwaitingReply function!"
80509	"Maximal number of retries reached by HandleStateSending!"
80510	"Maximal number of retries (NACK's) reached "(HandleStateSending)
80511	"We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times!"

Error Nr	Error String
80512	"We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times!"
80513	"We tried to receive an Acknowledge for DVIO_MAX_RETRIES_ACK times!"
80514	"VSM UART error timeout transmitting command"
80515	"VSM UART error timeout receiving reply"
80516	"VSM UART frame error occurred receiving from DVIO board"
80517	"VSM UART parity error occurred receiving from DVIO board"
80518	"The confirmation/indication from the DVIO module is invalid."
80519	"Setting the DVIO module in/out diagnostics mode failed"
80520	"Invalid input"
80521	"Getting the errors of the self-test failed"
80522	"Self-test failed"
80600	""
80601	"The DVIO board is not present in this DVDR."
80602	"The I2C could not be initialised."
80603	"The DVIO module could not be reset."
80604	"Unable to receive the reset indication from the DVIO module."
80605	"Unable to send the configuration to the DVIO module."
80606	"Unable to download the chip ID to the DVIO module."
80607	"Unable to set the mode of the DVIO module to IDLE."
80608	"Software Error in HandleStateAwaitingReply function!"
80609	"Maximal number of retries reached by HandleStateSending!"
80610	"Maximal number of retries (NACK's) reached "(HandleStateSending)
80611	"We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times!"
80612	"We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times!"
80613	"We tried to receive an Acknowledge for DVIO_MAX_RETRIES_ACK times!"
80614	"VSM UART error timeout transmitting command"
80615	"VSM UART error timeout receiving reply"
80616	"VSM UART frame error occurred receiving from DVIO board"
80617	"VSM UART parity error occurred receiving from DVIO board"
80618	"The confirmation/indication from the DVIO module is invalid."
80619	"Setting the DVIO module in/out diagnostics mode failed"
80700	""
80701	"The DVIO board is not present in this DVDR."
80702	"The I2C could not be initialised."
80703	"The DVIO module could not be reset."
80704	"Unable to receive the reset indication from the DVIO module."
80705	"Unable to send the configuration to the DVIO module."
80706	"Unable to download the chip ID to the DVIO module."
80707	"Unable to set the mode of the DVIO module to IDLE."
80708	"Software Error in HandleStateAwaitingReply function!"

Error Nr	Error String
80709	"Maximal number of retries reached by HandleStateSending!"
80710	"Maximal number of retries (NACK's) reached "(HandleStateSending)
80711	"We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times!"
80712	"We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times!"
80713	"We tried to receive an Acknowledge for DVIO_MAX_RETRIES_ACK times!"
80714	"VSM UART error timeout transmitting command"
80715	"VSM UART error timeout receiving reply"
80716	"VSM UART frame error occurred receiving from DVIO board"
80717	"VSM UART parity error occurred receiving from DVIO board"
80718	"The confirmation/indication from the DVIO module is invalid."
80719	"Setting the DVIO module in/out diagnostics mode failed"
90121	"Error: audio data in host memory contains wrong frequency: frequency Hz"
90122	"Error: audio data in host memory contains silence!"
90123	"There is no correct audio frame in the buffer"
90124	"The audio frame has an illegal version bit"
90125	"The audio frame has an illegal bitrate-index"
90126	"The audio frame has an illegal sampling rate"
90127	"The CRC of the audio frame is wrong"
90128	"The audio frame is not MPEG-I layer II !"
90129	"Error cannot de-mute DAC on analogue board"
90200	""
90201	"Initialisation of I2C failed"
90202	"Initialisation of VIP and EMPIRE failed"
90203	"Initialisation of PLL / Link failed."
90204	"Next descriptor address set wrong."
90205	"Turning on the colourbar failed"
90206	"No I2C communication possible to start video encoder."
90207	"Starting the video encoder failed."
90208	"Transfer of data from video encoder to VSM failed."
90209	"Stopping the encoder failed."
90210	"Turning off the colourbar failed."
90211	"Cannot intialize hostdecoder parallel input"
90212	"Cannot initialise VSM AV-out DMA port"
90213	"Cannot initialise VSM AV-out port"
90214	"Cannot start VSM AV-out DMA port"
90215	"Cannot start VSM AV-out port"
90216	"Transfer of data from VSM to host decoder failed."
90217	"VSM and Hostdec memory do not match (compared after transfer)"
90218	"Decoding of the video data in the hostdecoder memory failed"
90219	"The data in the hostdecoder is not equal to a colourbar"
90220	"The video encoder did not return the Group Of Picture count."
90221	"The video encoder did not receive data from the VIP."
90223	"Initialisation of VIP and EMPRESS failed"
90224	"The video encoder did not return the current status."

Error Nr	Error String
90225	"The video encoder timed out in BUSY mode. (no VIP input)"
90226	"The video encoder did not return the current bitrate."
90227	"The video encoder did not switch to ENCODING mode."
90228	"The video encoder could not start from STOP/ IDLE mode."
90229	"The video encoder did not switch from IDLE to STOP mode."
90300	""
90301	"Initialisation of I2C failed"
90302	"I2C communication to VIP failed"
90303	"Initialisation of VIP failed"
90304	"Generation of Close Caption data failed"
90305	"VIP not locked to video signal"
90306	"Initialisation of VBI Extractor failed
90307	"No CC data received"
90308	"Closed Caption data overrun"
90309	"Closed Caption data does not match"
90310	"Switch off ColourBar failed"
90400	""
90401	"Initialisation of I2C failed"
90402	"Initialisation of VIP and EMPIRE failed"
90403	"Initialisation of PLL / Link failed."
90404	"Next descriptor address set wrong."
90405	"Turning on the colourbar failed"
90406	"No I2C communication possible to start video encoder."
90407	"Starting the video encoder failed."
90408	"Transfer of data from video encoder to VSM failed."
90409	"Stopping the encoder failed."
90410	"Turning off the colourbar failed."
90411	"Cannot intialize hostdecoder parallel input"
90412	"Cannot initialise VSM AV-out DMA port"
90413	"Cannot initialise VSM AV-out port"
90414	"Cannot start VSM AV-out DMA port"
90415	"Cannot start VSM AV-out port"
90416	"Transfer of data from VSM to host decoder failed."
90417	"VSM and Hostdec memory do not match (compared after transfer)"
90418	"Decoding of the video data in the hostdecoder memory failed"
90419	"The data in the hostdecoder is not equal to a colourbar"
90420	"The video encoder did not return the Group Of Picture count."
90421	"The video encoder did not receive data from the VIP."
90422	"Execution of the command on the analogue board failed."
90423	"Initialisation of VIP and EMPRESS failed"
90424	"The video encoder did not return the current status."
90425	"The video encoder timed out in BUSY mode. (no VIP input)"
90426	"The video encoder did not return the current bitrate."
90427	"The video encoder did not switch to ENCODING mode."
90428	"The video encoder could not start from STOP/ IDLE mode."
90429	"The video encoder did not switch from IDLE to STOP mode."
90500	""
90501	"Initialisation of I2C failed"
90502	"I2C communication to VIP failed"
90503	"Initialisation of VIP failed"
90504	"Generation of Close Caption data failed"
90505	"VIP not locked to video signal"
90506	"Initialisation of VBI Extractor failed
90507	"No CC data received"
90508	"Closed Caption data overrun"
90509	"Closed Caption data does not match"
90510	"Switch off ColourBar failed"
90511	"Execution of the command on the analogue board failed."
90600	""
90601	"Initialisation of I2C failed"
90602	"Initialisation of VIP and EMPIRE failed"
90603	"Initialisation of PLL / Link failed."
90604	"Next descriptor address set wrong."
90605	"Turning on the colourbar failed"
90606	"No I2C communication possible to start video encoder."
90607	"Starting the video encoder failed."
90608	"Transfer of data from video encoder to VSM failed."
90609	"Stopping the encoder failed."
90610	"Turning off the colourbar failed."
90611	"Cannot intialize hostdecoder parallel input"
90612	"Cannot initialise VSM AV-out DMA port"
90613	"Cannot initialise VSM AV-out port"
90614	"Cannot start VSM AV-out DMA port"
90615	"Cannot start VSM AV-out port"
90616	"Transfer of data from VSM to host decoder failed."
90617	"VSM and Hostdec memory do not match (compared after transfer)"
90618	"Decoding of the video data in the hostdecoder memory failed"
90619	"The data in the hostdecoder is not equal to a colourbar"
90620	"The video encoder did not return the Group Of Picture count."
90621	"The video encoder did not receive data from the VIP."
90622	"Execution of the command on the analogue board failed."
90623	"Initialisation of VIP and EMPRESS failed"
90624	"The video encoder did not return the current status."
90625	"The video encoder timed out in BUSY mode. (no VIP input)"
90626	"The video encoder did not return the current bitrate."
90627	"The video encoder did not switch to ENCODING mode."
90628	"The video encoder could not start from STOP/ IDLE mode."
90629	"The video encoder did not switch from IDLE to STOP mode."
90700	""
90701	"Initialisation of I2C failed"
90702	"I2C communication to VIP failed"
90703	"Initialisation of VIP failed"
90704	"Generation of Close Caption data failed"

Error Nr	Error String
90705	"VIP not locked to video signal"
90706	"Initialisation of VBI Extractor failed
90707	"No CC data received"
90708	"Closed Caption data overrun"
90709	"Closed Caption data does not match"
90710	"Switch off ColourBar failed"
90711	"Execution of the command on the analogue board failed."
90800	""
90801	"Error routing the audio back to the digital board."
90802	"Error cannot initialise I2C"
90803	"Error cannot initialise VIP"
90804	"Error cannot set ADC enable pin"
90805	"Error cannot set VSM audio clock"
90806	"Error preparing the 12kHz audio-sine"
90807	"Error cannot initialise audio encoder"
90808	"Error cannot initialise VSM audio in port"
90809	"Error cannot initialise VSM audio in DMA port"
90810	"Error cannot initialise VSM audio out DMA port"
90811	"Error cannot initialise audio VSM out port"
90812	"Error cannot initialise host decoder audio in"
90813	"Error loop audio user/dealer cannot start audio encoder"
90814	"Error cannot start VSM audio in DMA port"
90815	"Error starting the 12kHz audio-sine"
90816	"Error transfer data from audio encoder to VSM"
90817	"Error cannot start VSM AV out DMA port"
90818	"Error cannot start VSM AV out port"
90819	"Error transfer data from VSM to host decoder"
90820	"Error: audio data in host memory and VSM memory differ"
90821	"Error: audio data in host memory contains wrong frequency: frequency Hz"
90822	"Error: audio data in host memory contains silence!"
90823	"There is no correct audio frame in the buffer"
90824	"The audio frame has an illegal version bit"
90825	"The audio frame has an illegal bitrate-index"
90826	"The audio frame has an illegal sampling rate"
90827	"The CRC of the audio frame is wrong"
90828	"The audio frame is not MPEG-I layer II !"
90829	"Error cannot de-mute DAC on analogue board"
90900	""
90901	"Error routing the audio back to the digital board."
90902	"Error cannot initialise I2C"
90903	"Error cannot initialise VIP"
90904	"Error cannot set ADC enable pin"
90905	"Error cannot set VSM audio clock"
90906	"Error preparing the 12kHz audio-sine"
90907	"Error cannot initialise audio encoder"
90908	"Error cannot initialise VSM audio in port"
90909	"Error cannot initialise VSM audio in DMA port"
90910	"Error cannot initialise VSM audio out DMA port"
90911	"Error cannot initialise audio VSM out port"
90912	"Error cannot initialise host decoder audio in"
90913	"Error loop audio user/dealer cannot start audio encoder"
90914	"Error cannot start VSM audio in DMA port"
90915	"Error starting the 12kHz audio-sine"
90916	"Error transfer data from audio encoder to VSM"
90917	"Error cannot start VSM AV out DMA port"
90918	"Error cannot start VSM AV out port"
90919	"Error transfer data from VSM to host decoder"
90920	"Error: audio data in host memory and VSM memory differ"
90921	"Error: audio data in host memory contains wrong frequency: frequency Hz"
90922	"Error: audio data in host memory contains silence!"
90923	"There is no correct audio frame in the buffer"
90924	"The audio frame has an illegal version bit"
90925	"The audio frame has an illegal bitrate-index"
90926	"The audio frame has an illegal sampling rate"
90927	"The CRC of the audio frame is wrong"
90928	"The audio frame is not MPEG-I layer II !"
90929	"Error cannot de-mute DAC on analogue board"
140000	""
140001	"I2C to Clock failed" or "I2C initialisation failed"
140100	""
140101	"I2C to Clock failed" or "I2C initialisation failed"
141200	""
141201	"Progressive Scan Board I2C bus busy"
141211	"Progressive Scan Board I2C FLI2200 bus busy"
141212	"Progressive Scan Board I2C FLI2200 read access time-out"
141213	"Progressive Scan Board I2C FLI2200 no read acknowledge"
141214	"Progressive Scan Board I2C FLI2200 read failed"
141215	"Progressive Scan Board I2C FLI2200 write access time-out"
141216	"Progressive Scan Board I2C FLI2200 no write acknowledge"
141217	"Progressive Scan Board I2C FLI2200 write failed"
141218	"Progressive Scan Board I2C FLI2200 failed"
141221	"Progressive Scan Board I2C AD7196 bus busy"
141222	"Progressive Scan Board I2C AD7196 read access time-out"
141223	"Progressive Scan Board I2C AD7196 no read acknowledge"
141224	"Progressive Scan Board I2C AD7196 read failed"
141225	"Progressive Scan Board I2C AD7196 write acess time-out"
141226	"Progressive Scan Board I2C AD7196 no write acknowledge"
141227	"Progressive Scan Board I2C AD7196 write failed"
141228	"Progressive Scan Board I2C AD7196 failed"
141300	""
141301	"Progressive Scan Route Enable failed"
141302	"Generating test image in Hostdecoder failed"
141400	""
141401	"Progressive Scan Route Disable failed"
141402	"Turning off test image in Hostdecoder failed"
141500	""
141501	"Progressive Scan Board I2C failed"
141600	""
141601	"Progressive Scan Board I2C failed"

Error Codes Nucleus 805

Error Code	**Description**	**Bus**	**Components**
0x00	No Error	-	-
0x11	No link register access	PA[8:0] I PAD[7:0]	Link I uP
0x12	No link register access or link reset failed	PA[8:0] I PAD[7:0] I 1394_RSTn	Link I uP I FPGA
0x13	No link register access or link reset failed	PA[8:0] I PAD[7:0] I 1394_RSTn	Link I uP I FPGA
0x14	No link register access	PA[8:0] I PAD[7:0]	Link I uP
0x15	No link register access	PA[8:0] I PAD[7:0]	Link I uP
0x16	No link register access	PA[8:0] I PAD[7:0]	Link I uP
0x17	Link reset failed	1394_RSTn	Link I FPGA
0x18	Link reset failed	1394_RSTn	Link I FPGA
0x19	Cycle timer in link chip does not increment	-	Link
0x1A	Interrupt from Link chip does not go low at 8051	LINK_INTn I PINT1n	Link I FPGA I uP
0x1B	Interrupt from Link chip does not go high at 8051	LINK_INTn I PINT1n	Link I FPGA I uP
0x1C	Submission of read request to Phy timed out	Bus_LP	Phy
0x1D	Reception of read data from Phy timed out	Bus_LP	Phy
0x1E	Inproper Phy read address was received from Phy	Bus_LP	Phy
0x1F	Phy write timed out	Bus_LP	Phy
0x20	Could not read reg #2 of Phy	Bus_LP	Phy
0x21	Could not write 0xaa to reg #1 of phy	Bus_LP	Phy
0x22	Could not write 0x55 to reg #1 of phy	Bus_LP	Phy
0x23	Read incorrect default gapcount from Phy	Bus_LP	Phy
0x24	Read incorrect updated gapcount from Phy	Bus_LP	Phy
0x25	Read incorrect gapcount from Phy after reset	F117 I F173	Phy I OptoPR
0x26	Expecting no 1394 connectivity; while Phy.CNA indicates connection	F108 I PHY_CNA I Bus_PC	Phy I OptoCNA I FPGA
0x27	Expecting 1394 connectivity; while Phy.CNA indicates no connection	F108 I PHY_CNA I Bus_PC	Phy I OptoCNA I FPGA
0x28	Expected port1 unconnected; but found connected	Bus_PC	Phy
0x29	Phy read retry limit exceeded	-	Phy
0x2A	Expected port2 unconnected; but found connected	-	Phy
0x2B	Expected port3 unconnected; but found connected	-	Phy
0x2C	Expected 0x1 in lower nibble of Phy reg 7	-	Phy
0x2D	Expected CPS and C bit set in Phy reg 6	-	Phy
0x30	Internal ram problem in address lines	Internal in uP	P89C51RD2
0x31	Internal ram problem in data lines	Internal in uP	P89C51RD2
0x32	External ram problem in address lines	PA[15:0] I PAD[7:0] I PRDn I PWRn	P89C51RD2/CY62256/ 74HC573
0x33	External ram problem in data lines	PAD[7:0]	P89C51RD2/CY62256/ 74HC573
0x34	Problem accessing flex scratch register	PAD[7:0]	EPF6024
0x36	INT0n stuck at '0'	PINT0n	EPF6024 / P89C51RD2
0x37	INT0n stuck at '1'	PINT1n	EPF6024 / P89C51RD2
0x38	Problem accessing NW701 registers	HAD[7:0]IDV_Asn/RWn/DSUn/DSLn	EPF6024 / NW701
0x39	Reset line to NW701 not functioning	DV_RSTn	EPF6024 / NW701
0x3A	Checksum of codespace 0x0000-0xfbff is not 0x00	Incorrectly programmed	P89C51RD2
0xF4	PHY chip not responding	-	Phy
0xF5	LINK chip not responding	-	Phy

5.5 Loop tests

The following loops can be distinguished:

- Loops performed on the digital board only
- User Dealer loops performed on the digital and analogue board
- System loops performed via an external connection: outputs are looped back to the inputs.

5.5.1 Nucleus 900: Digital Audio Loop

This nucleus tests the audio path through the digital board

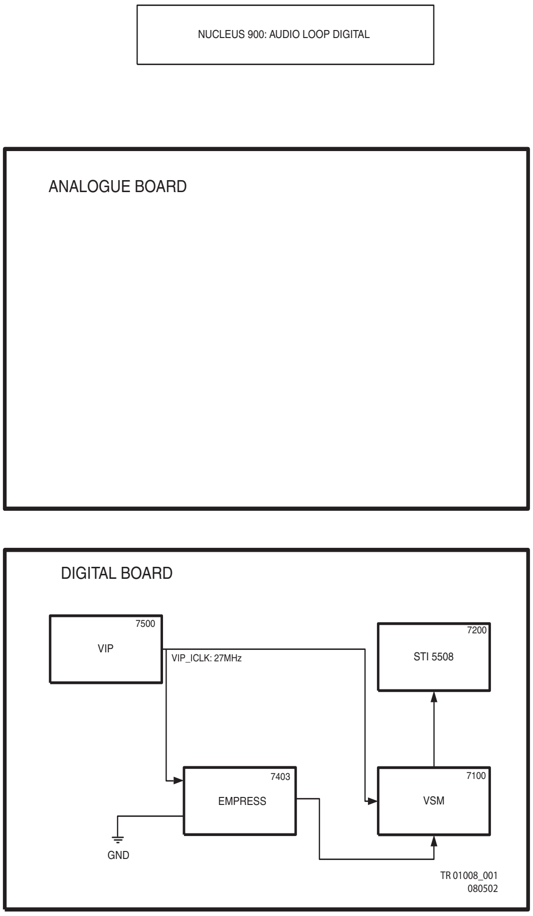

NUCLEUS 900: AUDIO LOOP DIGITAL
ANALOGUE BOARD
DIGITAL BOARD
7500
VIP
VIP_ICLK: 27MHz
7200
STI 5508
7403
EMPRESS
7100
VSM
GND
TR 01008_001
080502

Figure 5-9

5.5.2 Nucleus 901: Audio User Dealer Loop

This Nucleus is only possible in NAFTA sets.
A PCM audio sine of 12kHz is generated in the Host Decoder for a while and sent to the analogue board. The signal coming from the analogue board is encoded again and sent to the memory of the host decoder for comparison. This nucleus tests the components on the audio signal path:

- Host decoder
- Flex connection between connector 1602 (digital board) and connector 1900 (analogue board)
- DAC
- Op-amp
- Scart switch IC
- ADC
- Audio Encoder
- VIP
- VSM

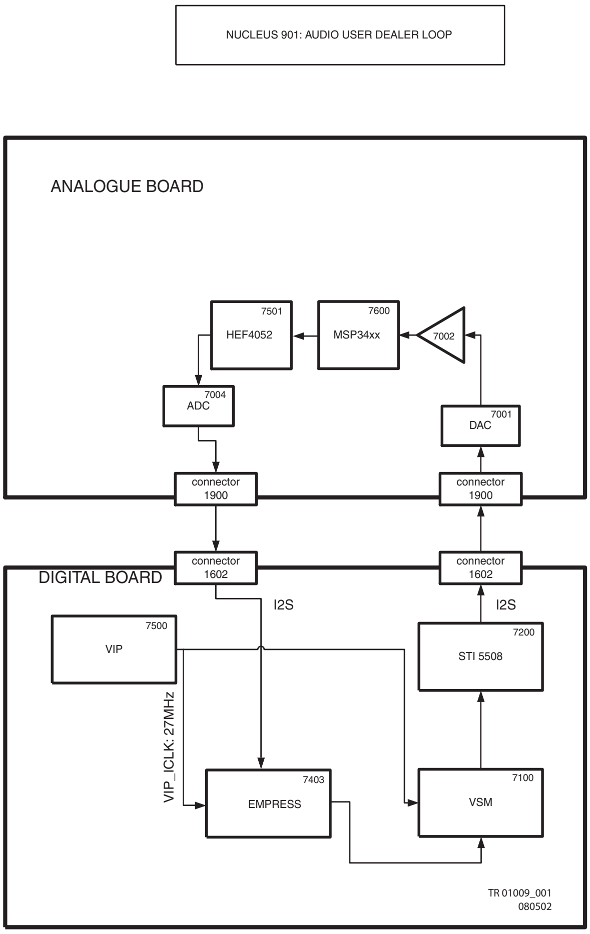

NUCLEUS 901: AUDIO USER DEALER LOOP
ANALOGUE BOARD
7501
HEF4052
7600
MSP34xx
7002
7004
ADC
7001
DAC
connector
1900
connector
1900
connector
1602
connector
1602
DIGITAL BOARD
I2S
I2S
7500
VIP
7200
STI 5508
VIP_ICLK: 27MHz
7403
EMPRESS
7100
VSM
TR 01009_001
080502

Figure 5-10

5.5.3 Nucleus 902: Digital Video Loop

A colourbar generated in the host decoder is looped through the VIP, Empire, and VSM and checked again in the host decoder. The following components are tested on the video signal path:

- VIP
- Empire
- VSM
- Host decoder

NUCLEUS 902: DIGITAL VIDEO LOOP

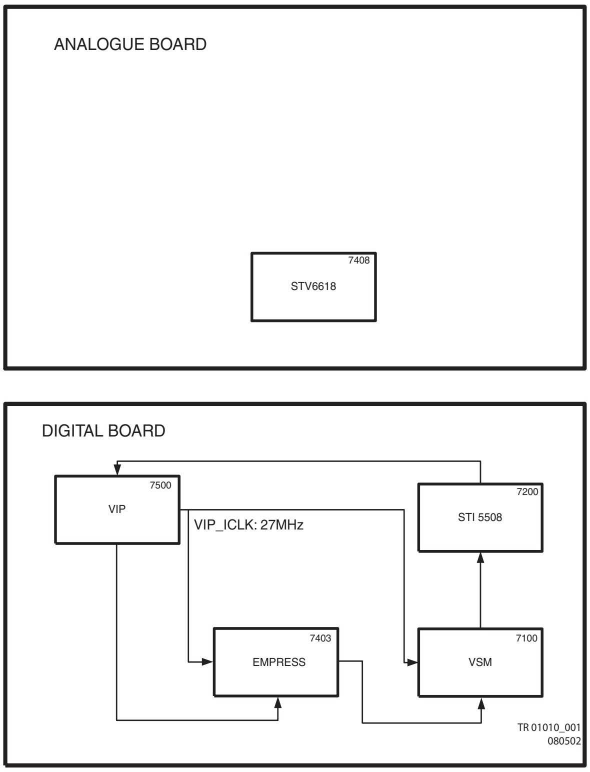

ANALOGUE BOARD
7408
STV6618
DIGITAL BOARD
7500
VIP
VIP_ICLK: 27MHz
7200
STI 5508
7403
EMPRESS
7100
VSM
TR 01010_001
080502

Figure 5-11

5.5.4 Nucleus 903: Digital Video VBI Loop

Nucleus for testing the components on the video VBI signal path:

- The VIP
- The VSM
- The Host Decoder

This is done by using the internal test signal source (digital board only)

Remark: this test is only successful if nucleus 121 is carried out first.

NUCLEUS 903: DIGITAL VIDEO VBI LOOP

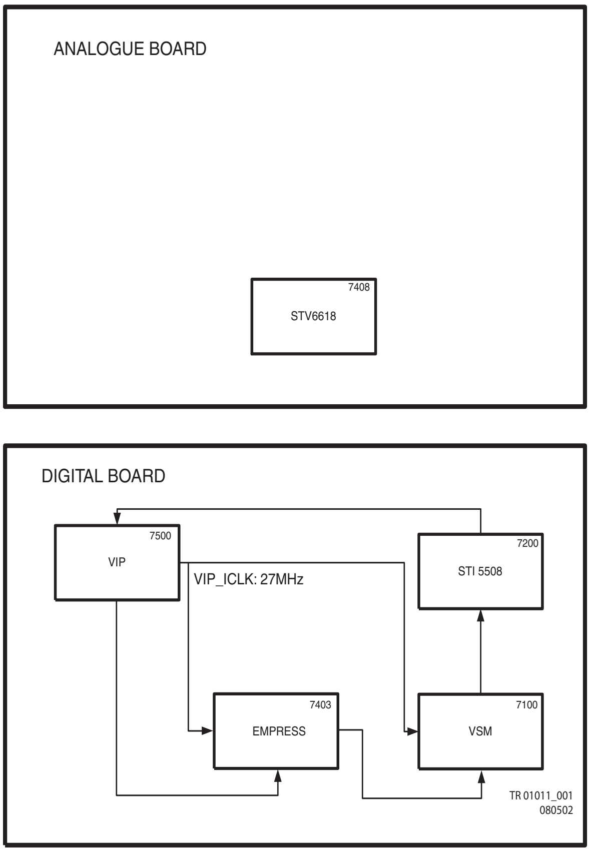

ANALOGUE BOARD
7408
STV6618
DIGITAL BOARD
7500
VIP
VIP_ICLK: 27MHz
7200
STI 5508
7403
EMPRESS
7100
VSM
TR 01011_001
080502

Figure 5-12

5.5.5 Nucleus 904: System Video Loop

Nucleus for testing the components on the video signal system path:

- The VIP
- The video encoder
- The VSM
- The host decoder
- The analogue board

On the analogue board the video signal will be routed to the SCART (EUROPE) or CINCH (NAFTA). There it will be looped back externally by means of the proper cable

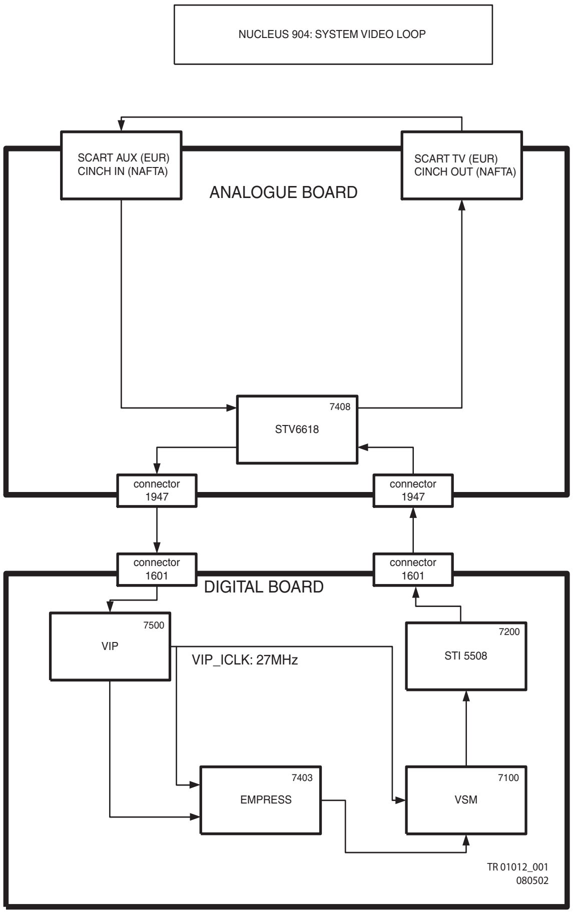

NUCLEUS 904: SYSTEM VIDEO LOOP
SCART AUX (EUR)
CINCH IN (NAFTA)
SCART TV (EUR)
CINCH OUT (NAFTA)
ANALOGUE BOARD
7408
STV6618
connector
1947
connector
1947
connector
1601
connector
1601
DIGITAL BOARD
7500
VIP
VIP_ICLK: 27MHz
7200
STI 5508
7403
EMPRESS
7100
VSM
TR 01012_001
080502

Figure 5-13

5.5.6 Nucleus 905: System Video VBI Loop

This nucleus tests the components on the video signal path:

- The VIP
- The VSM
- The Host Decoder

The video CVBS signal is routed to the output of the analogue board where it will be looped back by means of an external cable

Remark: this test is only successful if nucleus 121 is carried out first.

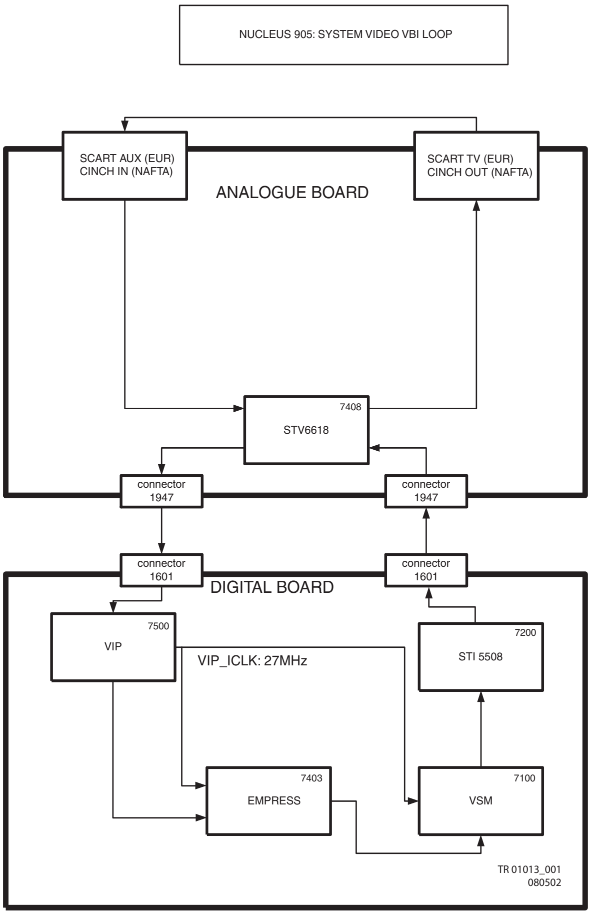

NUCLEUS 905: SYSTEM VIDEO VBI LOOP
SCART AUX (EUR)
CINCH IN (NAFTA)
SCART TV (EUR)
CINCH OUT (NAFTA)
ANALOGUE BOARD
7408
STV6618
connector
1947
connector
1947
connector
1601
connector
1601
DIGITAL BOARD
7500
VIP
VIP_ICLK: 27MHz
7200
STI 5508
7403
EMPRESS
7100
VSM
TR 01013_001
080502

Figure 5-14

5.5.7 Nucleus 906: Video User Dealer Loop

Nucleus for testing the components on the video signal system path:

- The VIP
- The video encoder
- The VSM
- The host decoder
- The analogue board

On the analogue board, the video signal is internally routed back to the digital board.

NUCLEUS 906: VIDEO USER DEALER LOOP

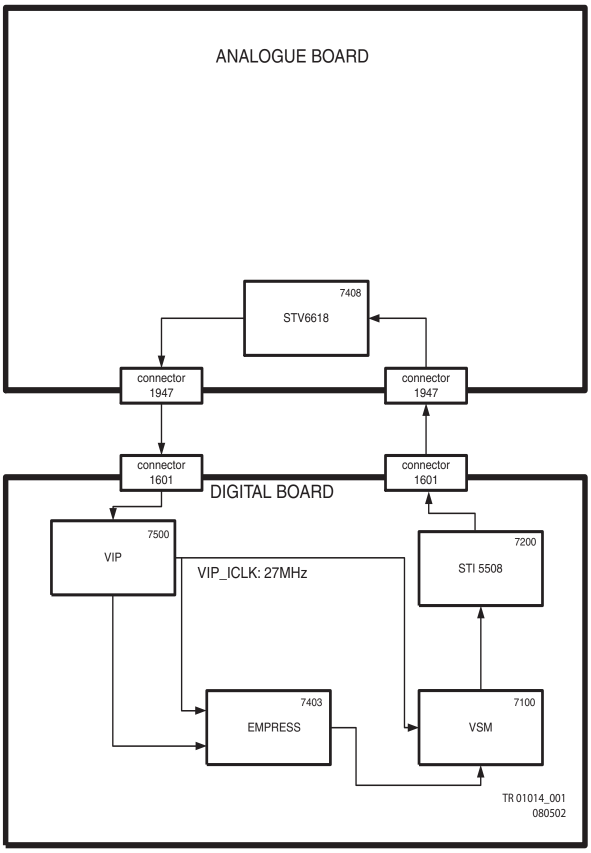

ANALOGUE BOARD
7408
STV6618
connector 1947
connector 1947
connector 1601
connector 1601
DIGITAL BOARD
7500
VIP
VIP_ICLK: 27MHz
7200
STI 5508
7403
EMPRESS
7100
VSM
TR 01014_001
080502

Figure 5-15

5.5.8 Nucleus 907: Video VBI User Dealer Loop

This nucleus tests the components on the video VBI signal path:

- The VIP
- The VSM
- The Host Decoder

The signal is routed back internally on the analogue board Remark: this test is only successful if nucleus 121 is carried out first.

NUCLEUS 907: VIDEO VBI USER DEALER LOOP

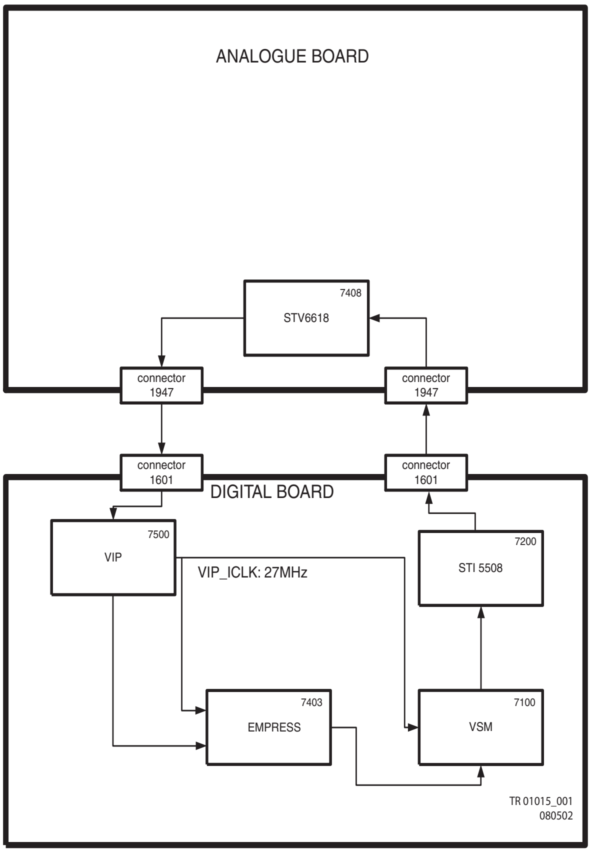

ANALOGUE BOARD
7408
STV6618
connector 1947
connector 1947
connector 1601
connector 1601
DIGITAL BOARD
7500
VIP
VIP_ICLK: 27MHz
7200
STI 5508
7403
EMPRESS
7100
VSM
TR 01015_001
080502

Figure 5-16

5.5.9 Nucleus 908: System Audio Loop Scart (Europe)

Nucleus for testing the components on the audio signal path:

- The hostdecoder
- The analogue board
- The audio encoder
- The VSM

On the analogue board, audio is passed to the SCART connector, where a SCART cable needs to be used to loop back the audio signal to the digital board

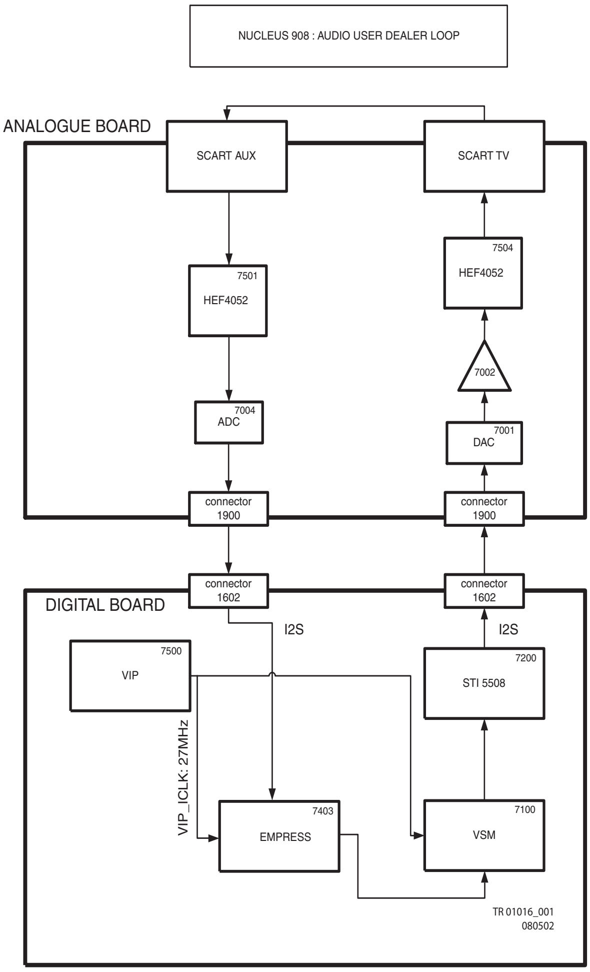

NUCLEUS 908 : AUDIO USER DEALER LOOP
ANALOGUE BOARD
SCART AUX
SCART TV
7504
HEF4052
7501
HEF4052
7002
7004
ADC
7001
DAC
connector 1900
connector 1900
connector 1602
connector 1602
DIGITAL BOARD
I2S
I2S
7500
VIP
7200
STI 5508
VIP_ICLK: 27MHz
7403
EMPRESS
7100
VSM
TR 01016_001 080502

Figure 5-17

5.5.10 Nucleus 909: System Audio Loop CINCH (Nafta)

Nucleus for testing the components on the audio signal path:

- The hostdecoder
- The analogue board
- The audio encoder
- The VSM

A parameter has to be specified to select the appropriate output routing. This parameter is identical to nucleus 713.

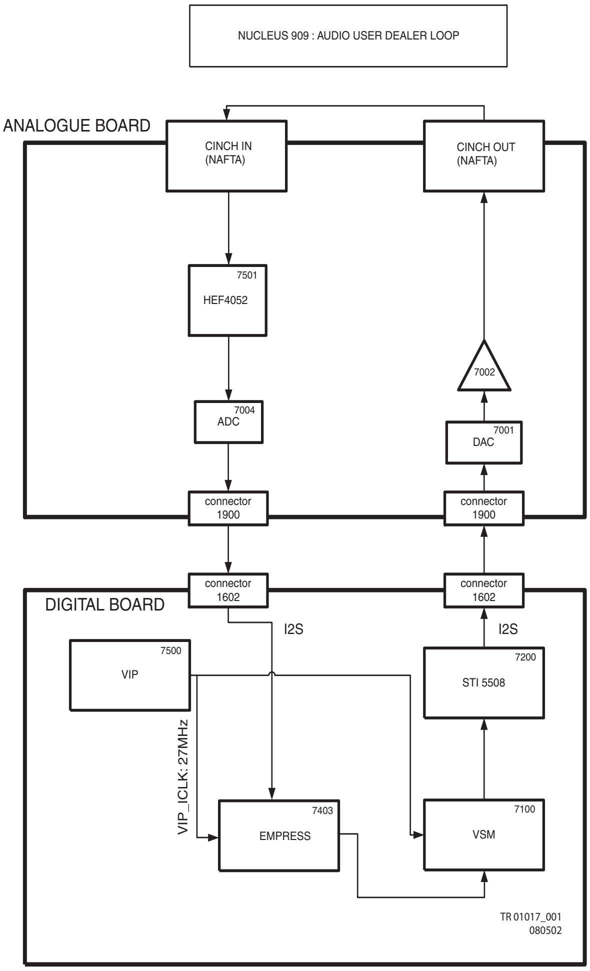

NUCLEUS 909 : AUDIO USER DEALER LOOP
ANALOGUE BOARD
CINCH IN (NAFTA)
CINCH OUT (NAFTA)
7501
HEF4052
7002
7004
ADC
7001
DAC
connector 1900
connector 1900
connector 1602
connector 1602
DIGITAL BOARD
I2S
I2S
7500
VIP
7200
STI 5508
VIP_ICLK: 27MHz
7403
EMPRESS
7100
VSM
TR 01017_001 080502

Figure 5-18

5.5.11 Nucleus 910: DVIO Video Input

Nucleus for testing the components on the video signal path:

- The DVIO board
- The VIP
- The video encoder
- The VSM
- The host decoder

Note :This Test is not valid for Nafta in DVDR-Lead. For Europe the sound will be available on scart 2.

5.5.12 Nucleus 911: DVIO Video VIP

Nucleus for testing the components on the video signal system path:

- The host decoder
- The analogue board
- The VIP

On the analogue board the video signal will be routed according to the parameter. There it will be looped back externally by means of the proper cable.

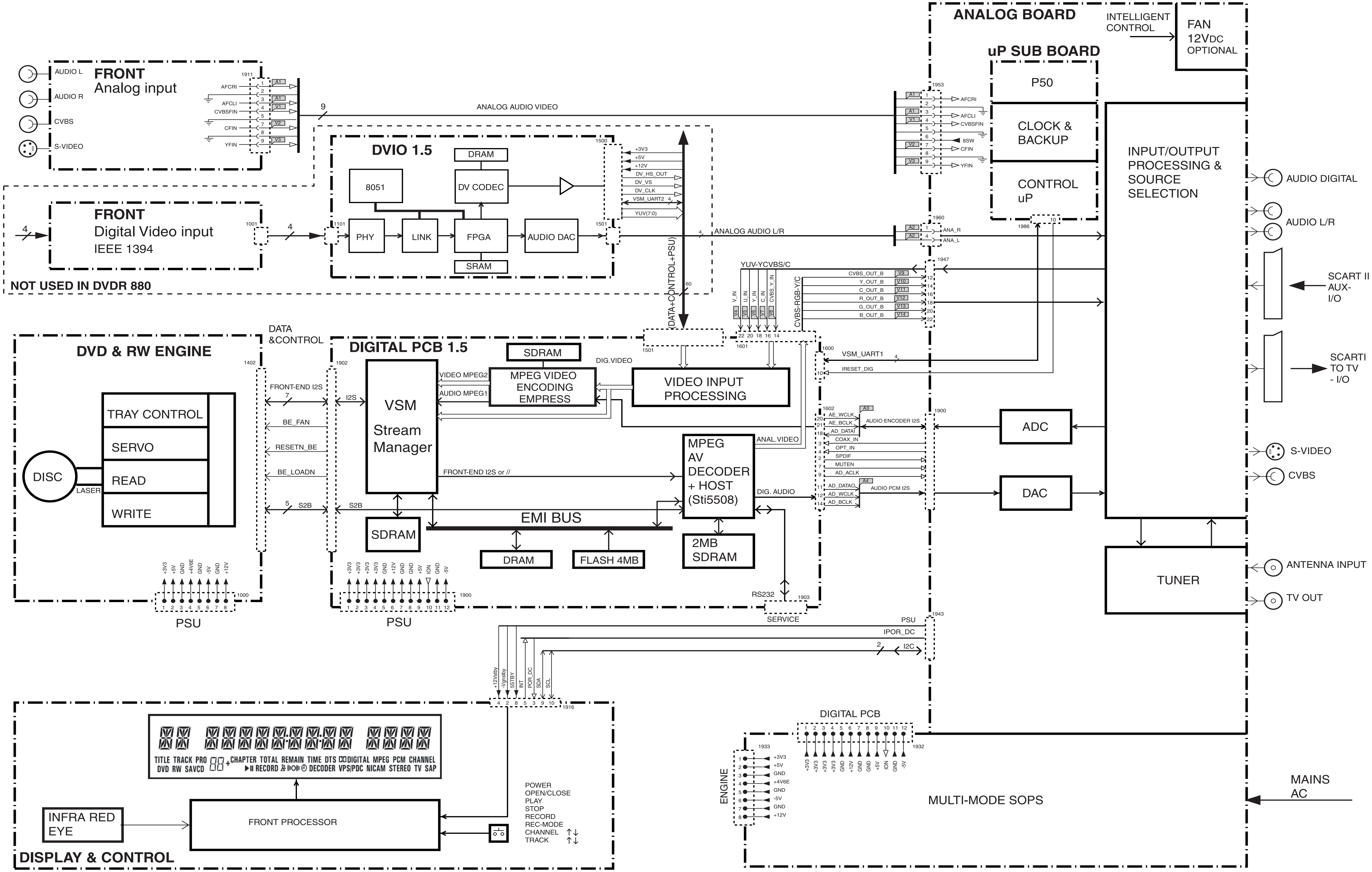
The correct Routing path has to be selected by a parameter:

Analog board Version	Selectable parameter	Internal call to nucleus 712
01	1	712.21
11	1	712.21
31	2	712.17
31	3	721.18
31	3	712.19
41	2	712.17
41	3	712.18
41	4	712.19
41	5	712.20
71	4	712.19

Remark: Nucleus 704 gives the analog board version

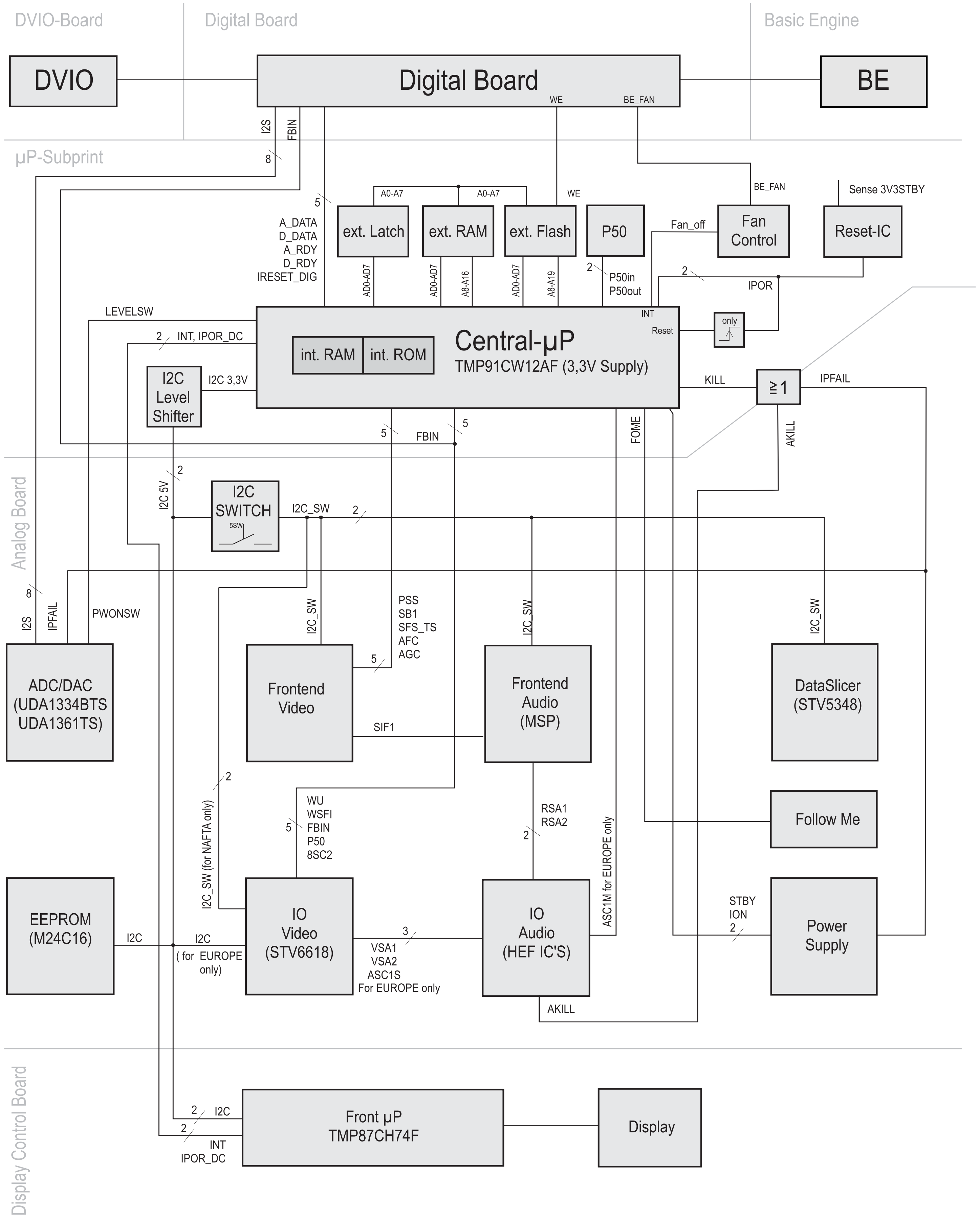
6. Block Diagrams, Waveforms, Wiring Diagram.

BLOCK DIAGRAM DVDR880, DVDR890 EURO


FRONT
Analog input
AUDIO L
AUDIO R
CVBS
S-VIDEO
AFCRI
AFCLI
CVBSFIN
CFIN
YFIN
1911
9
ANALOG AUDIO VIDEO
FRONT
Digital Video input
IEEE 1394
NOT USED IN DVDR 880
DVIO 1.5
8051
DRAM
DV CODEC
PHY
LINK
FPGA
SRAM
AUDIO DAC
+3V3
+5V
+12V
DV_HS_OUT
DV_VS
DV_CLK
VSM_UART2
YUV(7:0)
1500
1501
ANALOG AUDIO L/R
(DATA+CONTROL+PSU)
ANALOG BOARD
INTELLIGENT CONTROL
FAN
12VDC
OPTIONAL
uP SUB BOARD
P50
CLOCK & BACKUP
CONTROL uP
INPUT/OUTPUT PROCESSING & SOURCE SELECTION
1953
AFCRI
AFCLI
CVBSFIN
8SW
CFIN
YFIN
1960
ANA_R
ANA_L
1986
1947
YUV-YCVBS/C
CVBS_OUT_B
Y_OUT_B
C_OUT_B
R_OUT_B
G_OUT_B
B_OUT_B
CVBS-RGB-Y/C
V_IN
U_IN
Y_IN
C_IN
CVBS_Y_IN
AUDIO DIGITAL
AUDIO L/R
SCART II AUX-I/O
SCARTI TO TV - I/O
S-VIDEO
CVBS
ANTENNA INPUT
TV OUT
TUNER
ADC
DAC
DVD & RW ENGINE
TRAY CONTROL
SERVO
READ
WRITE
DISC
LASER
DATA &CONTROL
FRONT-END I2S
BE_FAN
RESETN_BE
BE_LOADN
S2B
DIGITAL PCB 1.5
VSM
Stream Manager
SDRAM
MPEG VIDEO ENCODING EMPRESS
VIDEO MPEG2
AUDIO MPEG1
DIG.VIDEO
VIDEO INPUT PROCESSING
VSM_UART1
IRESET_DIG
MPEG AV DECODER + HOST (Sti5508)
ANAL.VIDEO
DIG. AUDIO
FRONT-END I2S or //
AE_WCLK
AE_BCLK
AD_DATAI
COAX_IN
OPT_IN
SPDIF
MUTEN
AD_ACLK
AD_DATAO
AD_WCLK
AD_BCLK
AUDIO ENCODER I2S
AUDIO PCM I2S
1600
1602
1900
EMI BUS
SDRAM
DRAM
FLASH 4MB
2MB SDRAM
RS232
1903
SERVICE
PSU
PSU
1000
1900
PSU
IPOR_DC
I2C
1943
+12Vstby
-Vgrstby
5STBY
INT
POR_DC
SDA
SCL
1916
DIGITAL PCB
1933
1932
ENGINE
+3V3
+5V
GND
+4V6E
-5V
+12V
MULTI-MODE SOPS
MAINS AC
TITLE TRACK PRO DVD RW SAVCD CHAPTER TOTAL REMAIN TIME DTS DIGITAL MPEG PCM CHANNEL RECORD DECODER VPS/PDC NICAM STEREO TV SAP
INFRA RED EYE
FRONT PROCESSOR
POWER
OPEN/CLOSE
PLAY
STOP
RECORD
REC-MODE
CHANNEL
TRACK
DISPLAY & CONTROL

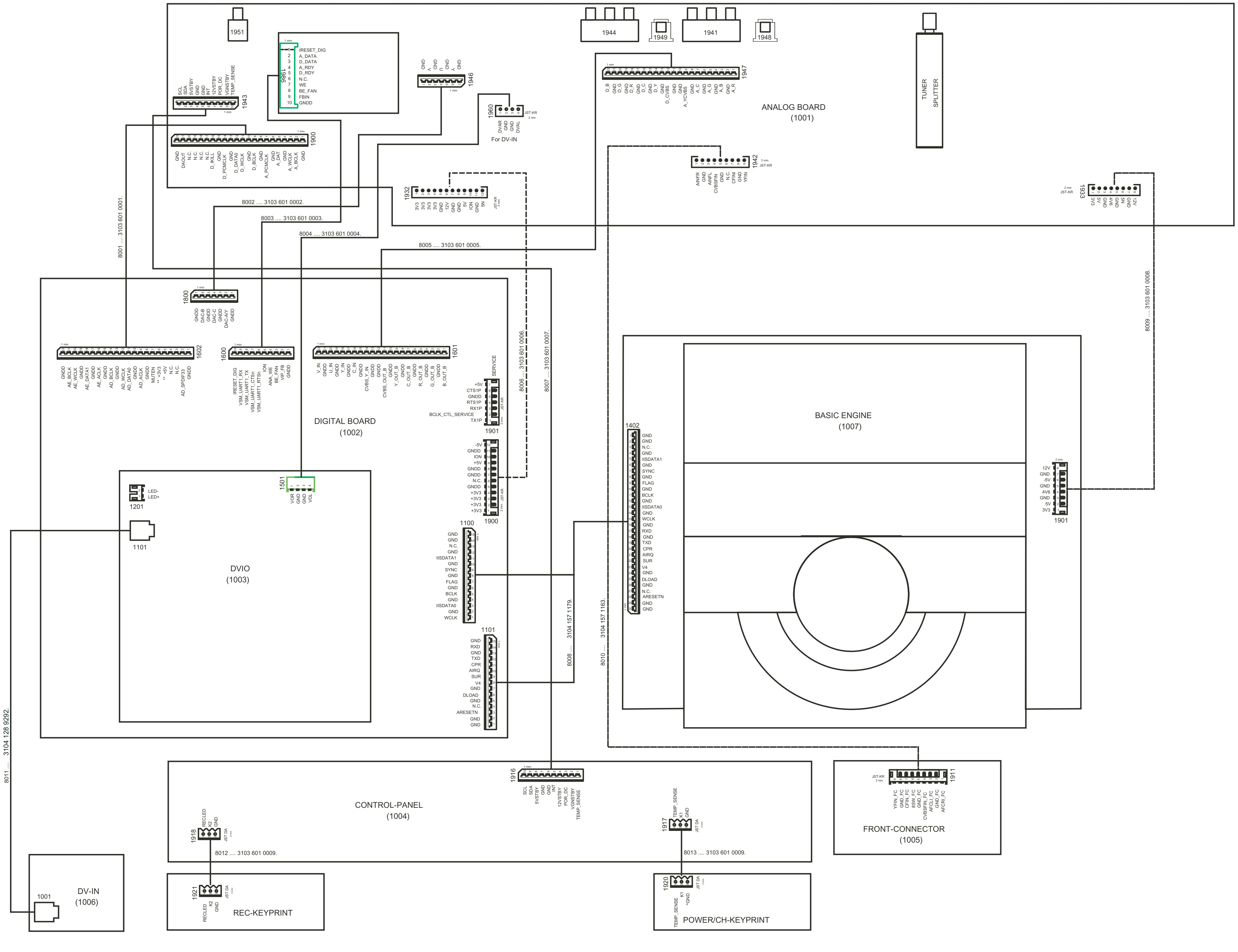
TR 01018_001
130502

Blockdiagram Control Lines and Bus Systems


DVIO-Board
Digital Board
Basic Engine
DVIO
Digital Board
BE
WE
BE_FAN
I2S
FBIN
8
µP-Subprint
5
A_DATA
D_DATA
A_RDY
D_RDY
IRESET_DIG
A0-A7
A0-A7
WE
BE_FAN
Sense 3V3STBY
ext. Latch
ext. RAM
ext. Flash
P50
Fan_off
Fan Control
Reset-IC
AD0-AD7
AD0-AD7
A8-A16
AD0-AD7
A8-A19
2
P50in
P50out
2
IPOR
LEVELSW
INT
Reset
only
2
INT, IPOR_DC
int. RAM
int. ROM
Central-µP
TMP91CW12AF (3,3V Supply)
I2C Level Shifter
I2C 3,3V
KILL
≧1
IPFAIL
FOME
AKILL
5
5
FBIN
2
I2C 5V
I2C SWITCH
5SW
I2C_SW
2
Analog Board
8
I2S
IPFAIL
PWONSW
I2C_SW
PSS
SB1
SFS_TS
AFC
AGC
5
I2C_SW
I2C_SW
ADC/DAC (UDA1334BTS UDA1361TS)
Frontend Video
Frontend Audio (MSP)
DataSlicer (STV5348)
SIF1
2
I2C_SW (for NAFTA only)
WU
WSFI
FBIN
P50
8SC2
5
RSA1
RSA2
2
ASC1M for EUROPE only
Follow Me
STBY
ION
2
EEPROM (M24C16)
I2C
I2C
(for EUROPE only)
IO Video (STV6618)
3
VSA1
VSA2
ASC1S
For EUROPE only
IO Audio (HEF IC'S)
AKILL
Power Supply
Display Control Board
2
I2C
2
INT
IPOR_DC
Front µP TMP87CH74F
Display

TR 01019_001
130502

Wiring Diagram

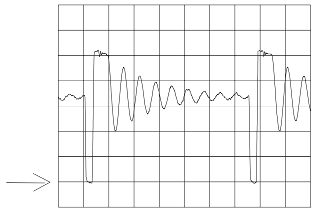

ANALOG BOARD
(1001)
1951
1944
1949
1941
1948
TUNER
SPLITTER
1986
1 mm
1 IRESET_DIG
2 A_DATA
3 D_DATA
4 A_RDY
5 D_RDY
6 N.C.
7 WE
8 BE_FAN
9 FBIN
10 GNDD
1943
SCL
SDA
5VSTBY
GND
GND
INT
12VSTBY
POR_DC
VGNSTBY
TEMP_SENSE
1900
GND
DAOUT
N.C.
N.C.
N.C.
N.C.
D_IKILL
GND
D_PCMCLK
GND
D_DATA0
D_WCLK
GND
D_BCLK
GND
A_PCMCLK
GND
A_DAT
GND
A_WCLK
A_BCLK
GND
1946
GND
V
GND
U
GND
Y
GND
1960
JST-KR
2 mm
DVAR
GND
GND
DVAL
For DV-IN
1947
D_B
GND
D_G
GND
D_R
GND
D_C
GND
D_Y
GND
D_CVBS
GND
GND
A_YCVBS
GND
A_C
GND
A_G
GND
A_B
GND
A_R
1942
JST-KR
AINFR
GND
AINFL
CVBSFIN
GND
N.C.
CFINI
GND
YFIN
1932
JST-KR
3V3
3V3
3V3
3V3
GND
12V
GND
GND
5V
ION
GND
5N
1933
JST-KR
3V3
5V
GND
4V6
GND
5N
GND
12V
8001 .... 3103 601 0001.
8002 .... 3103 601 0002.
8003 .... 3103 601 0003.
8004 .... 3103 601 0004.
8005 .... 3103 601 0005.
8006 .... 3103 601 0006.
8007 .... 3103 601 0007.
8008 .... 3104 157 1179.
8009 .... 3103 601 0008.
8010 .... 3104 157 1163.
8011 .... 3104 128 9292.
8012 .... 3103 601 0009.
8013 .... 3103 601 0009.
DIGITAL BOARD
(1002)
1800
GNDD
DAC-B
GNDD
DAC-C
GNDD
DAC-A/Y
GNDD
1602
GNDD
AE_BCLK
AE_WCLK
GNDD
AE_DATA1
GNDD
AE_ACLK
GNDD
AD_BCLK
GNDD
AD_WCLK
AD_DATA0
GNDD
AD_ACLK
GNDD
MUTEN
** +3V3
** +5V
N.C.
N.C.
AD_SPDIF33
GNDD
1600
IRESET_DIG
VSM_UART1_RX
VSM_UART1_TX
VSM_UART1_CTSn
VSM_UART1_RTSn
ION
ANA_WE
BE_FAN
VIP_FB
GNDD
1601
V_IN
GNDD
U_IN
GNDD
Y_IN
GNDD
C_IN
GNDD
CVBS_Y_IN
GNDD
GNDD
CVBS_OUT_B
GNDD
Y_OUT_B
GNDD
C_OUT_B
GNDD
R_OUT_B
GNDD
G_OUT_B
GNDD
B_OUT_B
SERVICE
1901
JST-KR
+5V
CTS1P
GNDD
RTS1P
RX1P
BCLK_CTL_SERVICE
TX1P
1900
-5V
GNDD
ION
+5V
GNDD
GNDD
N.C.
GNDD
+3V3
+3V3
+3V3
+3V3
1100
GND
GND
N.C.
GND
IISDATA1
GND
SYNC
GND
FLAG
GND
BCLK
GND
IISDATA0
GND
WCLK
1101
GND
RXD
GND
TXD
CPR
AIRQ
SUR
V4
GND
DLOAD
GND
N.C.
ARESETN
GND
GND
DVIO
(1003)
1201
LED-
LED+
1101
1501
VOR
GND
GND
VOL
BASIC ENGINE
(1007)
1402
GND
GND
N.C.
GND
IISDATA1
GND
SYNC
GND
FLAG
GND
BCLK
GND
IISDATA0
GND
WCLK
GND
RXD
GND
TXD
CPR
AIRQ
SUR
V4
GND
DLOAD
GND
N.C.
ARESETN
GND
GND
1901
2 mm
12V
GND
-5V
GND
4V6
GND
5V
3V3
CONTROL-PANEL
(1004)
1916
SCL
SDA
5VSTBY
GND
GND
INT
12VSTBY
POR_DC
VGNSTBY
TEMP_SENSE
1918
RECLED
K2
GND
JST DA
1917
TEMP_SENSE
K1
GND
JST DA
FRONT-CONNECTOR
(1005)
1911
JST-KR
YFIN_FC
GND_FC
CFIN_FC
8SW_FC
GND_FC
CVBSFIN_FC
AFCLI_FC
GND_FC
AFCRI_FC
DV-IN
(1006)
1001
REC-KEYPRINT
1921
RECLED
K2
GND
JST DA
POWER/CH-KEYPRINT
1920
TEMP_SENSE
K1
^GND
JST DA

TR 01020_001
150502

Waveforms

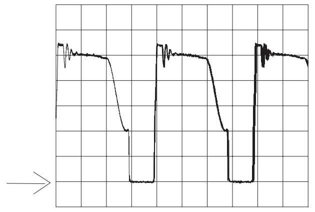
Waveforms Analog Board, uPC Sub PWB

F327 VDrain (Standby)



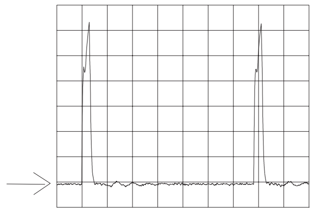
A: DC, 100V/Div
5us/Div

F327 VDrain (no disc loaded)



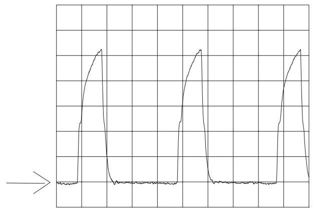
A: DC, 100V/Div
2us/Div

I324 VDrain (Standby)



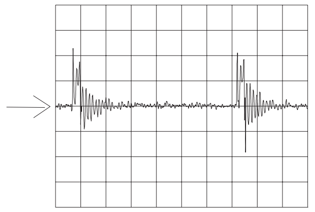
A: DC, 1V/Div
5us/Div

I324 VGate (no disc loaded)



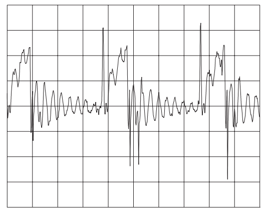
A: DC, 2V/Div
2us/Div

I325 VSource (Standby)



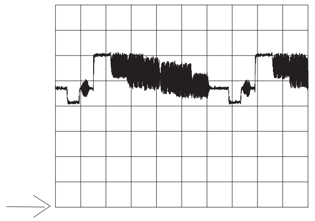
A: DC, 50mV/Div
5us/Div

I325 VSource (no disc loaded)



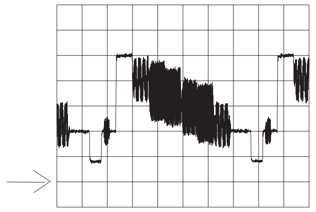
A: DC, 50mV/Div
2us/Div

VFV I723



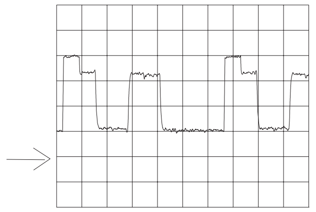
A: DC, 500mV/Div
10us/Div

I465



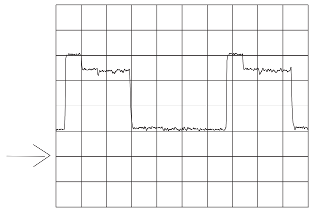
A: DC, 500mV/Div
10us/Div

I461



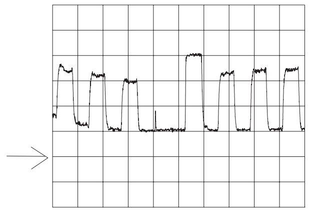
A: DC, 500mV/Div
10us/Div

I462



A: DC, 500mV/Div
10us/Div

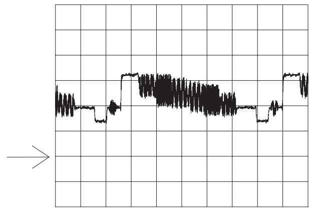
I463



A: DC, 500mV/Div
10us/Div

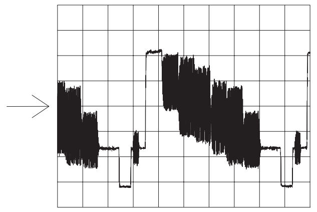
Waveforms Analog Board, uPC Sub PWB

A_CVBS I405



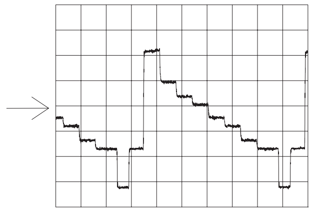
A: DC, 500mV/Div
10us/Div

D_CVBS F4712



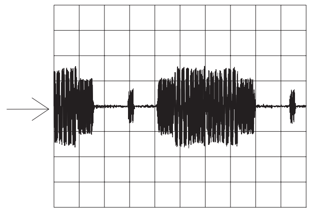
A: DC, 200mV/Div
10us/Div

D_Y F4714



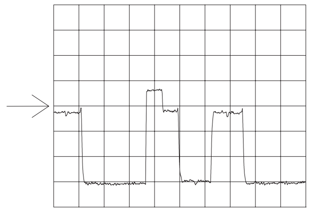
A: DC, 200mV/Div
10us/Div

D_C F4716



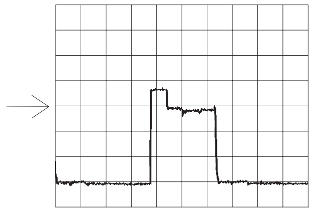
A: DC, 200mV/Div
10us/Div

D_R F4718



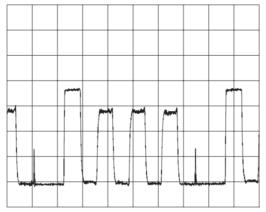
A: DC, 200mV/Div
10us/Div

D_G F4720



A: DC, 200mV/Div
10us/Div

D_B F4722

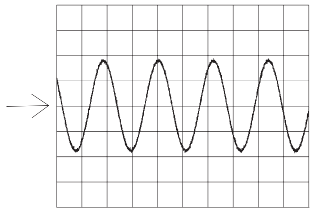


A: DC, 200mV/Div
10us/Div

TR 01021_001
150502

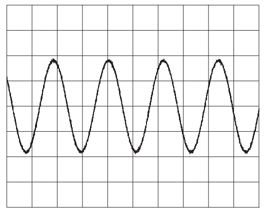
Waveforms Analog Board, uPC Sub PWB

I502/I504



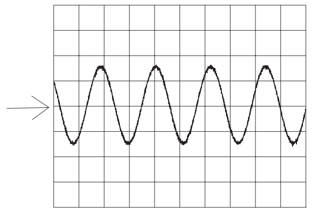
A: DC, 500mV/Div
500us/Div

I517/I518



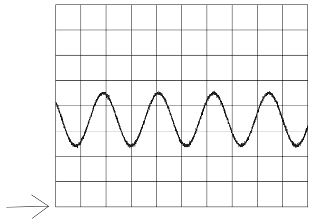
A: DC, 500mV/Div
500us/Div

F501/F502



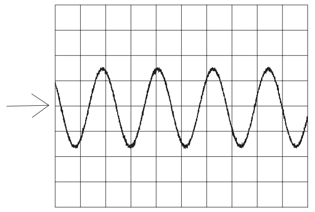
A: DC, 500mV/Div
500us/Div

I014/I032



A: DC, 500mV/Div
500us/Div

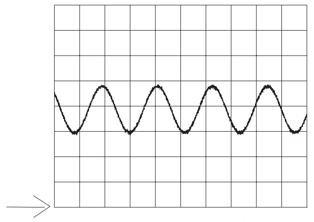
ARDAC/ALDAC F010/F011



A: DC, 500mV/Div
500us/Div

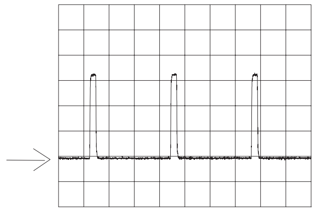
Waveforms Analog Board, uPC Sub PWB

I623



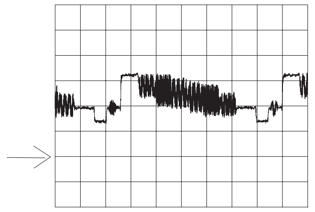
A: DC, 1 V/Div
500us/Div

SYNC F843



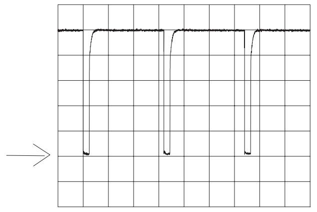
A: DC, 500mV/Div
10us/Div

A_CVBS F8008



A: DC, 500mV/Div
10us/Div

I818



A: DC, 1 V/Div
20us/Div

TR 01022_001
140502

Waveforms Digital Board

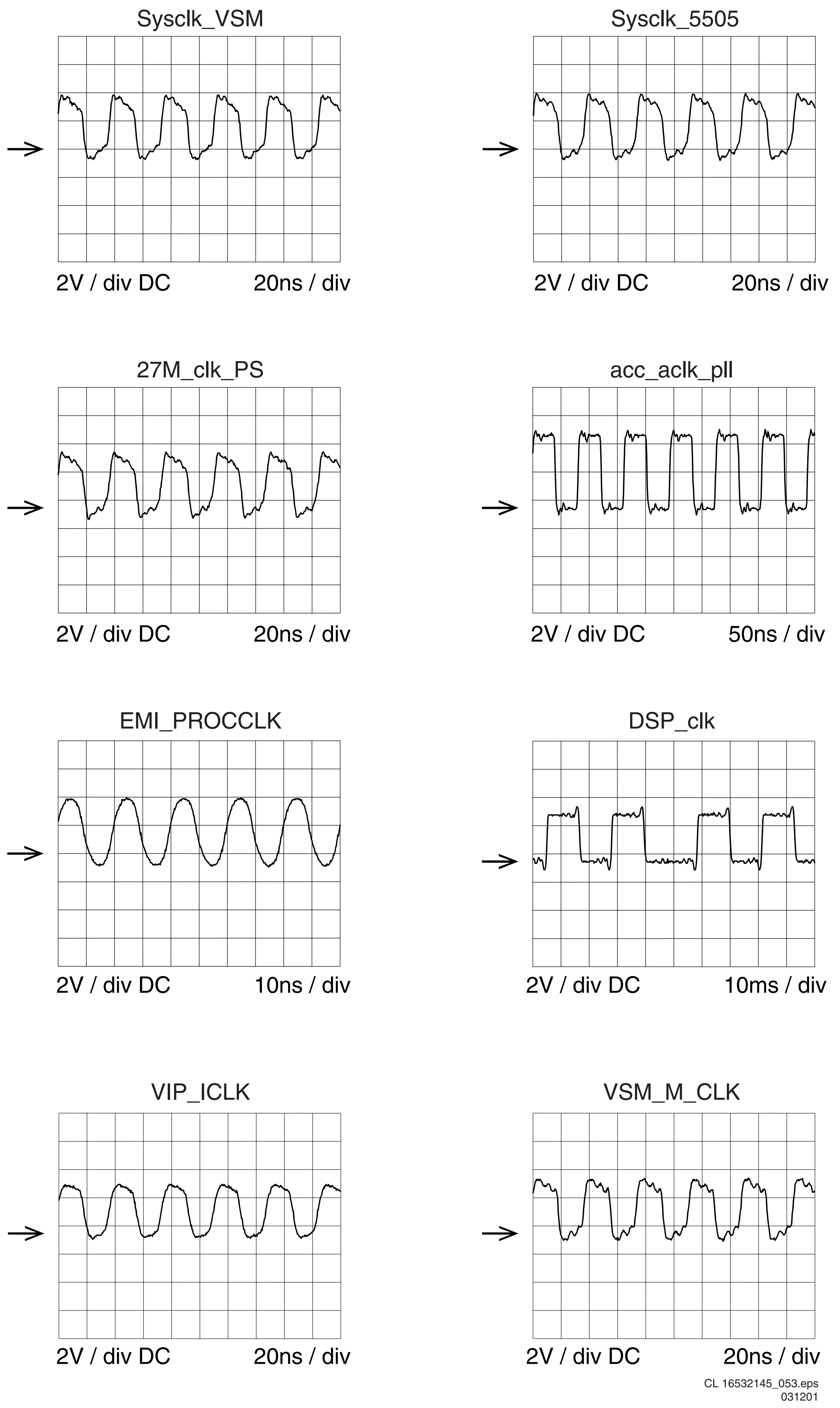


Figure 6-1

Waveforms Digital Board

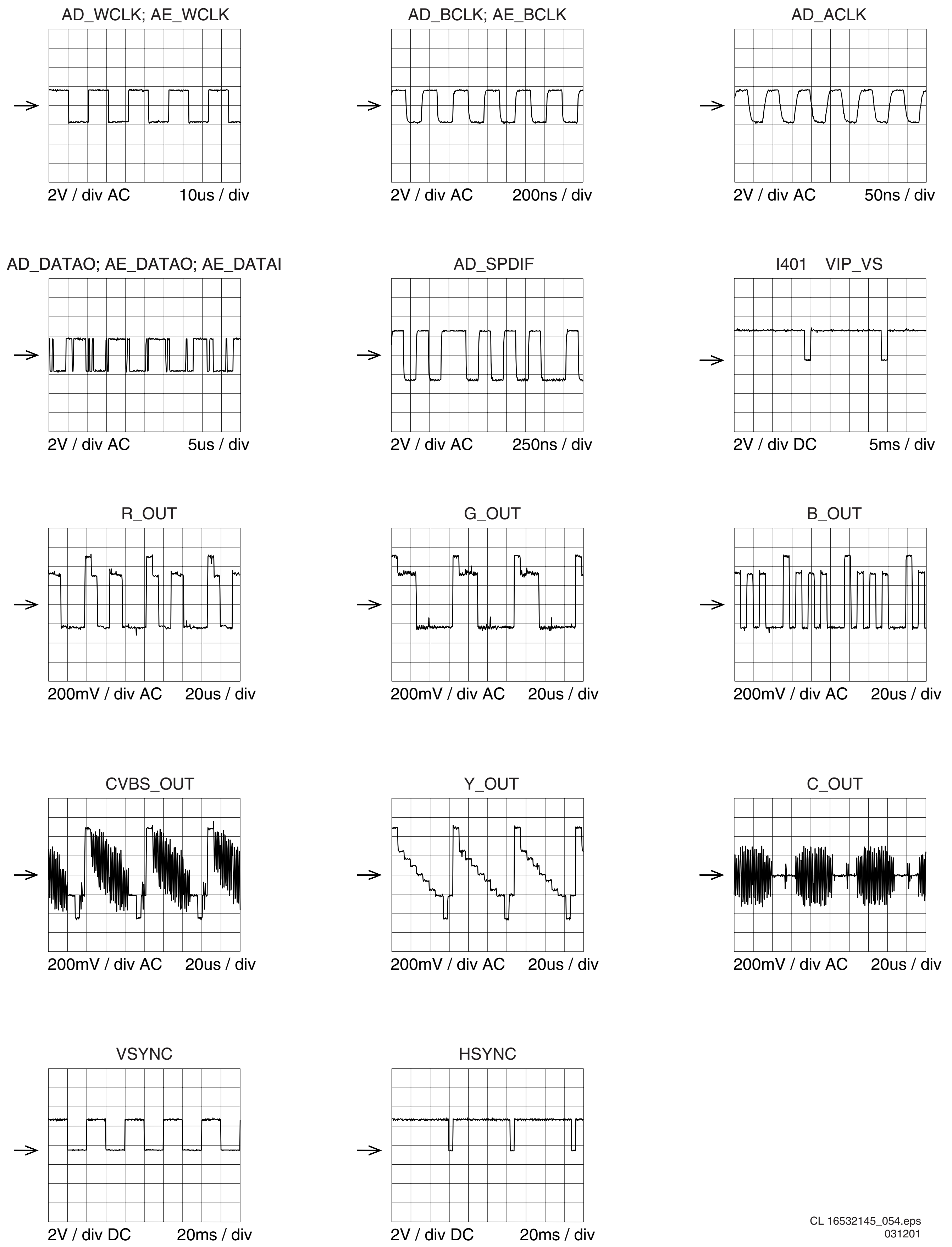
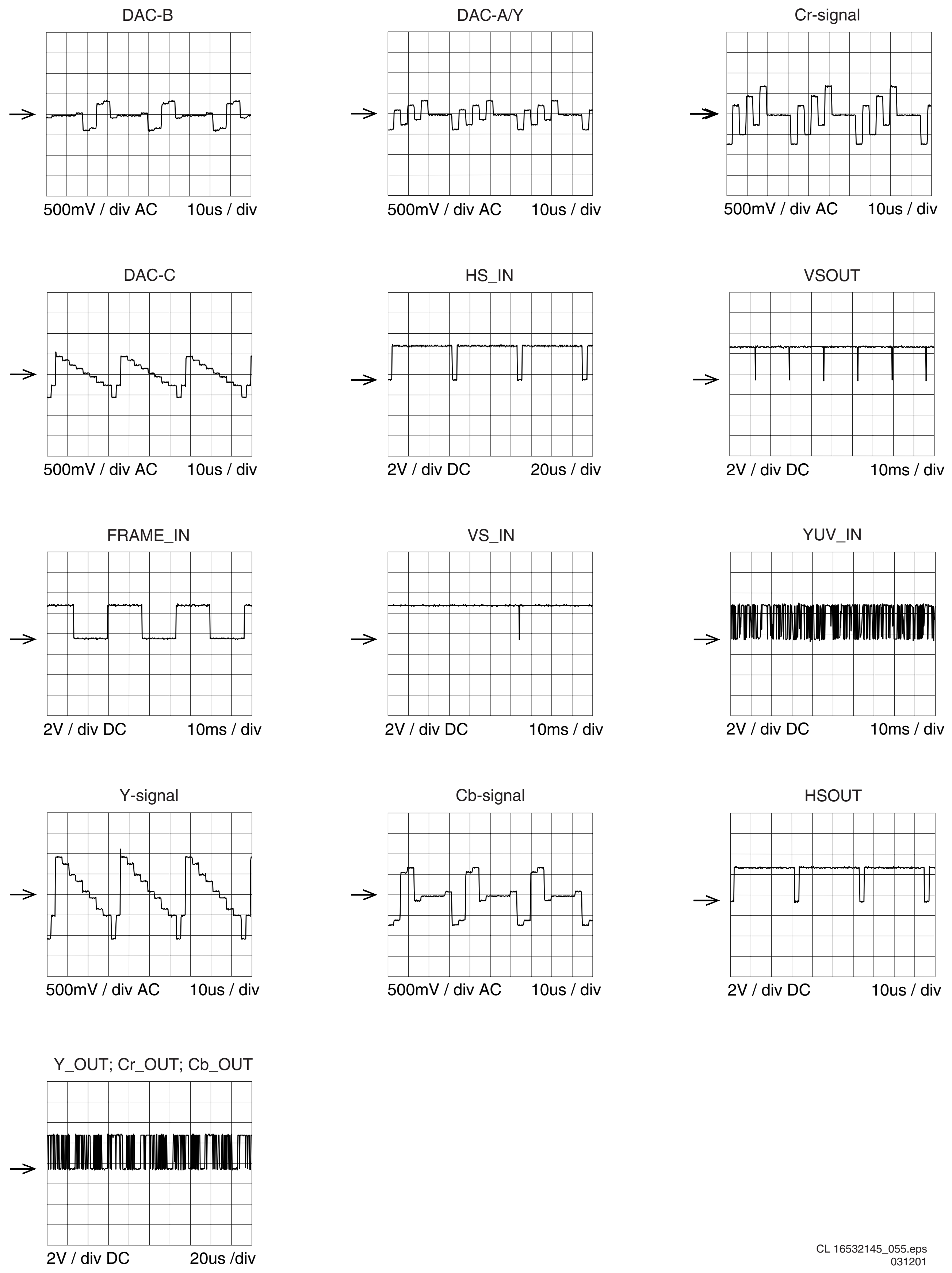


Figure 6-2

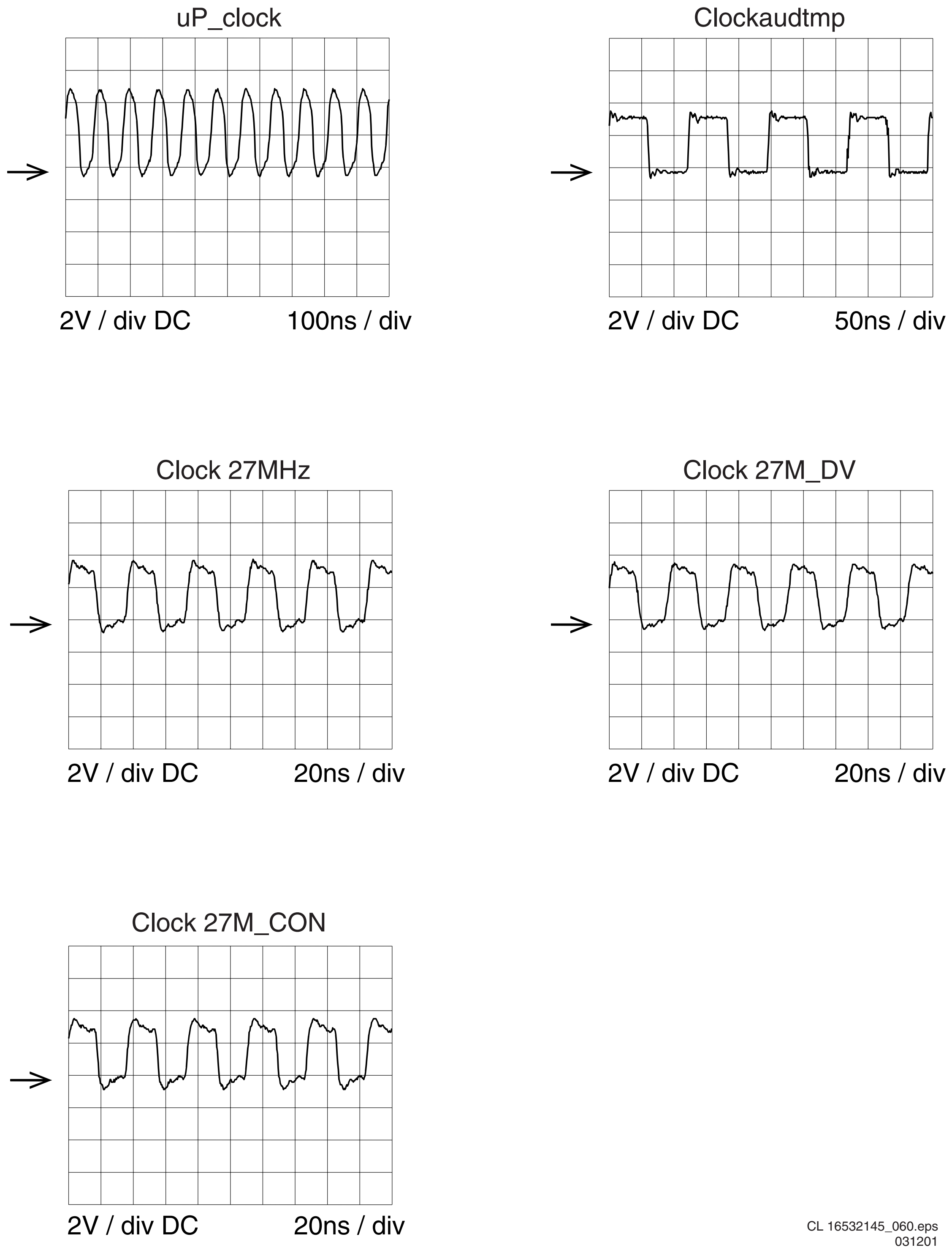
Waveforms Digital Board



CL 16532145_055.eps
031201

Figure 6-3

Waveforms DVIO



CL 16532145_060.eps
031201

Figure 6-4

Test points overview Analog Board

F0001	A10
F0002	C10
F0003	C9
F0005	C10
F0007	C9
F0009	C10
F0011	C10
F0012	C10
F0014	B10
F0016	C10
F0021	A10
F006	B9
F007	B9
F008	B9
F009	B9
F010	B9
F011	A10
F300	B3
F301	A3
F302	A4
F304	B1
F305	B2
F306	A1
F307	B1
F308	A2
F309	A2
F310	A2
F311	A2
F312	B1
F313	A1
F314	A1
F315	C1
F316	C2
F317	C4
F318	C3
F319	C2
F320	C1
F3205	C8
F321	B3
F322	B3
F323	B1
F324	B3
F325	A9
F326	B2
F327	C3
F328	B1
F329	B1
F331	A3
F333	B4
F334	A2
F335	A2
F336	A2
F337	A3
F338	B1
F339	B1
F340	A2
F341	A10
F342	C1
F344	A10
F345	C9
F346	B3
F347	A4
F348	C9
F349	B3
F350	C3
F351	B3
F352	C3
F353	C3
F354	A3
F355	A2
F356	C3
F357	C3
F358	B5
F359	B9
F360	C3
F361	C2
F362	B2
F363	B2
F364	B2
F365	A2
F366	A2
F367	A2
F368	A3
F371	B9
F372	A10
F373	A3
F374	A3
F401	A9
F402	A9
F4101	A5
F4102	A5
F4103	A5
F4104	A6
F4106	A5
F4107	A5
F4109	A5
F4110	A6
F4111	A5
F4201	C6
F4203	B7
F4206	C6
F4207	C5
F4209	C5
F422	C9
F4305	A10
F4402	A7
F4403	A7
F4404	A7
F4406	A7
F4407	A7
F4408	A7
F4409	A7
F4410	A8
F4411	A7
F4504	A9
F4505	A9
F4506	A9
F4511	A8
F4518	C9
F4523	C9
F4525	C9
F4707	B7
F4709	A9
F4712	B7
F4714	B6
F4716	B6
F4718	B6
F4720	B6
F4721	B6
F4722	B6
F4803	A4
F4804	A4
F4903	A6
F4904	A6
F499	A6
F5102	A9
F5103	A9
F6001	B6
F6002	B6
F6004	B6
F700	B3
F701	A3
I001	B10
I002	B10
I003	B10
I004	B10
I006	B10
I007	B10
I011	B10
I012	A10
I013	B9
I014	B10
I015	B9
I016	A10
I017	A10
I018	B10
I019	C10
I020	B9
I021	B10
I022	B9
I023	B9
I024	B9
I027	B10
I028	B9
I030	B9
I032	B10
I033	B10
I036	B9
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I301	A3
I303	B2
I304	B3
I305	B3
I306	A1
I307	C1
I308	B2
I309	A3
I310	C2
I311	B1
I312	B1
I313	B3
I314	A1
I315	A3
I316	A1
I317	A1
I318	C3
I319	C3
I320	C3
I321	B1
I322	B1
I323	A3
I324	B1
I325	B1
I327	A3
I329	A2
I330	C1
I331	C1
I332	B2
I333	A2
I334	A3
I335	C1
I336	A2
I337	A2
I338	A3
I339	A2
I340	C1
I343	C1
I344	C2
I345	A3
I346	A3
I347	B9
I348	C1
I349	B9
I350	C2
I351	C2
I352	B9
I353	A3
I354	C9
I355	C2
I356	A2
I357	A2
I361	A2
I401	A8
I402	A8
I403	A8
I404	A8
I405	A8
I410	A8
I411	C6
I412	C6
I413	C6
I414	A8
I415	C6
I416	B6
I417	C6
I418	A8
I419	A8
I420	A8
I421	A8
I428	A8
I449	B8
I450	B8
I451	A6
I453	A8
I454	A9
I456	B8
I457	B7
I461	B8
I462	B8
I463	B8
I466	B7
I467	C7
I468	C6
I469	B7
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I471	B8
I475	B8
I476	B8
I477	B7
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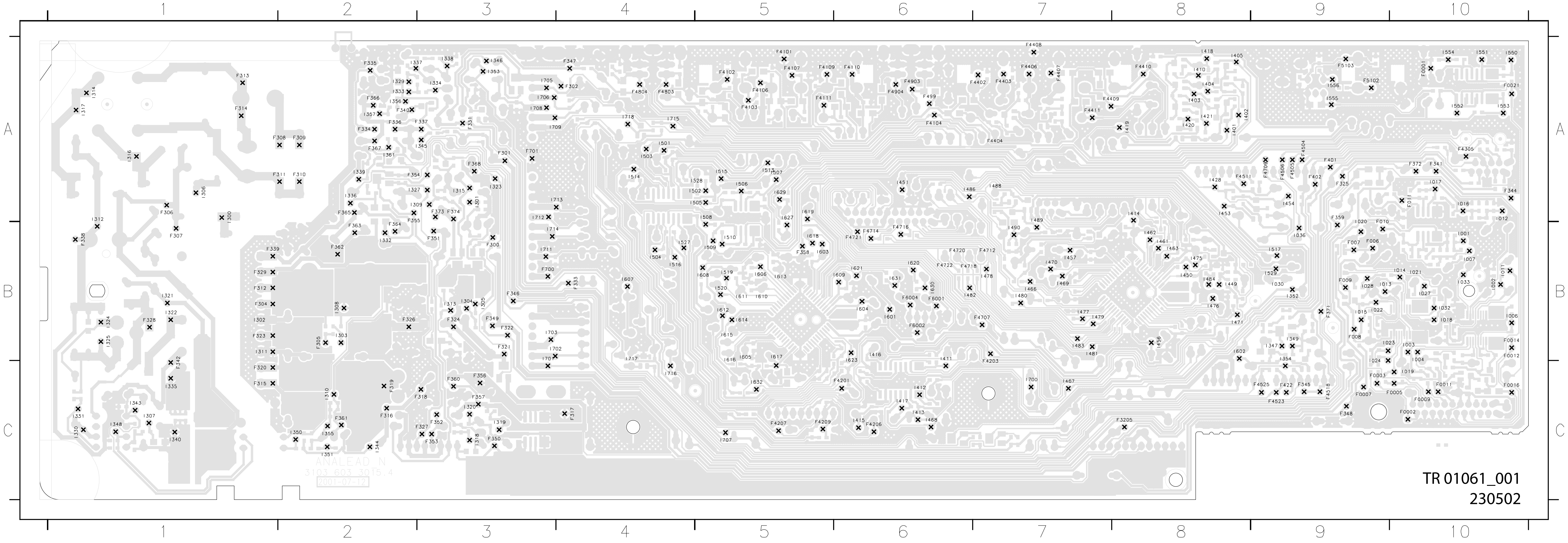
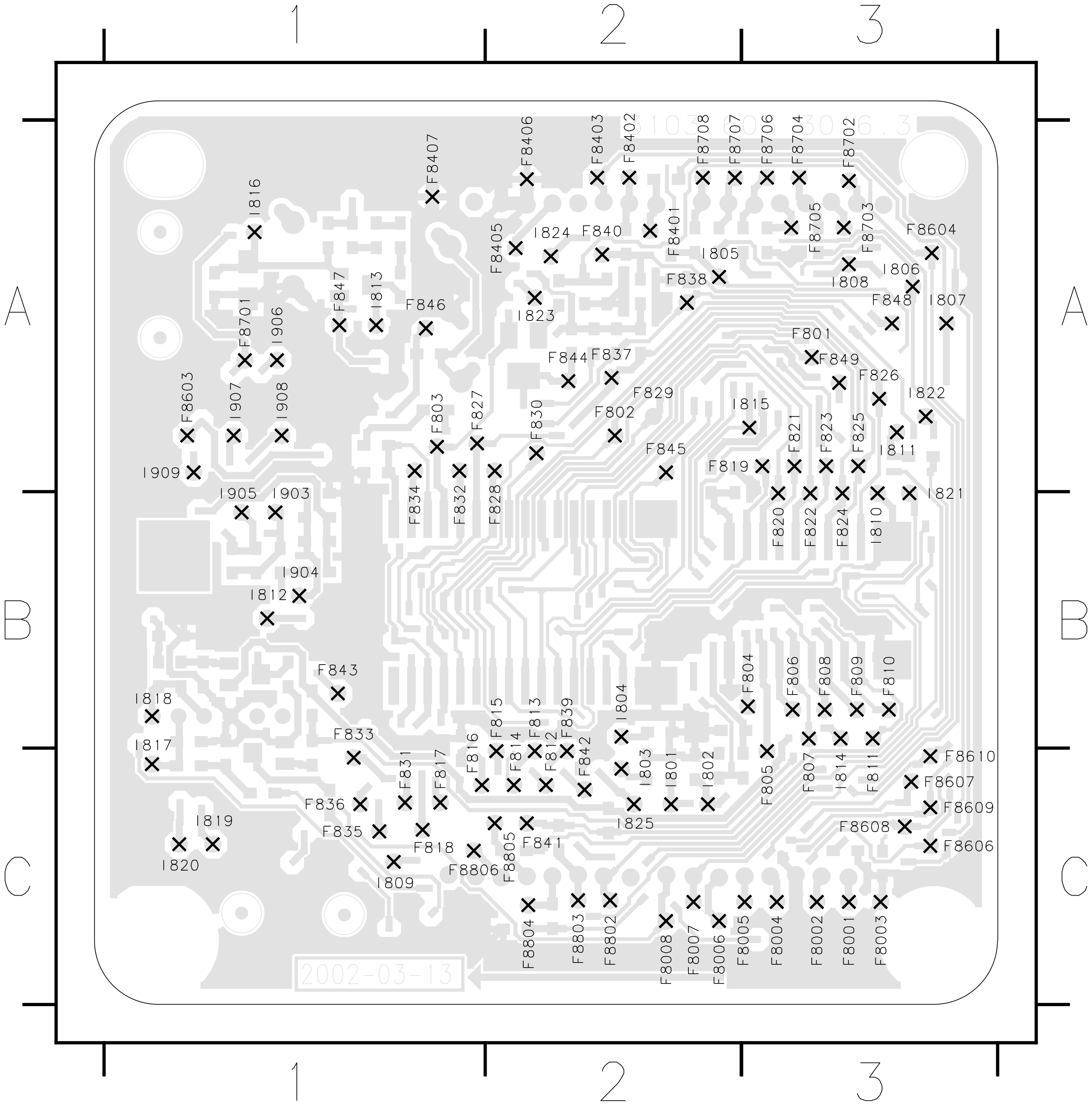
I482	B6
I483	B7
I484	B8
I486	A6
I488	A7
I489	B7
I490	B7
I501	A4
I502	A5
I503	A4
I504	B4
I505	A5
I506	A5
I507	A5
I508	B5
I509	B5
I510	B5
I513	A5
I514	A4
I515	A5
I516	B4
I517	B9
I519	B5
I520	B5
I527	B4
I528	A5
I529	B9
I550	A10
I551	A10
I552	A10
I553	A10
I554	A10
I555	A9
I556	A9
I601	B6
I602	B8
I603	B5
I604	B6
I605	B5
I606	B5
I607	B4
I608	B5
I609	B6
I610	B5
I611	B5
I612	B5
I613	B5
I614	B5
I615	B5
I616	B5
I617	C5
I618	B5
I619	A5
I620	B6
I621	B6
I623	B6
I627	B5
I629	A5
I630	B6
I631	B6
I632	C5
I700	C7
I701	C3
I702	B3
I703	B3
I705	A3
I706	A3
I707	C5
I708	A3
I709	A3
I711	B3
I712	A3
I713	A4
I714	B3
I715	A4
I716	C4
I717	C4
I718	A4



Test points overview UPC12 Sub PCB


1
2
3
A
B
C
1816
F8407
F8406
F8403
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F8707
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F8702
F8405
1824
F840
F8401
F8705
F8703
F8604
1805
1806
1808
F838
F848
1807
F847
1813
F846
1823
F8701
1906
F801
F849
F844
F837
F826
1822
F8603
1907
1908
F829
1815
F803
F827
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F802
F821
F823
F825
1811
F845
F819
1909
F834
F832
F828
1821
1905
1903
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F822
F824
1810
1904
1812
F843
F804
F806
F808
F809
F810
1818
F815
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F831
F817
1803
1801
1802
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1814
F811
F8610
F8607
F836
F8609
1819
F835
F818
F841
1825
F8608
F8606
1820
1809
F8806
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F8802
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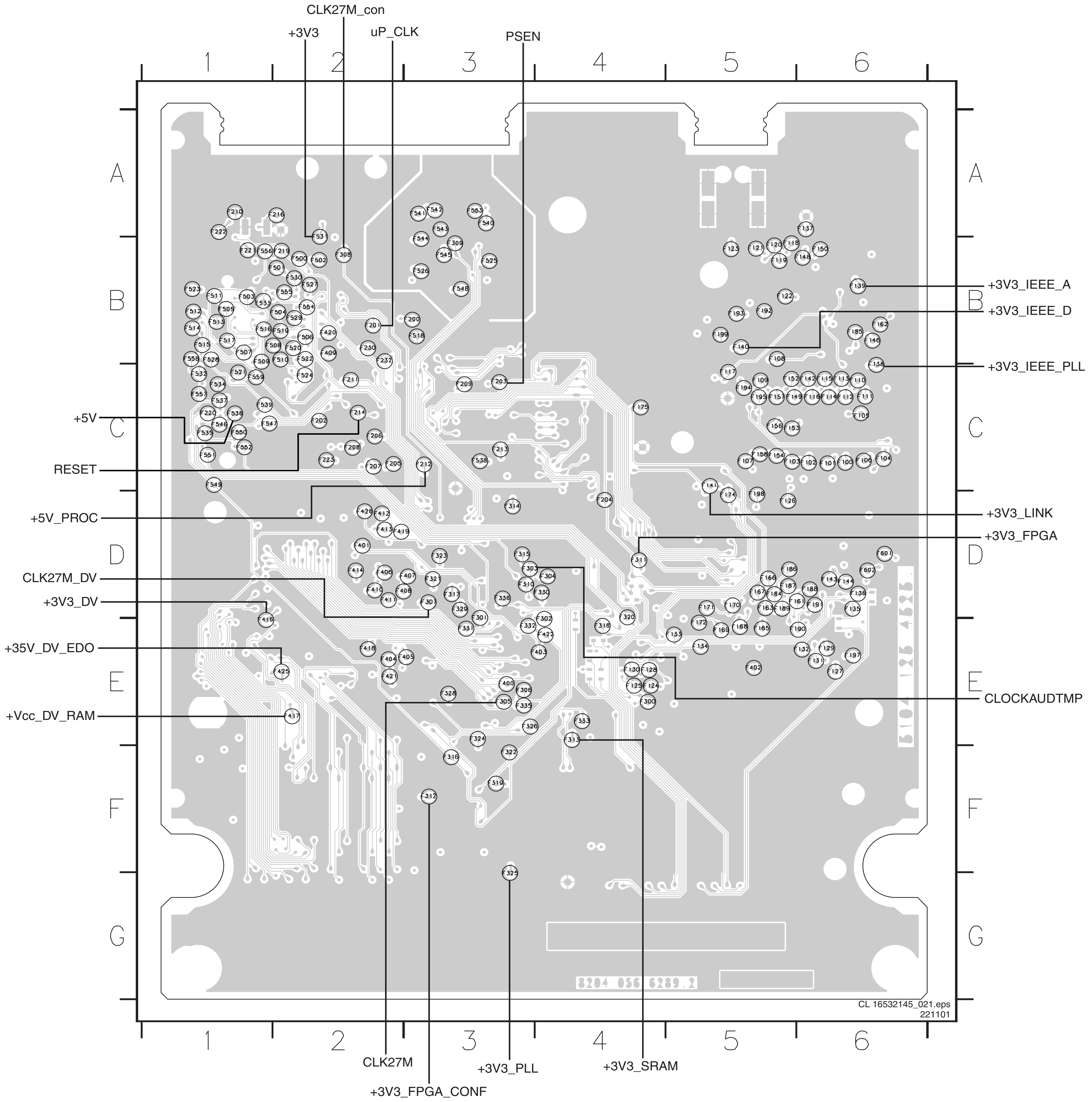
F8007
F8006
F8005
F8004
F8002
F8001
F8003
2002-03-13

F8001	C3
F8002	C3
F8003	C3
F8004	C3
F8005	C3
F8006	C2
F8008	C2
F8009	C2
F801	A3
F802	A2
F803	A1
F804	B3
F805	C3
F806	B3
F807	B3
F808	B3
F809	B3
F810	B3
F811	B3
F812	C2
F813	C2
F814	C2
F815	C2
F816	C1
F817	C1
F818	C1
F819	A3
F820	B3
F821	A3
F822	B3
F823	A3
F824	B3
F825	A3
F826	A3
F827	A1
F828	A2
F830	A2
F831	C1
F832	A1
F833	C1
F834	A1
F835	C1
F836	C1
F837	A2
F838	A2
F839	C2
F840	A2
F8401	A2
F8402	A2
F8403	A2
F8405	A2
F8406	A2
F8407	A1
F841	C2
F842	C2
F843	B1
F844	A2
F845	A2
F846	A1
F847	A1
F848	A3
F849	A3
F8603	A1
F8604	A3
F8606	C3
F8607	C3
F8608	C3
F8609	C3
F8610	C3
F8701	A1
F8702	A3
F8703	A3
F8704	A3
F8705	A3
F8706	A3
F8707	A2
F8708	A2
F8802	C2
F8803	C2
F8804	C2
F8805	C2
F8806	C1
I801	C2
I802	C2
I803	C2
I804	B2
I805	A2
I806	A3
I807	A3
I808	A3
I809	C1
I810	B3
I811	A3
I812	B1
I813	A1
I814	B3
I815	A3
I816	A1
I817	C1
I818	B1
I819	C1
I820	C1
I821	B3
I822	A3
I823	A2
I824	A2
I825	C2
I903	B1
I904	B1
I905	B1
I906	A1
I907	A1
I908	A1
I909	A1

TR 01053_001
140502

Test points overview DIVIO Board



F100	C6
F100	C6
F101	C6
F101	C6
F102	C6
F102	C6
F103	C5
F103	C5
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F104	C6
F105	C6
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F113	C6
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F115	C6
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F117	C5
F117	C5
F118	B5
F118	B5
F119	B5
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F120	B5
F121	B5
F121	B5
F122	B5
F122	B5
F123	B5
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F132	E6
F133	E5
F133	E5
F134	E5
F134	E5
F135	D6
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F138	C6
F139	B6
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F141	C5
F141	C5
F142	C6
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F143	D6
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F144	D6
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F146	B6
F146	B6
F148	B6
F148	B6
F149	C5
F149	C5
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F158	C5
F158	C5
F161	D6
F161	D6
F162	B6
F162	B6
F163	D5
F163	D5
F165	E5
F165	E5
F166	D5
F166	D5
F167	D5
F167	D5
F168	E5
F168	E5
F169	E5
F169	E5
F170	D5
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F201	B2
F202	C2
F202	C2
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F206	C2
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F208	C2
F208	C2
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F209	C3
F210	A1
F210	A1
F211	C2
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F214	C2
F214	C2
F216	A2
F216	A2
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F220	C1
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F221	B1
F222	A1
F222	A1
F223	C2
F223	C2
F230	B2
F230	B2
F232	B2
F232	B2
F300	E4
F300	E4
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F302	E4
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F304	D4
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F305	E3
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F310	D3
F311	D4
F311	D4
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F313	E4
F313	E4
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F552	C1
F553	A3
F553	A3
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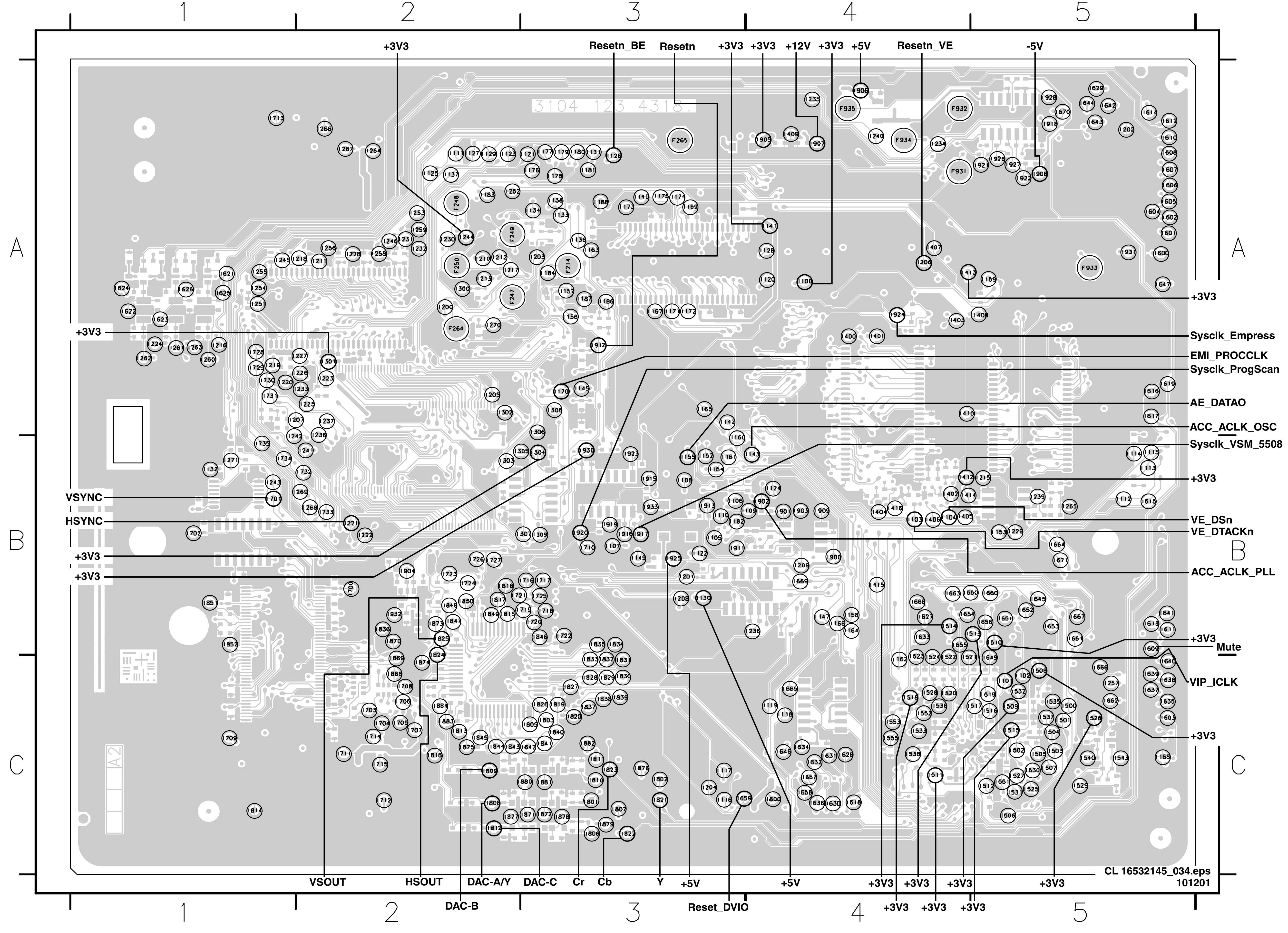
F554	B2
F555	B2
F555	B2
F556	B1
F556	B1
F557	C1

Test points overview Digital Board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2
3
4
5
A
B
C
+3V3
Resetn_BE
Resetn
+3V3
+3V3
+12V
+3V3
+5V
Resetn_VE
-5V
3104 123 4318
+3V3
Sysclk_Empress
EMI_PROCCLK
Sysclk_ProgScan
AE_DATAO
ACC_ACLK_OSC
Sysclk_VSM_5508
+3V3
VE_DSn
VE_DTACKn
ACC_ACLK_PLL
+3V3
Mute
VIP_ICLK
+3V3
+3V3
VSYNC
HSYNC
+3V3
+3V3
VSOUT
HSOUT
DAC-A/Y
DAC-C
Cr
Cb
Y
+5V
+5V
+3V3
+3V3
+3V3
+3V3
DAC-B
Reset_DVIO
+3V3
+3V3
+3V3
CL 16532145_034.eps
101201

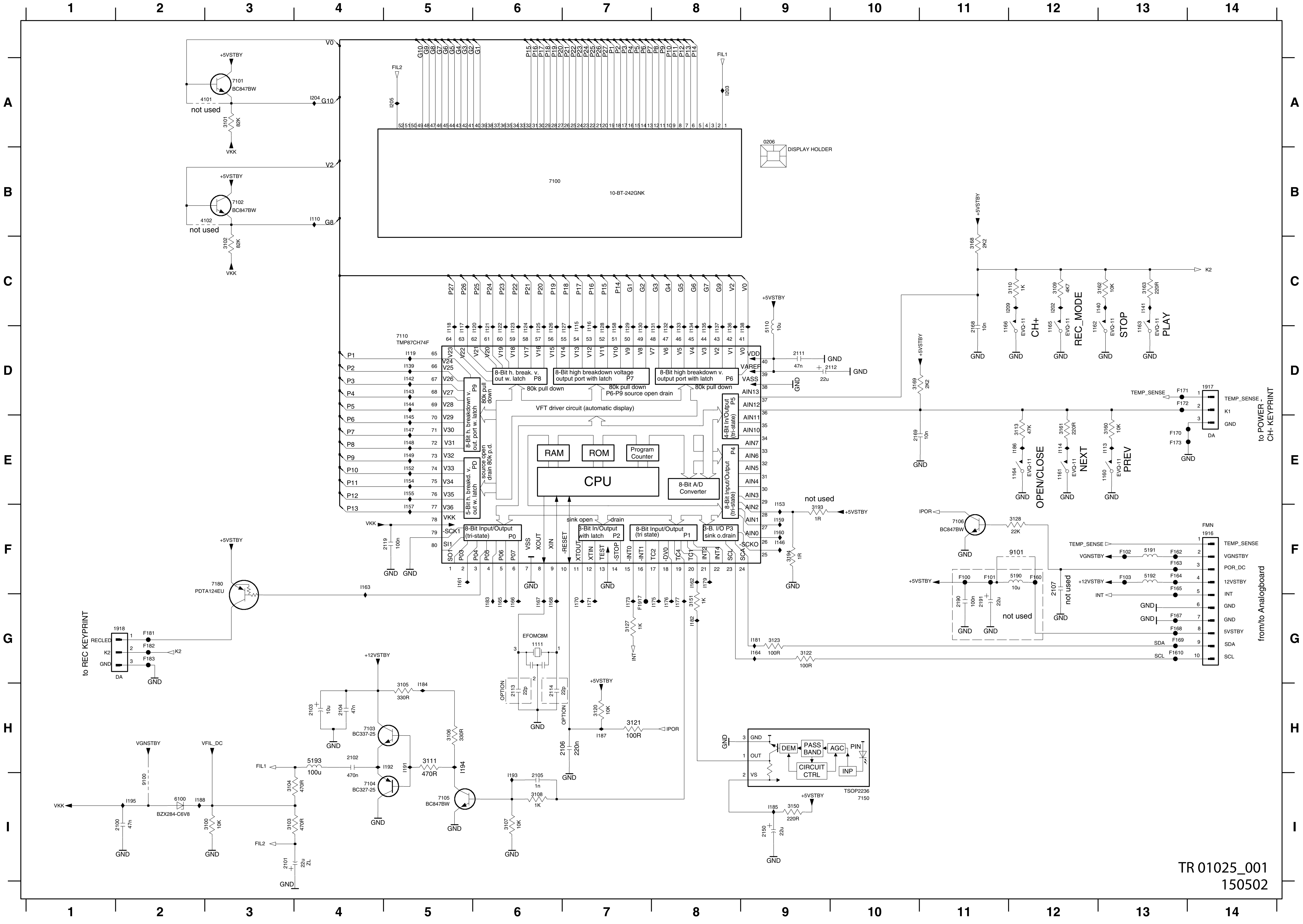
Layout Digital Board (Mapping Testlands)

F214	A3
F247	A2
F248	A2
F249	A2
F250	A2
F264	A2
F265	A3
F931	A4
F932	A4
F933	A5
F934	A4
F935	A4
I100	A4
I101	C5
I102	C5
I103	B4
I104	B4
I105	B3
I106	B3
I107	B3
I108	B3
I109	B4
I110	B3
I111	A2
I112	B5
I113	B5
I114	B5
I115	B5
I116	C3
I117	C3
I118	C4
I119	C4
I120	A4
I121	A3
I122	B3
I123	A2
I124	B4
I125	A2
I126	A3
I127	A2
I128	A4
I129	A2
I130	B3
I131	A3
I132	B1
I133	A3
I134	A3
I136	A3
I137	A2
I138	A3
I140	A3
I141	A4
I142	A3
I143	B4
I145	A3
I147	B4
I149	B3
I152	B3
I153	B5
I154	B3
I155	B3
I156	A3
I157	A3
I158	B4
I159	A5
I160	B3
I161	B3
I162	C4
I163	A3
I164	B4
I165	A3
I166	B4
I167	A3
I168	C5
I169	A3
I170	A3
I171	A3
I172	A3
I173	A3
I174	A3
I175	A3
I176	A3
I177	A3
I178	A3
I179	A3
I180	A3
I181	A3
I182	B3
I183	A2
I184	A3
I186	A3
I187	A3
I188	A3
I200	A2
I201	B3
I202	A5
I203	A3
I204	C3
I205	A2
I206	A4
I207	A2
I208	B3
I209	B4
I210	A2
I211	A2
I212	A2
I213	A2
I215	B5
I216	A1
I217	A2
I218	A2
I219	A1
I220	A1
I221	B2
I222	B2
I223	A2
I224	A1
I225	A2
I226	A2
I227	A2
I228	A2
I229	B5
I230	A2
I231	A2
I232	A2
I233	A2
I234	A4
I235	A4
I236	B4
I237	A2
I238	A2
I239	B5
I240	A4
I241	B2
I242	B1
I243	B1
I244	A2
I245	A1
I246	A2
I251	A1
I252	A2
I253	A2
I254	A1
I255	A1
I256	A2
I257	C5
I258	A2
I259	A2
I260	A1
I261	A1
I262	A1
I263	A1
I264	A2
I265	B5
I266	A2
I267	A2
I268	B2
I269	B2
I270	A2
I271	B1
I300	A2
I301	A2
I302	A2
I303	B2
I304	B3
I305	B3
I306	A3
I307	B3
I308	A3
I309	B3
I400	A4
I401	A4
I402	B4
I403	A4
I404	B4
I405	B4
I406	B4
I407	A4
I408	A5
I409	A4
I410	A4
I412	B4
I413	A4
I414	B4
I415	B4
I416	B4
I500	C5
I501	C5
I502	C5
I503	C5
I504	C5
I505	C5
I506	C5
I507	C5
I508	C5
I509	C5
I510	B5
I511	C4
I512	C5
I513	B5
I514	B4
I515	C5
I516	C5
I517	C5
I518	C4
I519	C5
I520	C4
I521	C4
I522	C4
I523	C4
I524	C4
I525	C5
I526	C5
I527	C5
I528	C4
I529	C5
I530	C5
I531	C5
I532	C5
I533	C4
I535	C5
I536	C4
I537	C5
I538	C4
I540	C5
I543	C5
I551	C5
I552	C4
I553	C4
I555	C4
I600	A5
I601	A5
I602	A5
I603	C5
I604	A5
I605	A5
I606	A5
I607	A5
I608	A5
I609	B5
I610	A5
I611	B5
I612	A5
I613	B5
I614	A5
I615	B5
I616	A5
I617	A5
I618	C4
I619	A5
I621	A1
I622	A1
I623	A1
I624	A1
I625	A1
I626	A1
I627	B4
I628	C4
I629	A5
I630	C4
I631	C4
I632	C4
I633	B4
I634	C4
I635	C5
I636	C4
I637	C5
I638	C5
I639	C5
I640	C5
I641	B5
I642	A5
I643	A5
I644	A5
I645	B5
I646	C4
I647	A5
I649	C5
I650	B4
I651	B5
I652	B5
I653	B5
I654	B4
I655	B4
I656	B5
I657	C4
I658	C4
I659	C3
I660	B5
I661	B5
I662	C5
I663	B4
I664	B5
I665	C4
I666	C5
I667	B5
I668	B4
I669	B4
I670	A5
I671	B5
I700	B2
I701	B1
I702	B1
I703	C2
I704	C2
I705	C2
I706	C2
I707	C2
I708	C2
I709	C1
I710	B3
I711	C2
I712	C2
I713	A1
I714	C2
I715	C2
I716	B3
I717	B3
I718	B3
I719	B3
I720	B3
I721	B2
I722	B3
I723	B2
I724	B2
I725	B3
I726	B2
I727	B2
I728	A1
I729	A1
I730	A1
I731	A1
I732	B2
I733	B2
I734	B1
I735	B1
I800	C4
I801	C3
I802	C3
I803	C3
I805	C3
I806	C3
I807	C3
I808	C2
I809	C2
I810	C3
I811	C3
I812	C2
I813	C2
I814	C1
I815	B2
I816	B2
I817	B2
I818	C2
I819	C3
I820	C3
I821	C3
I822	C3
I823	C3
I824	B2
I825	B2
I826	C3
I827	C3
I828	C3
I829	C3
I830	C3
I831	C3
I832	C3
I833	C3
I834	B3
I835	B3
I836	B2
I837	C3
I838	C3
I839	C3
I840	C3
I841	C3
I842	C3
I843	C2
I844	C2
I845	C2
I846	B3
I847	B2
I848	B2
I849	B2
I850	B2
I851	B1
I852	B1
I868	C2
I869	C2
I870	B2
I871	C3
I872	C3
I873	B2
I874	C2
I875	C2
I876	C3
I877	C2
I878	C3
I879	C3
I880	C3
I881	C3
I882	C3
I883	C2
I884	C2
I900	B4
I901	B4
I902	B4
I903	B4
I904	B2
I905	A4
I906	A4
I907	A4
I908	A5
I909	B4
I911	B3
I912	A3
I913	B3
I915	B3
I916	B3
I917	B3
I918	A5
I919	B3
I920	B3
I921	A5
I922	A5
I923	B3
I924	A4
I925	B3
I926	A5
I927	A5
I928	A5
I930	B3
I931	A5
I932	B2
I933	B3

CL 16532145-34m.eps
101201

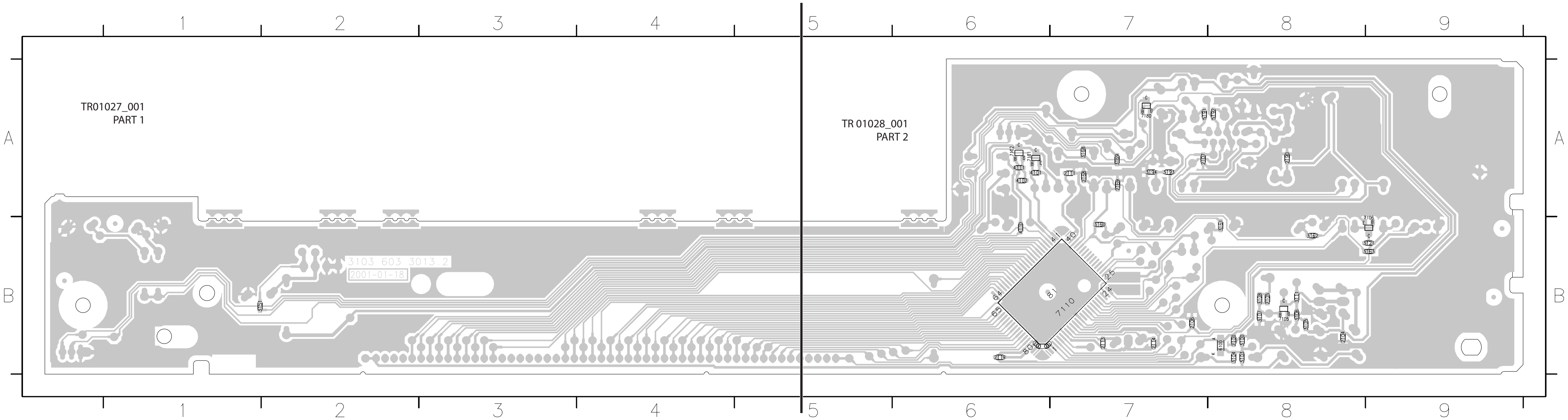
7. Circuit Diagrams and PWB Layouts

Display Panel

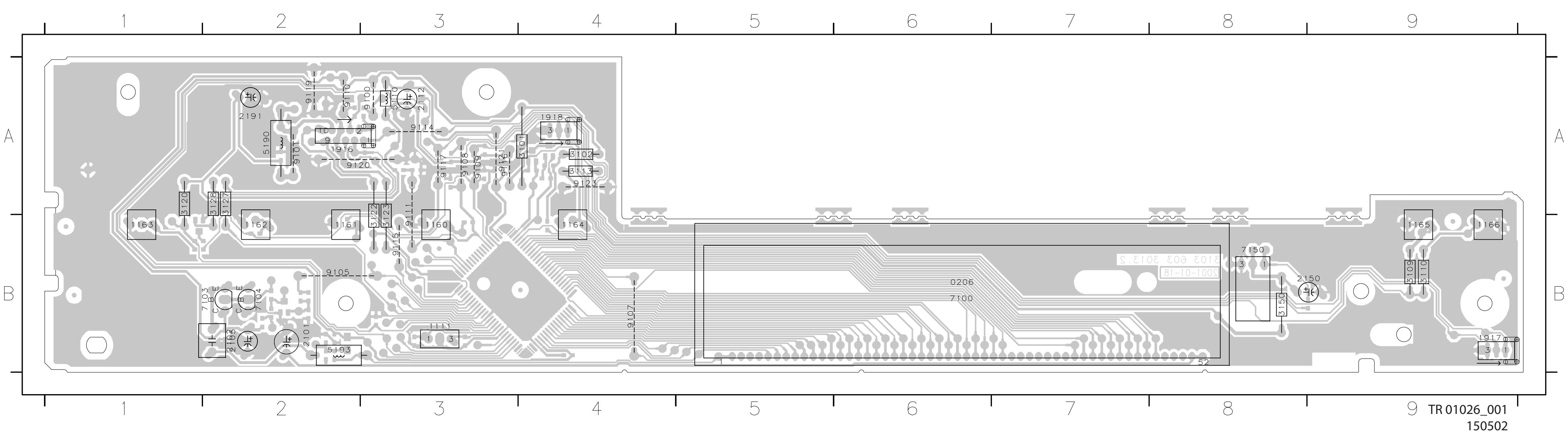

1 2 3 4 5 6 7 8 9 10 11 12 13 14
A B C D E F G H I
7100
10-BT-242GNK
0206 DISPLAY HOLDER
7101 BC847BW
7102 BC847BW
4101 not used
4102 not used
7110 TMP87CH74F
CPU
RAM
ROM
Program Counter
8-Bit A/D Converter
VFT driver circuit (automatic display)
7180 PDTA124EU
7103 BC337-25
7104 BC327-25
7105 BC847BW
7106 BC847BW
6100 BZX284-C6V8
1111 EFOMC8M
7150 TSOP2236
DEM PASS BAND AGC PIN CIRCUIT CTRL INP
CH+
REC_MODE
STOP
PLAY
OPEN/CLOSE
NEXT
PREV
to REC KEYPRINT
to POWER - CH- KEYPRINT
from/to Analogboard
not used
TR 01025_001
150502

0206	A9
1111	G6
1160	E13
1161	E12
1162	D12
1163	D13
1164	E12
1165	D12
1166	D11
1916	F14
1917	D14
1918	G2
2100	I2
2101	I3
2102	H4
2103	H4
2104	H4
2105	I6
2106	H7
2107	F12
2111	D9
2112	D10
2113	H6
2114	H6
2119	F5
2150	I9
2168	D11
2169	E10
2190	G11
2191	G11
3100	I3
3101	A3
3102	C3
3103	I3
3104	I3
3105	H5
3106	H5
3107	I6
3108	I6
3109	C12
3110	C12
3111	H5
3113	E12
3120	H7
3121	H7
3122	G9
3123	G9
3127	G7
3128	F12
3150	I9
3151	G8
3160	E13
3161	E12
3162	C13
3163	C13
3168	C11
3169	D10
3193	F9
3194	F9
4101	A3
4102	B3
5110	D9
5190	F12
5191	F13
5192	F13
5193	H4
6100	I2
7100	B6
7101	A3
7102	B3
7103	H4
7104	I4
7105	I5
7106	F11
7110	D5
7150	I10
7180	F3
9100	I2
9101	F12
F100	F11
F101	F11
F102	F13
F103	F13
F160	F12
F1610	G13
F162	F13
F163	F13
F164	F13
F165	F13
F167	G13
F168	G13
F169	G13
F170	E14
F171	D14
F172	D14
F173	E14
F181	G2
F182	G2
F183	G2
F1917	G7
I110	B4
I113	E13
I114	E12
I115	D7
I116	D7
I117	D5
I118	D5
I119	D5
I120	D6
I121	D6
I122	D6
I123	D6
I124	D6
I125	D6
I126	D6
I127	D7
I128	D7
I129	D7
I130	D7
I131	D8
I132	D8
I133	D8
I134	D8
I135	D8
I136	D8
I137	D8
I138	D9
I139	D5
I140	C13
I141	C13
I142	D5
I143	D5
I144	D5
I145	E5
I146	F9
I147	E5
I148	E5
I149	E5
I152	E5
I153	E9
I154	E5
I155	E5
I157	F5
I158	D7
I159	F9
I160	F9
I161	F5
I162	F8
I163	F4
I164	G9
I165	G6
I166	G6
I167	G6
I168	G6
I170	G7
I171	G7
I173	G7
I175	G8
I176	G8
I177	G8
I179	F8
I181	G9
I182	G8
I183	G6
I184	H5
I185	I9
I186	E12
I187	H7
I188	I2
I191	H5
I192	H5
I193	I6
I194	H5
I195	I2
I202	C12
I203	A8
I204	A4
I205	A5
I209	C11

Layout Display Panel (DISP)

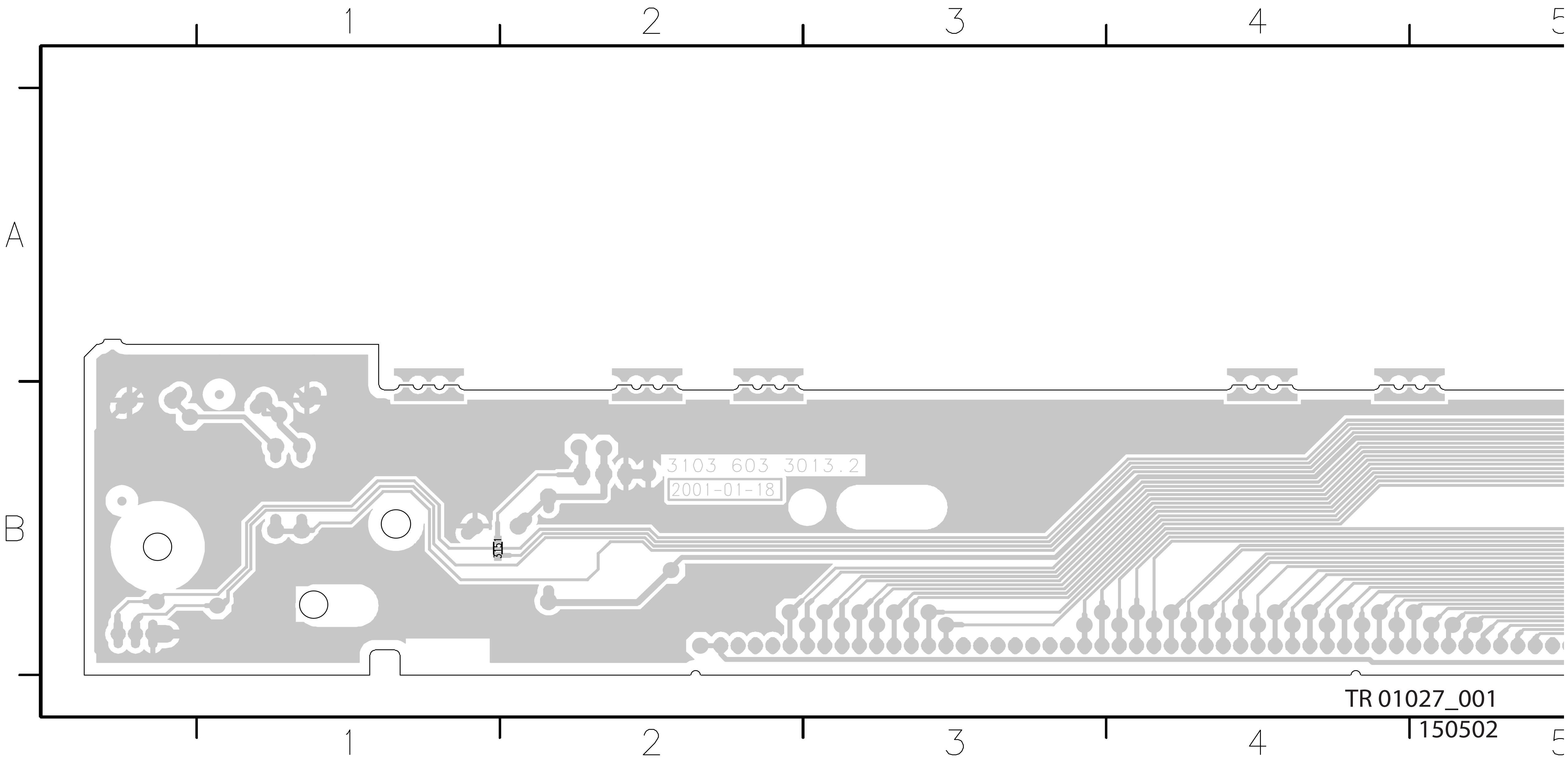

TR01027_001
PART 1
TR 01028_001
PART 2
3103 603 3013.2
2001-01-18
7110
1
2
3
4
5
6
7
8
9
A
B

2100	B8
2104	B9
2105	B9
2111	B7
2113	B7
2114	B7
2119	B6
2168	B8
2169	B7
2190	A7
3100	B8
3101	A6
3102	A6
3103	B8
3104	B8
3105	B9
3106	B9
3107	B9
3108	B9
3120	B8
3151	B2
3160	B7
3161	B8
3162	B8
3163	B9
3193	B8
3194	B8
4101	A6
4102	A6
4110	B6
4111	A6
5110	A7
5191	A7
5192	A7
6100	B8
7101	A6
7102	A6
7105	B9
7106	B9
7110	B7
7180	A6

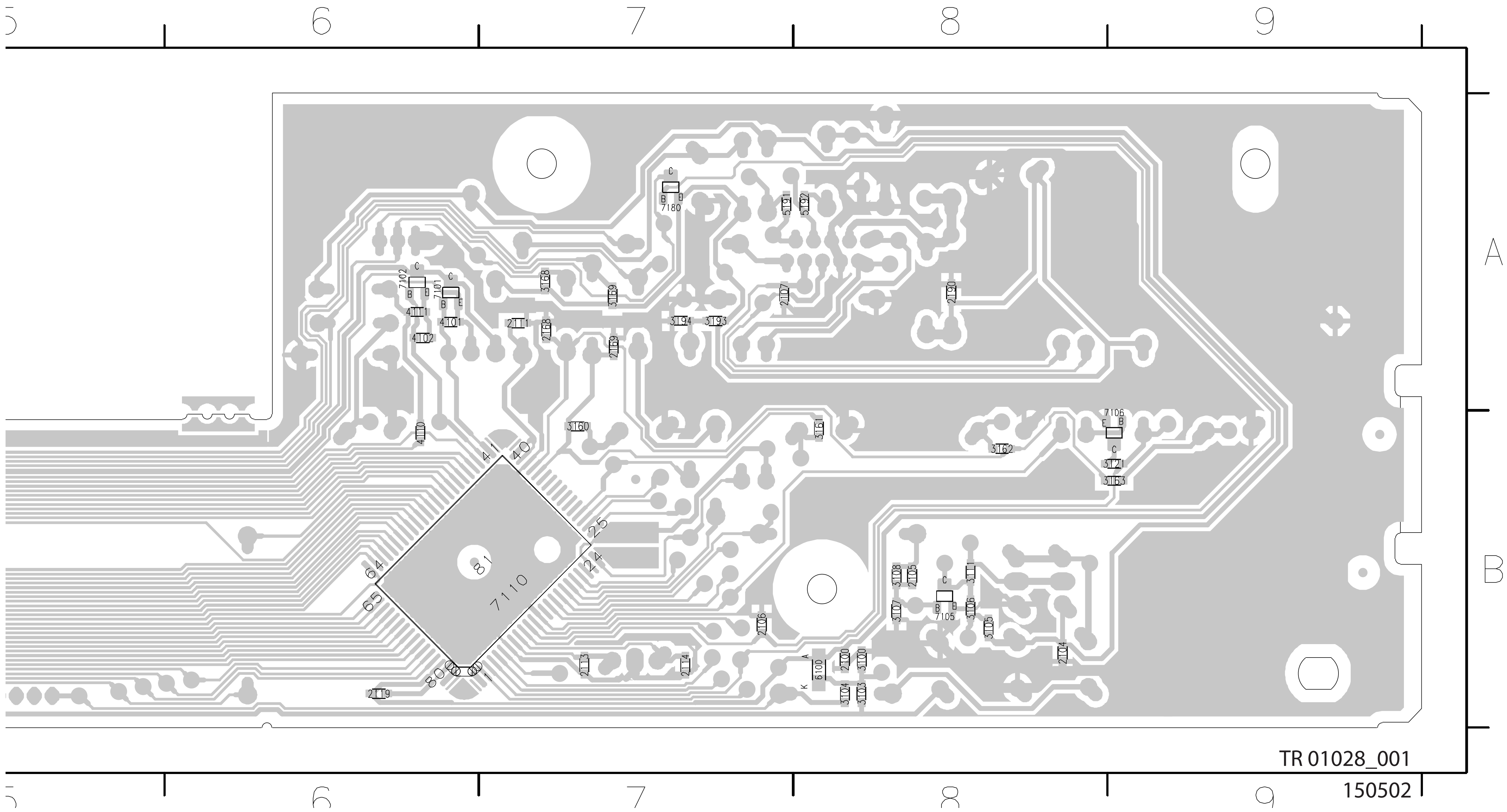

1163
1162
1161
1160
1164
1165
1166
1918
1916
1917
1111
2191
2112
2150
2101
2102
5190
5193
5110
7103
7104
7150
3120
3128
3127
3123
3122
3101
3102
3113
3150
3109
3110
9100
9101
9105
9107
9108
9109
9110
9111
9114
9115
9116
9117
9119
9120
9121
9123
0206
7100
3103 603 3013.2
2001-01-18
TR 01026_001
150502
1
2
3
4
5
6
7
8
9
A
B

0206	B6
1111	B3
1160	B3
1161	B2
1162	B2
1163	B1
1164	B4
1165	B9
1166	B9
1916	A2
1917	B9
1918	A4
2101	B2
2102	B2
2103	B2
2112	A3
2150	B9
2191	A2
3101	A4
3102	A4
3109	B9
3110	B9
3113	A4
3120	A1
3122	B3
3123	B3
3127	A2
3128	A2
3150	B8
5110	A3
5190	A2
5193	B2
7100	B6
7103	B2
7104	B2
7150	B8
9100	A3
9101	A2
9105	B2
9107	B4
9108	A3
9109	A3
9110	A2
9111	A3
9114	A3
9115	B3
9116	A3
9117	A3
9119	A2
9120	A2
9121	A3
9123	A4

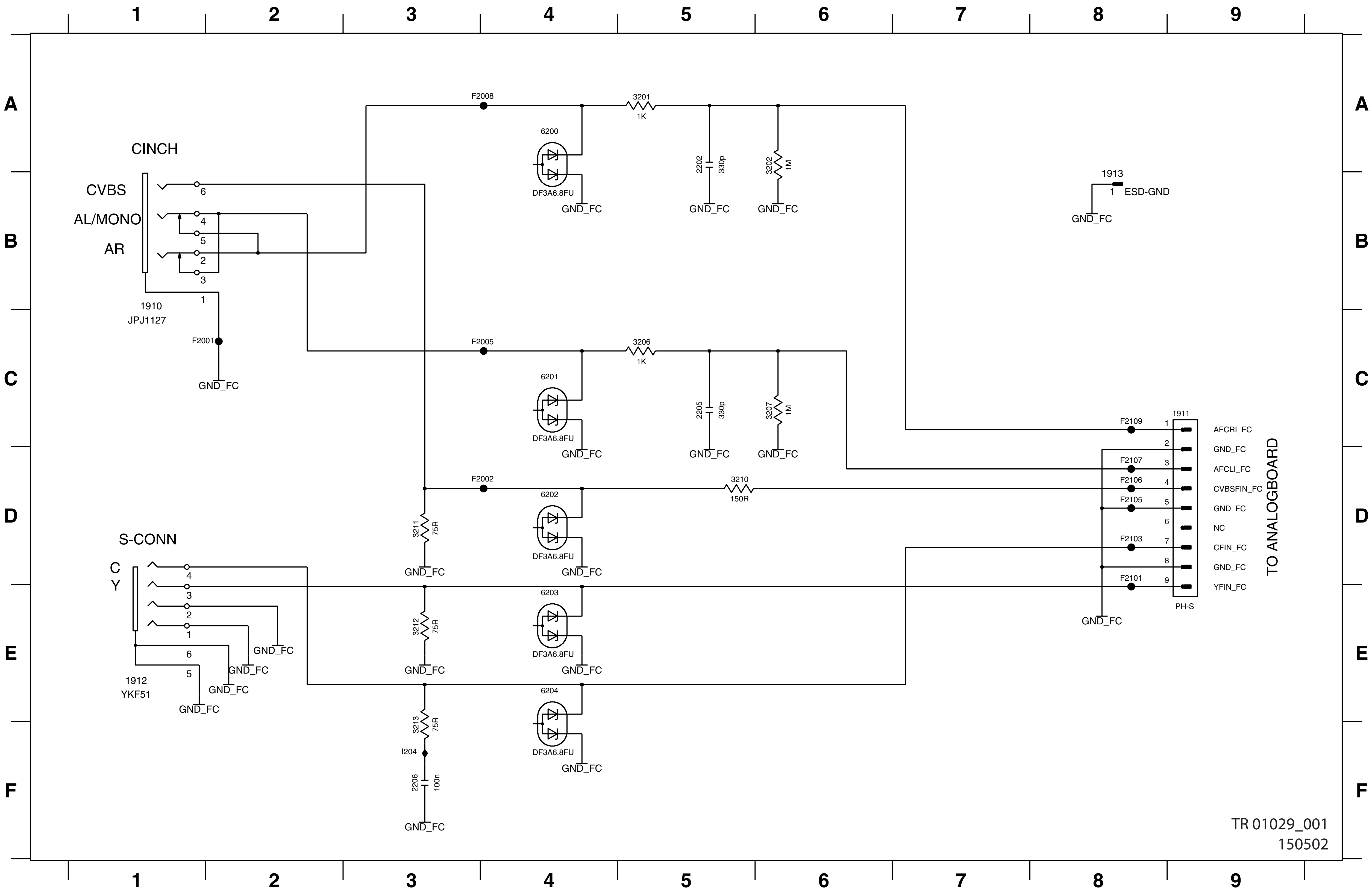
Layout Display Panel (Part 1 Bottom View)


1
2
3
4
5
A
B
3103 603 3013.2
2001-01-18
TR 01027_001
150502

Layout Display Panel (Part 2 Bottom View)


6
7
8
9
A
B
7180
5191
5192
7102
7101
4111
4101
4102
3168
3169
2111
2168
2169
3194
3193
2107
2190
4110
3160
3161
3162
7106
3121
3163
41
40
25
24
64
65
81
7110
80
1
2106
2113
2114
2119
6100
2100
3100
3104
3103
3108
2105
3107
7105
3111
3106
3105
2104
TR 01028_001
150502

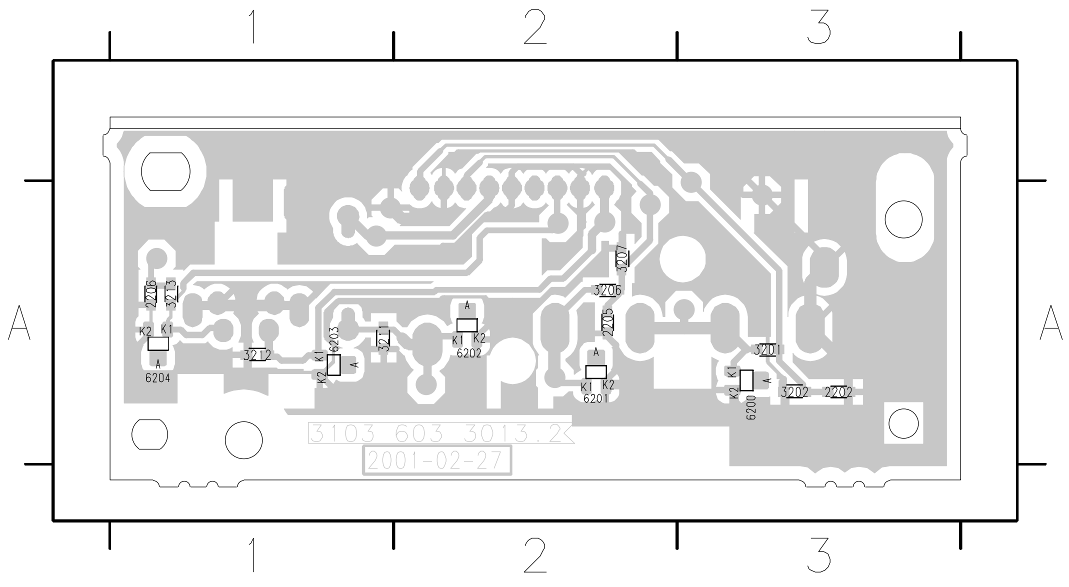
Front Connector Panel (FC)


1
2
3
4
5
6
7
8
9
A
B
C
D
E
F
CINCH
CVBS
AL/MONO
AR
6
4
5
2
3
1
1910
JPJ1127
F2001
GND_FC
F2008
3201
1K
6200
DF3A6.8FU
GND_FC
2202
330p
GND_FC
3202
1M
GND_FC
1913
1
ESD-GND
GND_FC
F2005
3206
1K
6201
DF3A6.8FU
GND_FC
2205
330p
GND_FC
3207
1M
GND_FC
F2002
6202
3210
150R
3211
75R
GND_FC
DF3A6.8FU
GND_FC
S-CONN
C
Y
4
3
2
1
6
5
GND_FC
GND_FC
GND_FC
GND_FC
1912
YKF51
6203
3212
75R
GND_FC
DF3A6.8FU
GND_FC
6204
3213
75R
I204
2206
100n
GND_FC
DF3A6.8FU
GND_FC
1911
F2109
F2107
F2106
F2105
F2103
F2101
1
2
3
4
5
6
7
8
9
AFCRI_FC
GND_FC
AFCLI_FC
CVBSFIN_FC
GND_FC
NC
CFIN_FC
GND_FC
YFIN_FC
PH-S
GND_FC
TO ANALOGBOARD
TR 01029_001
150502

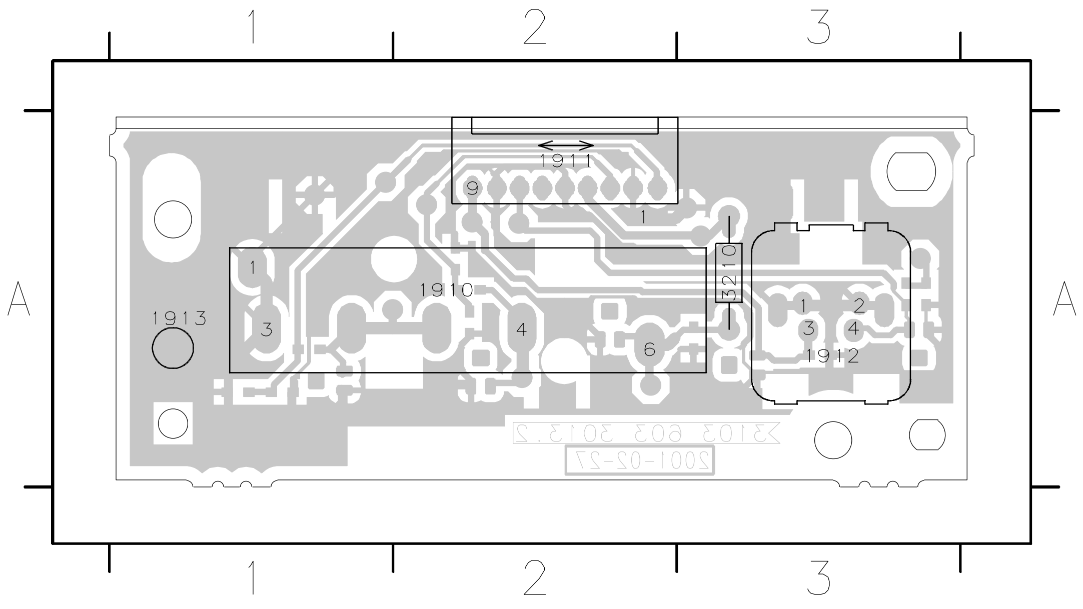
1910	**B1**
1911	**C9**
1912	**E1**
1913	**B8**
2202	**A5**
2205	**C5**
2206	**F3**
3201	**A5**
3202	**A6**
3206	**C5**
3207	**C6**
3210	**D5**
3211	**D3**
3212	**E3**
3213	**F3**
6200	**A4**
6201	**C4**
6202	**D4**
6203	**E4**
6204	**E4**
F2001	**C1**
F2002	**D4**
F2005	**C4**
F2008	**A4**
F2101	**D8**
F2103	**D8**
F2105	**D8**
F2106	**D8**
F2107	**D8**
F2109	**C8**
I204	**F3**

Layout Front Connector Panel (FC)

2200	A2	2205	A2	3203	A3	3208	A3	4201	A3	6202	A2
2201	A3	2206	A1	3204	A3	3209	A3	4202	A2	6203	A1
2202	A3	3200	A3	3205	A2	3211	A2	4203	A3	6204	A1
2203	A3	3201	A3	3206	A2	3212	A1	6200	A3	7200	A3
2204	A3	3202	A3	3207	A3	3213	A1	6201	A2	7201	A2


1
2
3
A
A
2206
3213
K2 K1
6204
3212
6203
K2 K1
3211
6202
K1 K2
3207
3206
3205
6201
K1 K2
3201
6200
K2 K1
3202
2202
3103 603 3013.2
2001-02-27
1
2
3

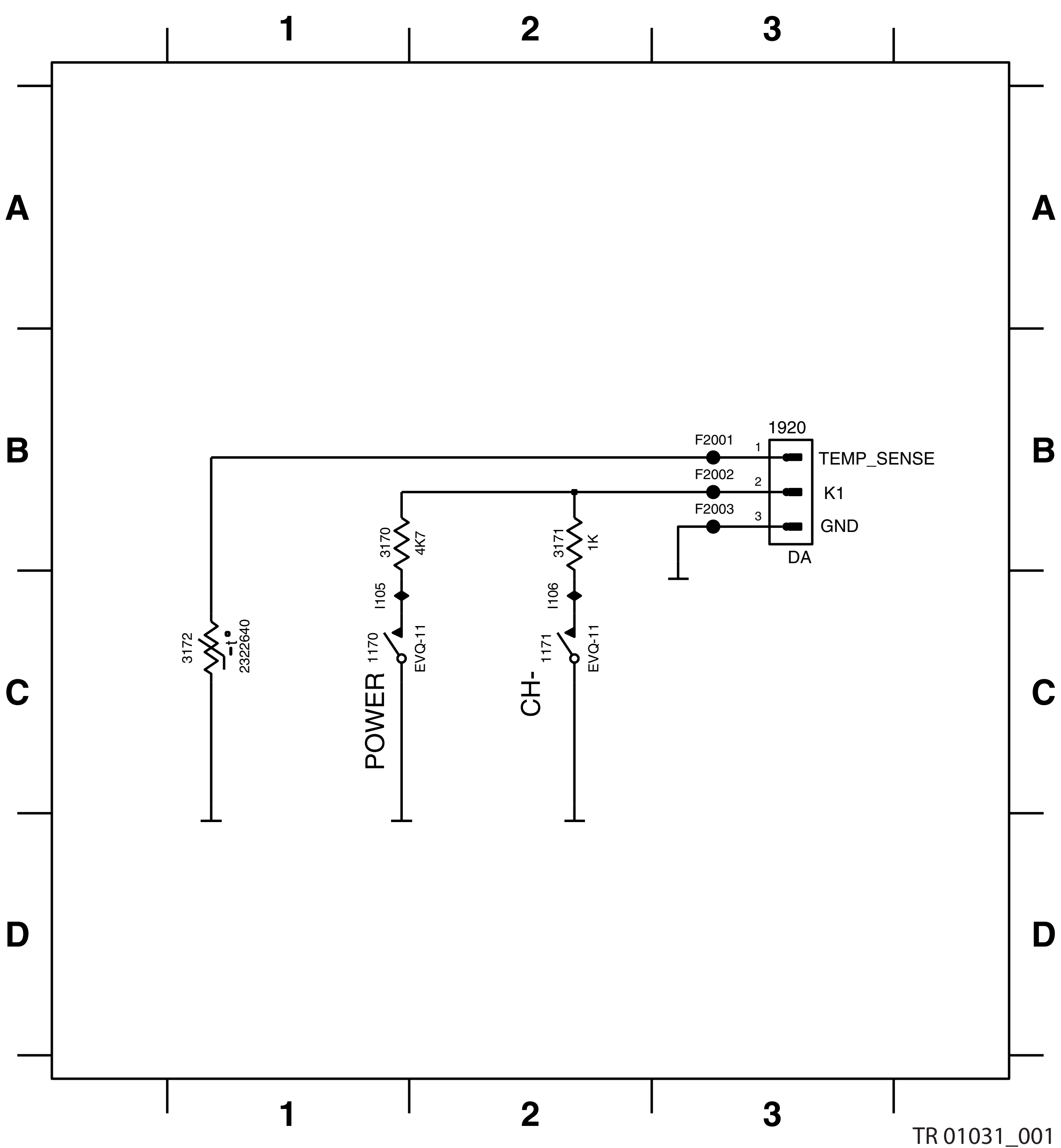
1910	A2	1911	A2	1912	A3	1913	A1	3210	A3


1
2
3
A
A
1911
9
1
1910
1
3
4
6
1913
3210
1
2
3
4
1912
3103 603 3013.2
2001-02-27
1
2
3

TR 01030_001
150502

Key Panel (KEY)

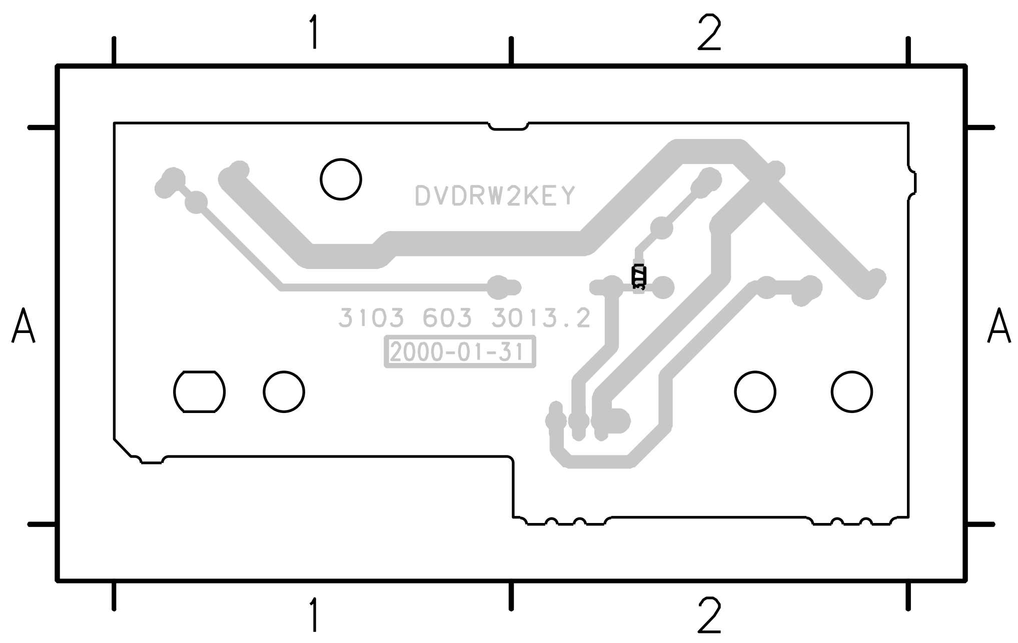
1170 C1	**1920 B3**	**3171 B2**	**F2001 B3**	**F2003 B3**	**I106 C2**
1171 C2	**3170 B1**	**3172 C1**	**F2002 B3**	**I105 C1**	


1
2
3
A
B
C
D
1920
F2001
F2002
F2003
1
2
3
TEMP_SENSE
K1
GND
DA
3170
4K7
3171
1K
I105
I106
3172
2322640
1170
EVQ-11
1171
EVQ-11
POWER
CH-

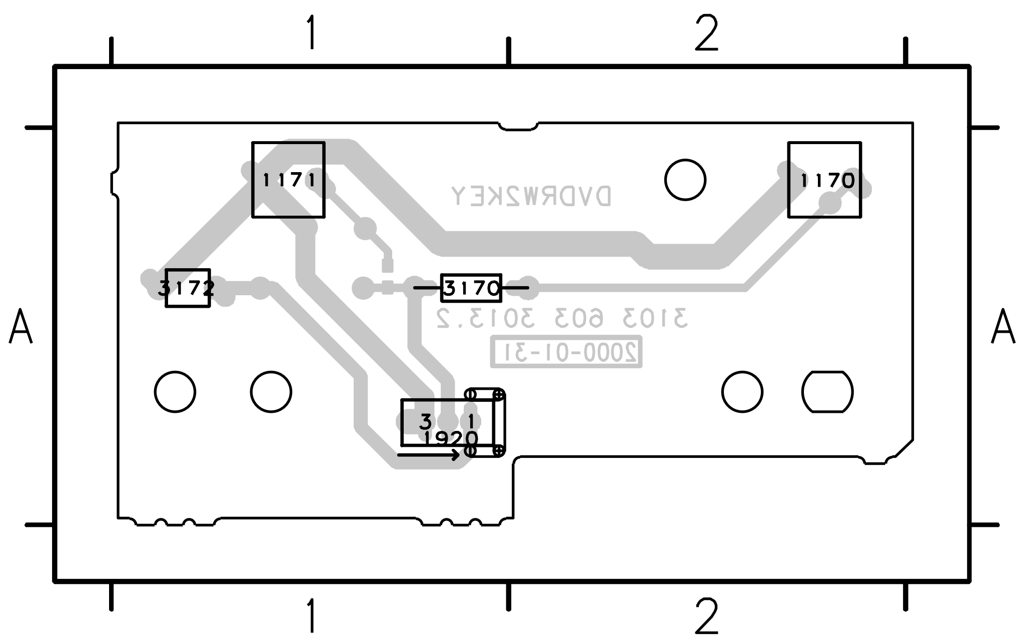
TR 01031_001
150502

Layout Key Panel (KEY)

3171 A2


1
2
A
DVDRW2KEY
3103 603 3013.2
2000-01-31

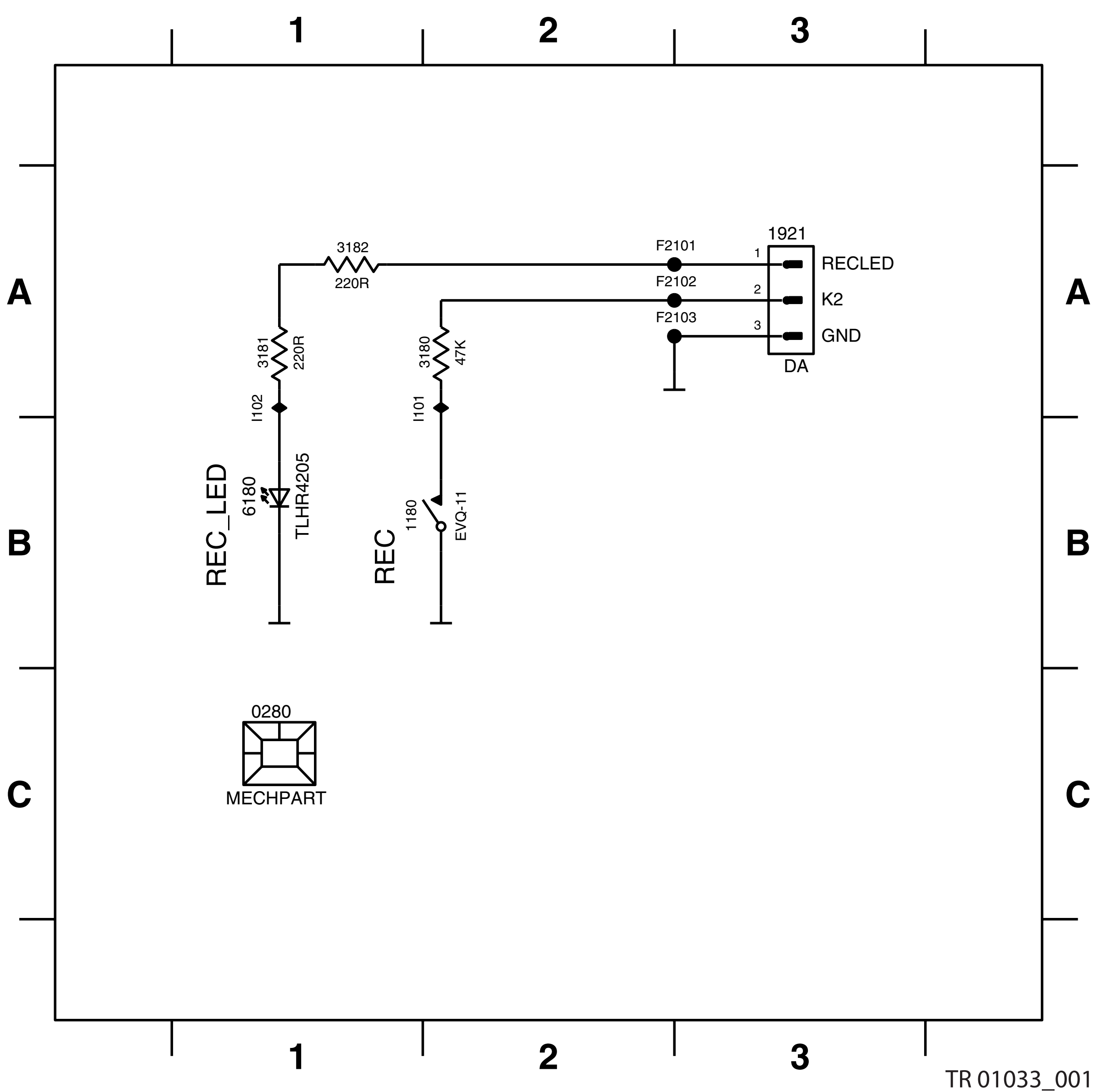
1170 A2
1171 A1
1920 A1
3170 A1
3172 A1


1
2
A
1171
1170
3172
3170
1920
3
1

TR 01032_001
150502

Record Key Panel (REC)

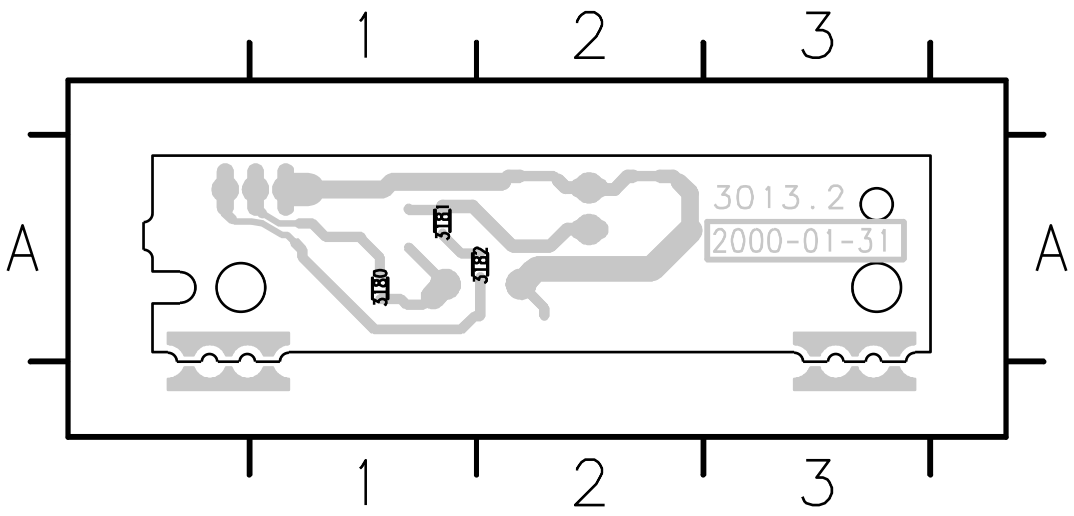
0280	C1
1180	B1
1921	A3
3180	A2
3181	A1
3182	A1
6180	B1
F2101	A3
F2102	A3
F2103	A3
I101	A1
I102	A1


1
2
3
A
B
C
3182
220R
F2101
F2102
F2103
1921
1
2
3
RECLED
K2
GND
DA
3181
220R
3180
47K
I102
I101
REC_LED
6180
TLHR4205
REC
1180
EVQ-11
0280
MECHPART

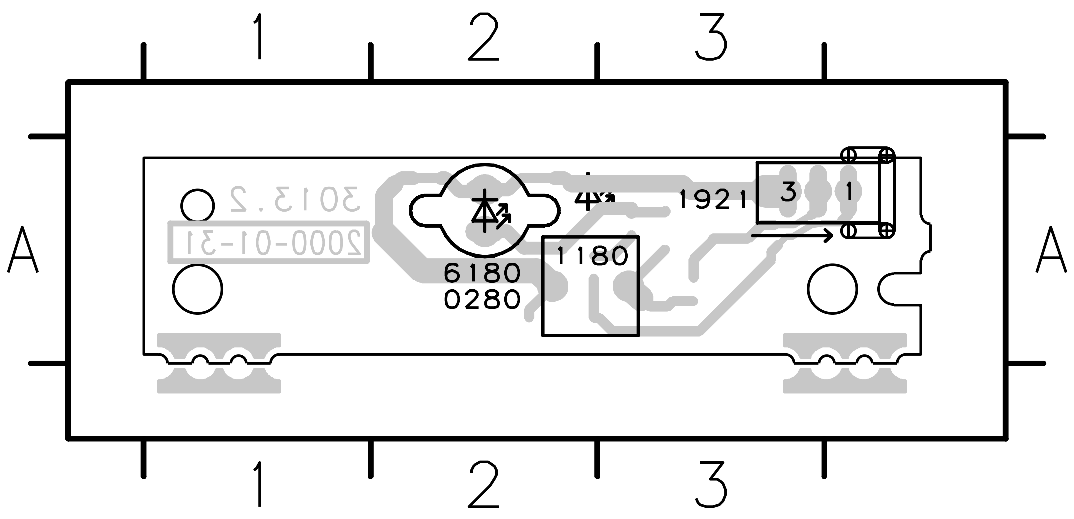
TR 01033_001
150502

Layout Record Key Panel (REC)

3180	A1
3181	A1
3182	A2


1
2
3
A
3013.2
2000-01-31
3180
3181
3182

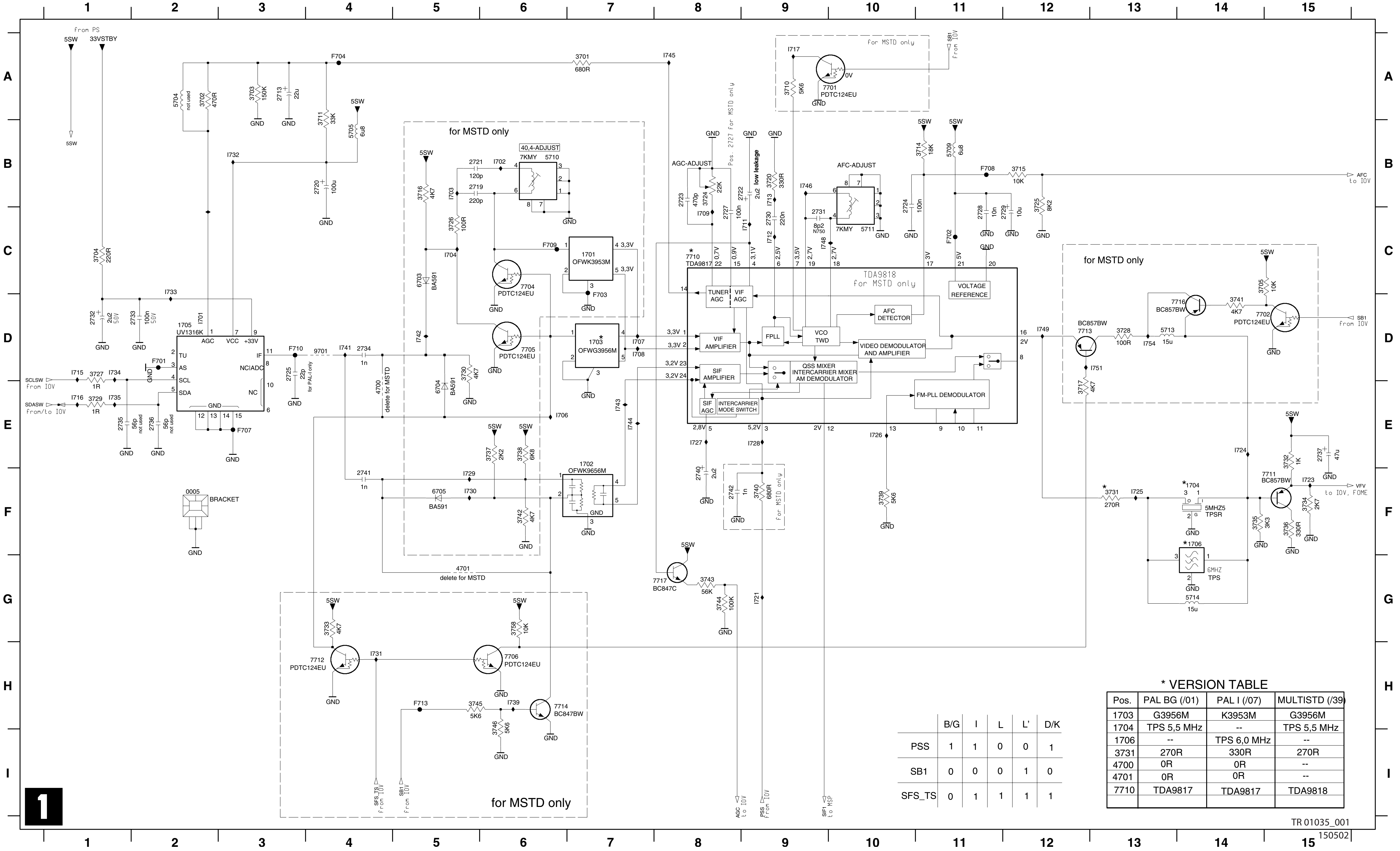
0280	A2
1180	A2
1921	A3
6180	A2


1
2
3
A
3013.2
2000-01-31
6180
0280
1180
1921
3
1

TR 01034_001
150502

Analog Board: Fronted Video (FV)

0005 F2
1701 C7
1702 E7
1703 D7
1704 F14
1705 D2
1706 F14
2713 A3
2719 B5
2720 B4
2721 B5
2722 B9
2723 B8
2724 B10
2725 D3
2727 C8
2728 C11
2729 C12
2730 C9
2731 C9
2732 D1
2733 D2
2734 D4
2735 E1
2736 E2
2737 E15
2740 F8
2741 F4
2742 F8
3701 A7
3702 A2
3703 A3
3704 C1
3705 C14
3710 A9
3711 A4
3714 B11
3715 B12
3716 B5
3717 E12
3720 B9
3724 B8
3725 B12
3726 C5
3727 D1
3728 D13
3729 E1
3730 D5
3731 F13
3732 E15
3733 G4
3734 F15
3735 F14
3736 F15
3737 E6
3738 E6
3739 F10
3740 F9
3741 D14
3742 F6
3743 G8
3744 G8
3745 H5
3746 H6
3758 G6
4700 E4
4701 G5
5704 A2
5705 B4
5709 B11
5710 B6
5711 C10
5713 D13
5714 G14
6703 C5
6704 E5
6705 F5
7701 A10
7702 D15
7704 C6
7705 D6
7706 H6
7710 C8
7711 F14
7712 H4
7713 D12
7714 H6
7716 D14
7717 G7
9701 D4
F701 D2
F702 C11
F703 D7
F704 A4
F707 E3
F708 B11
F709 C6
F710 D3
F713 H5
I701 D2
I702 B6
I703 B5
I704 C5
I706 E6
I707 D7
I708 D7
I709 C8
I711 C9
I712 C9
I713 B9
I715 D1
I716 E1
I717 A9
I721 G9
I723 F15
I724 E14
I725 F13
I726 E10
I727 E8
I728 E9
I729 F5
I730 F5
I731 H4
I732 B3
I733 C2
I734 D1
I735 E1
I739 H6
I741 D4
I742 D5
I743 E7
I744 E7
I745 A8
I746 B9
I748 C9
I749 D12
I751 D13
I754 D13


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
A B C D E F G H I
from PS
5SW
33VSTBY
F704
3701
680R
I745
for MSTD only
SB1 from IOV
I717
3710 5K6
7701 PDTC124EU
0V
5704 not used
3702 470R
3703 150K
2713 22u
3711 33K
5705 6u8
I732
2720 100u
40,4-ADJUST
7KMY 5710
2721 120p
2719 220p
I702
I703
3716 4K7
3726 100R
F709
1701 OFWK3953M
7704 PDTC124EU
7705 PDTC124EU
1703 OFWG3956M
F703
6703 BA591
I742
I704
I707
I708
3730 4K7
6704 BA591
I706
3704 220R
I733
2732 2u2 50V
2733 100n 50V
1705 UV1316K
I701
AGC VCC +33V
TU AS SCL SDA
IF NC\ADC NC
GND
F701
F710
9701
I741
2734 1n
2725 22p for PAL-I only
4700 delete for MSTD
SCLSW from IOV
SDASW from/to IOV
3727 1R
3729 1R
I715 I716 I734 I735
2735 56p not used
2736 56p not used
F707
0005 BRACKET
3737 2K2
3738 6K8
I729
2741 1n
6705 BA591
I730
1702 OFWK9656M
3742 4K7
4701 delete for MSTD
AGC-ADJUST
2723 470p
3724 22K
I709
2727 100n
2722 2u2 low leakage
Pos. 2727 for MSTD only
3720 330R
I713 I711 I712
2730 220n
I746
2731 8p2 N750
AFC-ADJUST
7KMY 5711
I748
3714 18K
5709 6u8
F708
3715 10K
AFC to IOV
2724 100n
F702
2728 10n
2729 10u
3725 8K2
7710 TDA9817
TDA9818 for MSTD only
TUNER AGC
VIF AGC
VIF AMPLIFIER
SIF AMPLIFIER
FPLL
VCO TWD
AFC DETECTOR
VOLTAGE REFERENCE
VIDEO DEMODULATOR AND AMPLIFIER
QSS MIXER INTERCARRIER MIXER AM DEMODULATOR
SIF AGC
INTERCARRIER MODE SWITCH
FM-PLL DEMODULATOR
3,3V 3,2V 2,8V 5,2V 2V 0,7V 0,9V 3,1V 2,5V 3,5V 2,7V 3V 5V
I727 I728 I726 I743 I744
2740 2u2
2742 1n
3740 680R
3739 5K6
7717 BC847C
3743 56K
3744 100K
I721
AGC to IOV
PSS from IOV
SIF1 to MSP
for MSTD only
I749
BC857BW 7713
3728 100R
I754
5713 15u
I751
3717 4K7
7716 BC857BW
3741 4K7
3705 10K
7702 PDTC124EU
SB1 from IOV
I724
3731 270R
I725
1704 5MHZ5 TPSR
1706 6MHZ TPS
5714 15u
3735 3K3
3736 330R
7711 BC857BW
3732 1K
2737 47u
I723
3734 2K7
VFV to IOV, FOME
3733 4K7
7712 PDTC124EU
I731
3758 10K
7706 PDTC124EU
F713
3745 5K6
I739
7714 BC847BW
3746 5K6
SFS_TS from IOV
SB1 from IOV
for MSTD only
GND

* VERSION TABLE

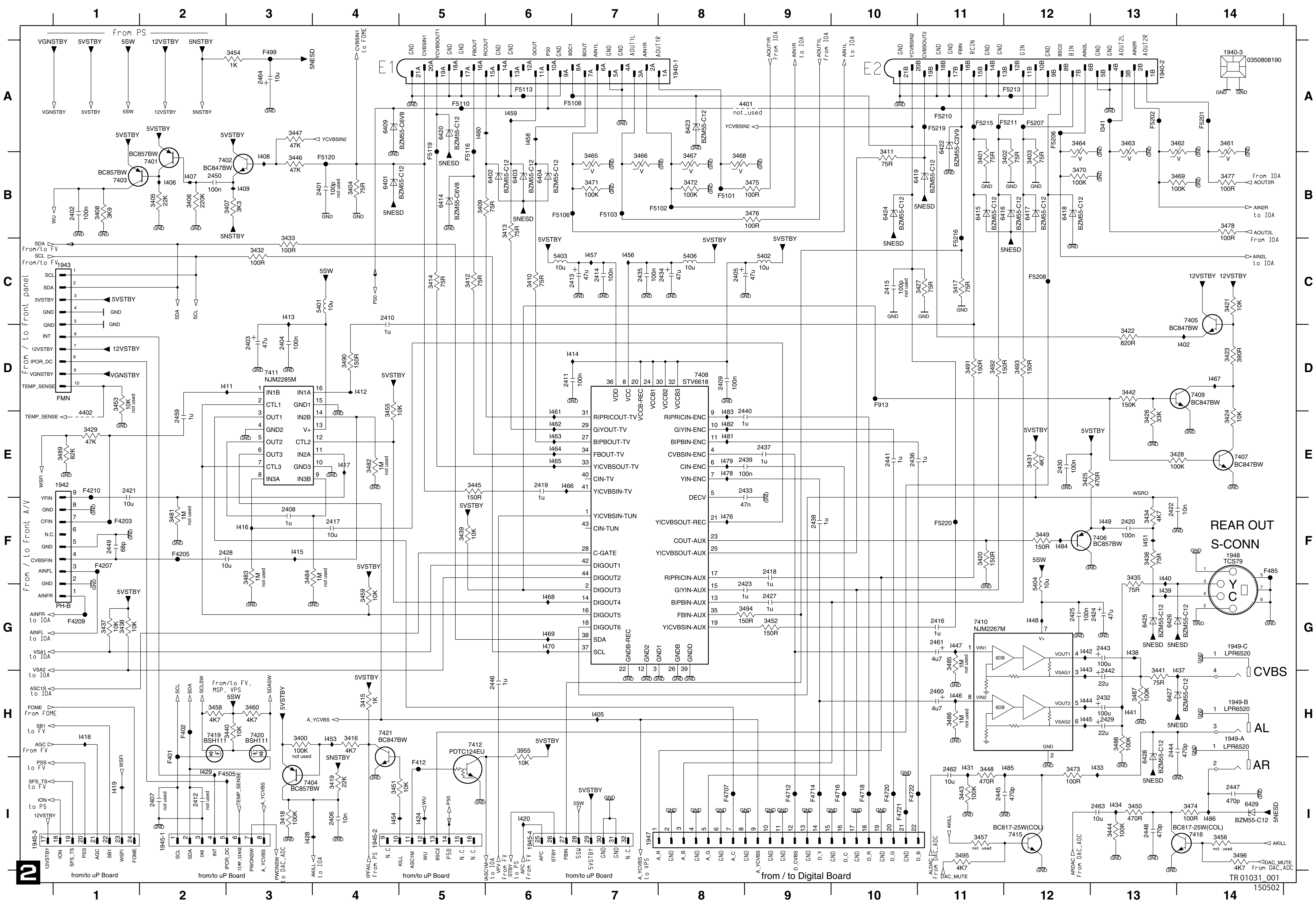
Pos.	PAL BG (/01)	PAL I (/07)	MULTISTD (/39)
1703	G3956M	K3953M	G3956M
1704	TPS 5,5 MHz	--	TPS 5,5 MHz
1706	--	TPS 6,0 MHz	--
3731	270R	330R	270R
4700	0R	0R	--
4701	0R	0R	--
7710	TDA9817	TDA9817	TDA9818

	B/G	I	L	L'	D/K
PSS	1	1	0	0	1
SB1	0	0	0	1	0
SFS_TS	0	1	1	1	1

TR 01035_001

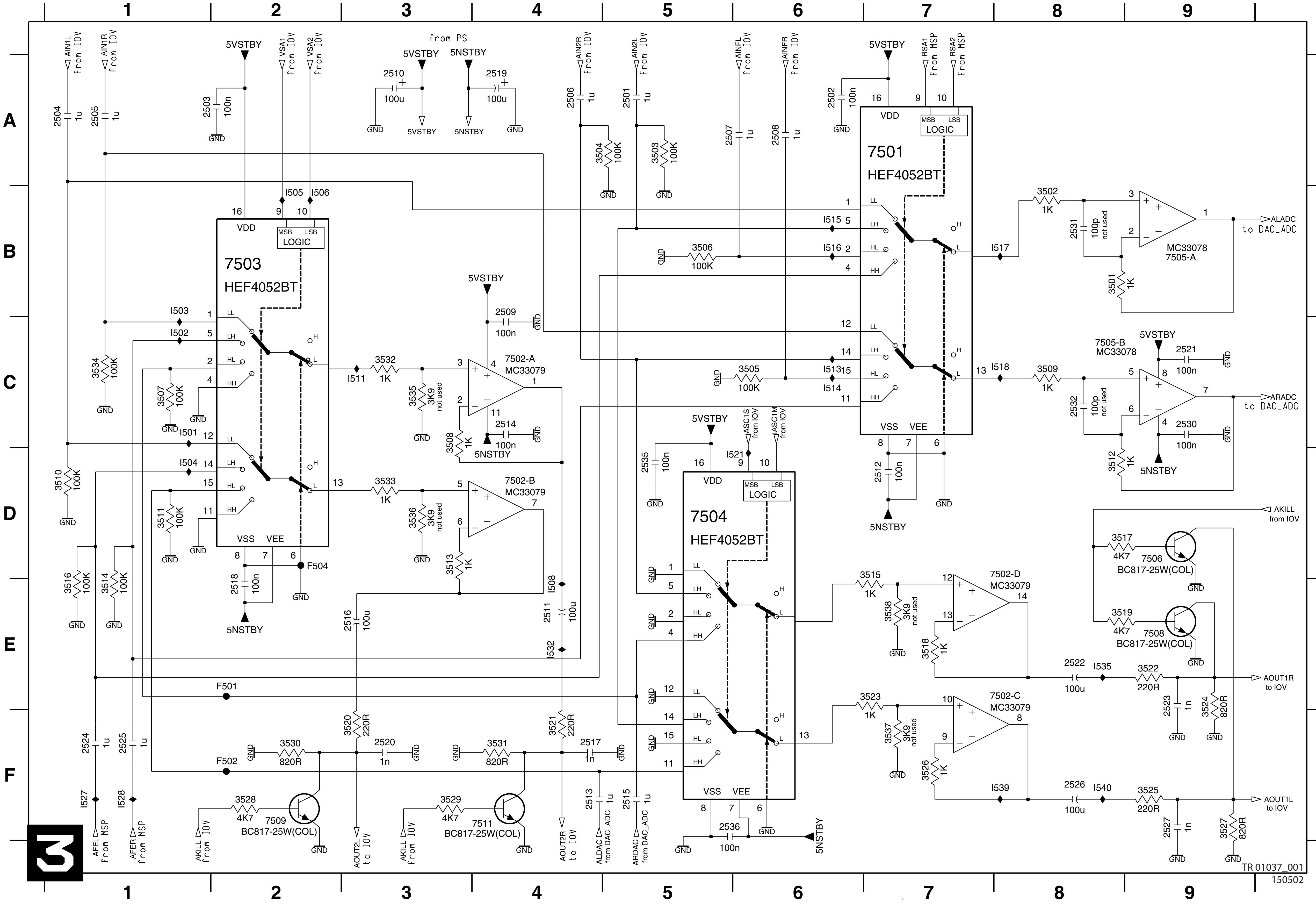
150502

Analog Board: In/Out Video (IOV)


1
2
3
4
5
6
7
8
9
10
11
12
13
14
A
B
C
D
E
F
G
H
I
from PS
VGNSTBY
5VSTBY
5SW
12VSTBY
5NSTBY
5NESD
E1
E2
1940-1
1940-2
1940-3
0350808190
7401 BC857BW
7403 BC857BW
7402 BC847BW
YCVBSIN2
from/to FV
SDA
SCL
1943
FMN
INT
IPOR_DC
TEMP_SENSE
from / to front panel
from / to front A/V
1942
YFIN
CFIN
N.C.
CVBSFIN
AINFL
AINFR
PH-B
7411 NJM2285M
IN1B
CTL1
OUT1
GND2
OUT2
OUT3
CTL3
IN3A
IN1A
GND1
IN2B
V+
CTL2
IN2A
GND3
IN3B
7408 STV6618
VDD
VCC
VCCB-REC
VCCB1
VCCB2
VCCB3
R|PR|COUT-TV
G|YOUT-TV
B|PBOUT-TV
FBOUT-TV
Y|CVBSOUT-TV
CIN-TV
Y|CVBSIN-TV
Y|CVBSIN-TUN
CIN-TUN
C-GATE
DIGOUT1
DIGOUT2
DIGOUT3
DIGOUT4
DIGOUT5
DIGOUT6
SDA
SCL
GNDB-REC
GND2
GND1
GNDB
GNDD
R|PR|CIN-ENC
G|YIN-ENC
B|PBIN-ENC
CVBSIN-ENC
CIN-ENC
YIN-ENC
DECV
Y|CVBSOUT-REC
COUT-AUX
Y|CVBSOUT-AUX
R|PR|CIN-AUX
G|YIN-AUX
B|PBIN-AUX
FBIN-AUX
Y|CVBSIN-AUX
7405 BC847BW
7409 BC847BW
7407 BC847BW
7406 BC857BW
REAR OUT
S-CONN
1948 TCS79
Y
C
7410 NJM2267M
VIN1
VIN2
6DB
VOUT1
VSAG1
VOUT2
VSAG2
1949-C LPR6520
CVBS
1949-B LPR6520
AL
1949-A LPR6520
AR
7415 BC817-25W(COL)
7416 BC817-25W(COL)
AKILL
DAC_MUTE
from DAC_ADC
7419 BSH111
7420 BSH111
7404 BC857BW
7421 BC847BW
7412 PDTC124EU
A_YCVBS
from/to FV, MSP, VPS
1945-3
1945-1
1945-2
1945-4
1947
from/to uP Board
from / to Digital Board
AINFR to IOA
AINFL to IOA
VSA1 to IOA
VSA2 to IOA
ASC1S to IOA
FOME from FOME
SB1 to FV
AGC from FV
PSS to FV
SFS_TS to FV
ION to PS
AIN2R to IOA
AOUT2L from IOA
AOUT2R from IOA
AIN2L to IOA
not used
2
TR 01031_001
150502

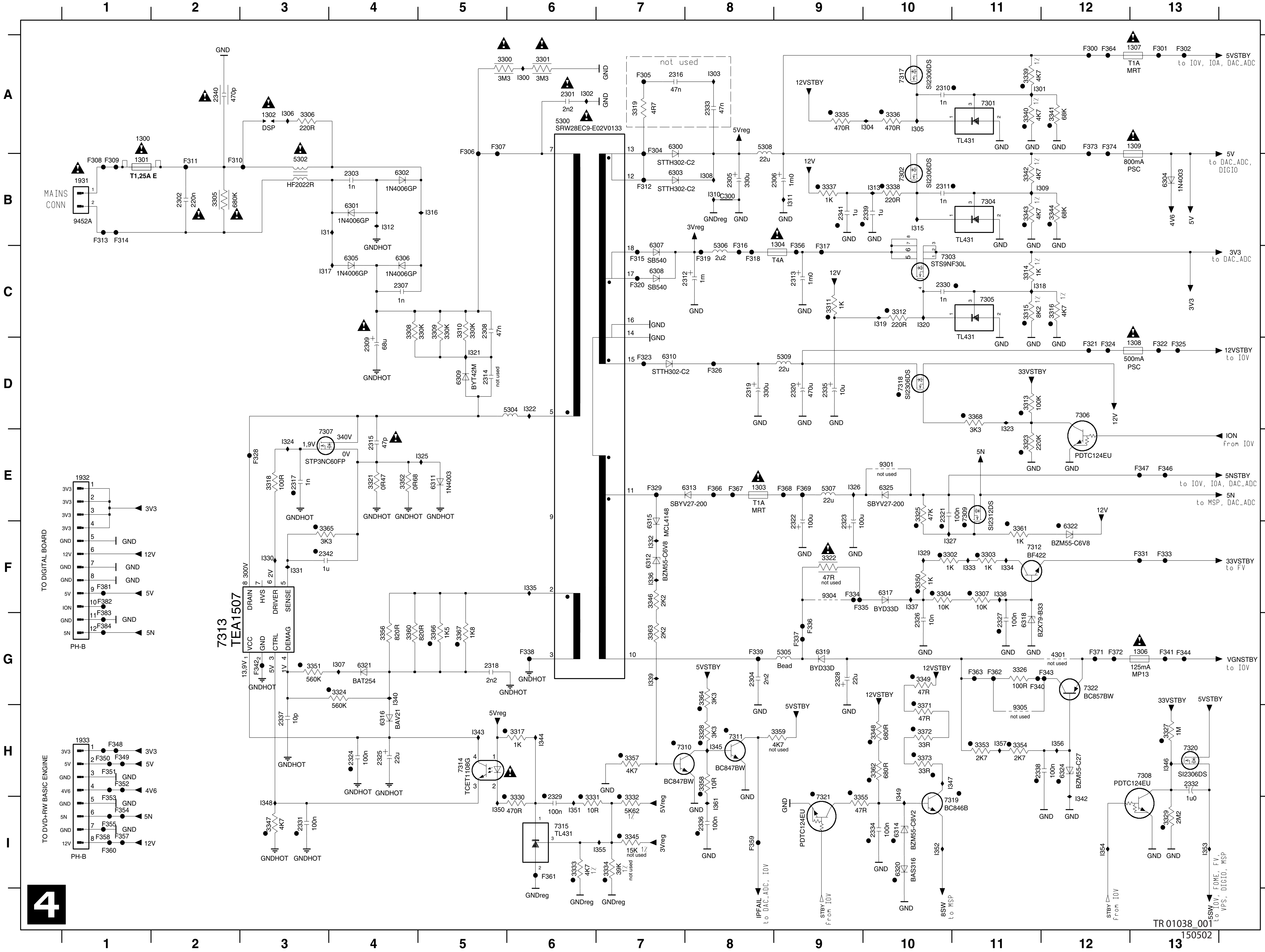
1940-1 A8	6417 B12
1940-2 A13	6418 B12
1940-3 A14	6419 B11
1942 E1	6420 A5
1943 C1	6422 A11
1945-1 I2	6423 A8
1947 I7	6424 B10
1948 F14	6425 G13
1949-A H14	6426 G13
1949-B H14	6427 H13
1949-C G14	6428 H13
2401 B4	6429 I14
2402 B1	7401 B2
2403 D3	7402 B3
2404 D3	7403 B1
2405 C8	7404 I4
2406 I4	7405 C14
2407 I2	7406 F13
2408 F3	7407 E14
2409 D8	7408 D8
2410 C4	7409 D14
2411 D6	7410 G11
2412 I2	7411 D3
2413 C7	7412 H5
2414 C7	7415 I12
2415 C10	7416 I14
2416 G11	7419 H2
2417 F4	7420 H3
2418 F9	7421 H4
2419 E6	F401 H2
2420 F13	F402 H2
2421 E1	F412 I5
2422 F13	F4203 F1
2423 G9	F4205 F2
2424 G13	F4207 F1
2425 G12	F4209 G1
2427 G9	F4210 E1
2428 F2	F4505 I3
2429 H13	F4707 I8
2430 E12	F4712 I9
2432 H13	F4714 I9
2433 E9	F4716 I10
2434 C8	F4718 I10
2435 C7	F4720 I10
2436 E10	F4721 I10
2437 E9	F4722 I10
2438 F9	F485 F14
2439 E9	F499 A3
2440 E9	F5101 B8
2441 E10	F5102 B8
2442 H13	F5103 B7
2443 G13	F5106 B6
2444 H13	F5108 A7
2445 I11	F5110 A5
2446 H6	F5113 A6
2447 I14	F5116 B5
2448 I13	F5119 A5
2449 F1	F5120 B4
2450 B2	F5201 A14
2459 E2	F5202 A13
2460 H11	F5206 A12
2461 G11	F5207 A12
2462 I11	F5208 C12
2463 I13	F5210 A11
2464 A3	F5211 A12
3400 H3	F5213 A12
3401 B11	F5215 A11
3402 B12	F5216 B11
3403 B12	F5219 A11
3404 B4	F5220 F11
3405 B2	F913 D10
3406 B2	I341 A13
3407 B3	I402 D14
3408 B1	I405 H7
3409 B5	I406 B2
3410 C6	I407 B2
3411 B10	I408 B3
3412 C5	I409 B3
3413 B6	I411 D3
3414 C5	I412 D4
3415 H4	I413 C3
3416 H4	I414 D7
3417 C11	I415 F3
3418 I3	I416 F3
3419 I4	I417 E4
3420 F11	I418 H1
3421 C14	I419 I1
3422 D13	I420 I6
3423 D14	I424 I5
3424 E14	I428 I3
3425 E12	I429 I2
3426 E13	I431 I11
3427 C11	I433 I13
3428 E14	I434 I13
3429 E1	I437 G14
3431 E12	I438 G13
3432 C3	I439 G13
3433 C3	I440 F13
3434 F13	I441 H13
3435 F13	I442 G12
3436 F13	I443 G12
3437 G1	I444 H12
3438 G1	I445 H12
3439 F5	I446 H11
3440 H3	I447 G11
3441 H13	I448 G12
3442 D13	I449 F13
3443 I11	I451 F13
3444 I13	I453 H4
3445 E5	I454 I4
3446 B3	I456 C7
3447 A3	I457 C7
3448 I11	I458 A6
3449 F12	I459 A6
3450 I13	I460 A5
3451 I4	I461 E6
3452 G9	I462 E6
3453 D1	I463 E6
3454 A3	I464 E6
3455 D4	I465 E6
3456 I14	I466 E6
3457 I11	I467 D14
3458 H2	I468 G6
3459 G4	I469 G6
3460 H3	I470 G6
3461 A14	I476 F8
3462 A14	I478 E8
3463 A13	I479 E8
3464 A12	I481 E8
3465 B7	I482 E8
3466 B7	I483 E8
3467 B8	I484 F12
3468 B8	I485 I12
3469 B14	I486 I14
3470 B12	
3471 B7	
3472 B8	
3473 I12	
3474 I14	
3475 B9	
3476 B9	
3477 B14	
3478 B14	
3481 F2	
3482 E4	
3483 F3	
3484 F3	
3485 G11	
3486 H11	
3487 H13	
3488 H13	
3489 E1	
3490 D4	
3491 D11	
3492 D11	
3493 D12	
3494 G9	
3495 I11	
3496 I14	
3955 H6	
4401 A9	
4402 E1	
5401 C4	
5402 C9	
5403 C6	
5404 F12	
5406 C8	
6401 B4	
6402 B6	
6403 B6	
6404 B6	
6409 A4	
6414 B5	
6415 B11	
6416 B12	

Analog Board: IN/Out Audio (IOA)


1 2 3 4 5 6 7 8 9
A B C D E F
AIN1L from IOV
AIN1R from IOV
5VSTBY
VSA1 from IOV
VSA2 from IOV
from PS
5NSTBY
2510 100u
2519 100u
AIN2R from IOV
AIN2L from IOV
AINFL from IOV
AINFR from IOV
RSA1 from MSP
RSA2 from MSP
2504 1u
2505 1u
2503 100n
GND
2506 1u
2501 1u
3504 100K
3503 100K
2507 1u
2508 1u
2502 100n
VDD
MSB LSB LOGIC
7501 HEF4052BT
7503 HEF4052BT
7504 HEF4052BT
LL LH HL HH H L
VSS VEE
I503 I502 I501 I504 I505 I506
I511 I515 I516 I513 I514 I517 I518 I521
3506 100K
3505 100K
3534 100K
3507 100K
3510 100K
3511 100K
3516 100K
3514 100K
2509 100n
2514 100n
3532 1K
3533 1K
3535 3K9 not used
3536 3K9 not used
3508 1K
3513 1K
7502-A MC33079
7502-B MC33079
7502-C MC33079
7502-D MC33079
3502 1K
3509 1K
2531 100p not used
2532 100p not used
3501 1K
3512 1K
7505-A MC33078
7505-B MC33078
2521 100n
2530 100n
ALADC to DAC_ADC
ARADC to DAC_ADC
AKILL from IOV
3517 4K7
3519 4K7
7506 BC817-25W(COL)
7508 BC817-25W(COL)
2512 100n
2518 100n
F504
2535 100n
ASC1S from IOV
ASC1M from IOV
2516 100u
2511 100u
I508 I532
F501 F502
3515 1K
3538 3K9 not used
3518 1K
3523 1K
3537 3K9 not used
3526 1K
2522 100u
I535
3522 220R
2523 1n
3524 820R
AOUT1R to IOV
2526 100u
I540 I539
3525 220R
2527 1n
3527 820R
AOUT1L to IOV
2524 1u
2525 1u
I527 I528
AFEL from MSP
AFER from MSP
3530 820R
3531 820R
3520 220R
3521 220R
2520 1n
2517 1n
3528 4K7
3529 4K7
7509 BC817-25W(COL)
7511 BC817-25W(COL)
AKILL from IOV
AOUT2L to IOV
AOUT2R to IOV
2513 1u
2515 1u
ALDAC from DAC_ADC
ARDAC from DAC_ADC
2536 100n
TR 01037_001
150502

2501	A5
2502	A6
2503	A1
2504	A1
2505	A1
2506	A4
2507	A5
2508	A6
2509	B4
2510	A3
2511	E4
2512	D7
2513	F4
2514	C4
2515	F5
2516	E3
2517	F4
2518	E2
2519	A4
2520	F3
2521	C9
2522	E8
2523	E9
2524	F1
2525	F1
2526	F8
2527	F9
2530	C9
2531	B8
2532	C8
2535	D5
2536	F5
3501	B8
3502	B8
3503	A5
3504	A4
3505	C6
3506	B5
3507	C1
3508	C3
3509	C8
3510	D1
3511	D1
3512	D8
3513	D3
3514	E1
3515	D7
3516	E1
3517	D8
3518	E7
3519	E8
3520	F3
3521	F4
3522	E9
3523	E7
3524	E9
3525	F9
3526	F7
3527	F9
3528	F2
3529	F3
3530	F2
3531	F4
3532	C3
3533	D3
3534	C1
3535	C3
3536	D3
3537	F7
3538	E7
7501	A7
7502-A	C4
7502-B	D4
7502-C	E7
7502-D	D7
7503	B2
7504	D5
7505-A	B9
7505-B	C8
7506	D9
7508	E9
7509	F2
7511	F4
F501	E2
F502	F2
F504	D2
I501	C1
I502	C1
I503	B1
I504	D1
I505	B2
I506	B2
I508	E4
I511	C3
I513	C6
I514	C6
I515	B6
I516	B6
I517	B8
I518	C8
I521	D6
I527	F1
I528	F1
I532	E4
I535	E8
I539	F8
I540	F8

Analog Board: Power Supply (PS)


1
2
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9
10
11
12
13
A
B
C
D
E
F
G
H
I
MAINS CONN
1931
9452A
1300
1301
T1,25A E
F308
F309
F311
F310
F313
F314
2302 220n
2340 470p
3305 680K
1302 DSP
3306 220R
5302 HF2022R
2303 1n
6301 1N4006GP
6302 1N4006GP
6305 1N4006GP
6306 1N4006GP
2307 1n
GNDHOT
2309 68u
3308 330K
3309 330K
3310 330K
2308 47n
6309 BYT42M
2314 not used
3300 3M3
3301 3M3
2301 2n2
5300 SRW28EC9-E02V0133
not used
2316 47n
3319 4R7
2333 47n
6300 STTH302-C2
6303 STTH302-C2
6307 SB540
6308 SB540
6310 STTH302-C2
5vreg
3Vreg
2305 330u
2306 1m0
C300
GNDreg
5308 22u
5306 2u2
1304 T4A
2312 1m
2313 1m0
5309 22u
2319 330u
2320 470u
2335 10u
12VSTBY
12V
3335 470R
3336 470R
7317 SI2306DS
7302 SI2306DS
7318 SI2306DS
7303 STS9NF30L
TL431
7301
7304
7305
3337 1K
3338 220R
3311 1K
3312 220R
2341 1u
2339 1u
2310 1n
2311 1n
2330 1n
3339 4K7
3340 4K7
3341 68K
3342 4K7
3343 4K7
3344 68K
3314 1K
3315 8K2
3316 4K7
1307 T1A MRT
1309 800mA PSC
1308 500mA PSC
6304 1N4003
5VSTBY to IOV, IOA, DAC_ADC
5V to DAC_ADC, DIGIO
3V3 to DAC_ADC
12VSTBY to IOV
4V6
33VSTBY
3313 100K
3368 3K3
3323 220K
7306 PDTC124EU
ION from IOV
7307 STP3NC60FP
340V
1,9V
0V
2315 47p
3318 100R
2317 1n
3321 0R47
3352 0R68
6311 1N4003
3365 3K3
2342 1u
7313 TEA1507
DRAIN
HVS
DRIVER
SENSE
VCC
GND
CTRL
DEMAG
300V
2V
13,9V
5V
1V
3356 820R
3360 820R
3366 1K5
3367 1K8
2318 2n2
3351 560K
6321 BAT254
3324 560K
6316 BAV21
2337 10p
2324 100n
2325 22u
2331 100n
3347 4K7
7314 TCET1108G
3317 1K
5Vreg
3330 470R
2329 100n
3331 10R
3332 5K62 1%
3345 15K 1%
7315 TL431
3333 4K7 1%
3334 39K 1% not used
F361
6313 SBYV27-200
6315 MCL4148
6312 BZM55-C6V8
3346 2K2
3363 2K2
1303 T1A MRT
5307 22u
2322 100u
2323 100u
6325 SBYV27-200
9301 not used
5N
3325 47K
2321 100n
7309 SI2312DS
3361 1K
6322 BZM55-C6V8
7312 BF422
3322 47R not used
9304
6317 BYD33D
3302 1K
3303 1K
3350 1K
3304 10K
3307 10K
2326 10n
2327 100n
6318 BZX79-B33
5305 Bead
6319 BYD33D
2304 2n2
2328 22u
5VSTBY
3364 3K3
3328 3K3
7310 BC847BW
7311 BC847BW
3359 4K7 not used
3357 4K7
3358 10R
2336 100n
IPFAIL to DAC_ADC, IOV
7321 PDTC124EU
STBY from IOV
3349 47R
3371 47R
3372 33R
3373 33R
3348 680R
3362 680R
3355 47R
7319 BC846B
2334 100n
6314 BZM55-C8V2
6320 BAS316
8SW to MSP
3326 100R
9305 not used
7322 BC857BW
3353 2K7
3354 2K7
2338 100n
6324 BZM55-C27
4301 not used
1306 125mA MP13
VGNSTBY to IOV
5NSTBY to IOV, IOA, DAC_ADC
5N to MSP, DAC_ADC
33VSTBY to FV
3327 1M
7320 SI2306DS
7308 PDTC124EU
2332 1u0
3329 2M2
STBY from IOV
5SW to IOV, FDME, FV, VPS, DIGIO, MSP
1932
1933
TO DIGITAL BOARD
TO DVD+RW BASIC ENGINE
PH-B
3V3
GND
12V
5V
ION
5N
4V6
TR 01038_001
150502
4

1300	A1
1301	B1
1302	A3
1303	E8
1304	C9
1306	G13
1307	A13
1308	D13
1309	A13
1931	B1
1932	E1
1933	H1
2301	A6
2302	B2
2303	B4
2304	G8
2305	B8
2306	B9
2307	C4
2308	C5
2309	D4
2310	A10
2311	B10
2312	C8
2313	C9
2314	D5
2315	E4
2316	A7
2317	E3
2318	G5
2319	D8
2320	D9
2321	E10
2322	F9
2323	F9
2324	H4
2325	H4
2326	G10
2327	G11
2328	G9
2329	I6
2330	C10
2331	I3
2332	H13
2333	A8
2334	I10
2335	D9
2336	I8
2337	H3
2338	H11
2339	B10
2340	A2
2341	B9
2342	F3
3300	A5
3301	A6
3302	F10
3303	F11
3304	F10
3305	B2
3306	A3
3307	F11
3308	C4
3309	C5
3310	C5
3311	C9
3312	C10
3313	D11
3314	C11
3315	C11
3316	C12
3317	H6
3318	E3
3319	A7
3321	E4
3322	F9
3323	E11
3324	G4
3325	E10
3326	G11
3327	H13
3328	H8
3329	I13
3330	I6
3331	I6
3332	I7
3333	I6
3334	I7
3335	A9
3336	A10
3337	B9
3338	B10
3339	A11
3340	A11
3341	A12
3342	B11
3343	B11
3344	B12
3345	I7
3346	F7
3347	I3
3348	H10
3349	G10
3350	F10
3351	G3
3352	E4
3353	H11
3354	H11
3355	I9
3356	G4
3357	H7
3358	H8
3359	H9
3360	G4
3361	F11
3362	H10
3363	G7
3364	G8
3365	F3
3366	G5
3367	G5
3368	D11
3371	H10
3372	H10
3373	H10
4301	G12
5300	A6
5302	B3
5304	D6
5305	G9
5306	C8
5307	E9
5308	A8
5309	D9
6300	A7
6301	B4
6302	B4
6303	B7
6304	B13
6305	C4
6306	C4
6307	C7
6308	C7
6309	D5
6310	D7
6311	E5
6312	F7
6313	E8
6314	I10
6315	E7
6316	H4
6317	F10
6318	G11
6319	G9
6320	I10
6321	G4
6322	F12
6324	H12
6325	E10
7301	A11
7302	B10
7303	C10
7304	B11
7305	C11
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7307	E3
7308	H13
7309	E11
7310	H7
7311	H8
7312	F11
7313	G2
7314	H5
7315	I6
7317	A10
7318	D10
7319	I10
7320	H13
7321	I9
7322	G12
9301	E10
9304	F9
9305	H11
C300	B8
F300	A12
F301	A13
F302	A13
F304	A7
F305	A7
F306	B5
F307	A5
F308	B1
F309	B1
F310	B2
F311	B2
F312	B7
F313	B1
F314	B1
F315	C7
F316	C8
F317	C9
F318	C8
F319	C8
F320	C7
F321	D12
F322	D13
F323	D7
F324	D12
F325	D13
F326	D8
F328	E3
F329	E7
F331	F13
F333	F13
F334	F9
F335	F9
F336	G9
F337	G9
F338	G6
F339	G8
F340	G11
F341	G13
F342	G3
F343	G12
F344	G13
F346	E13
F347	E13
F348	H1
F349	H1
F350	H1
F351	H1
F352	H1
F353	I1
F354	I1
F355	I1
F356	C9
F357	I1
F358	I1
F359	I8
F360	I1
F361	I6
F362	G11
F363	G11
F364	A12
F366	E8
F367	E8
F368	E9
F369	E9
F371	G12
F372	G12
F373	A12
F374	A12
F381	F1
F382	F1
F383	G1
F384	G1
I300	A6
I301	A11
I302	A6
I303	A8
I304	A10
I305	A10
I306	A3
I307	G4
I308	B8
I309	B12
I310	B8
I311	B9
I312	B4
I313	B10
I314	B3
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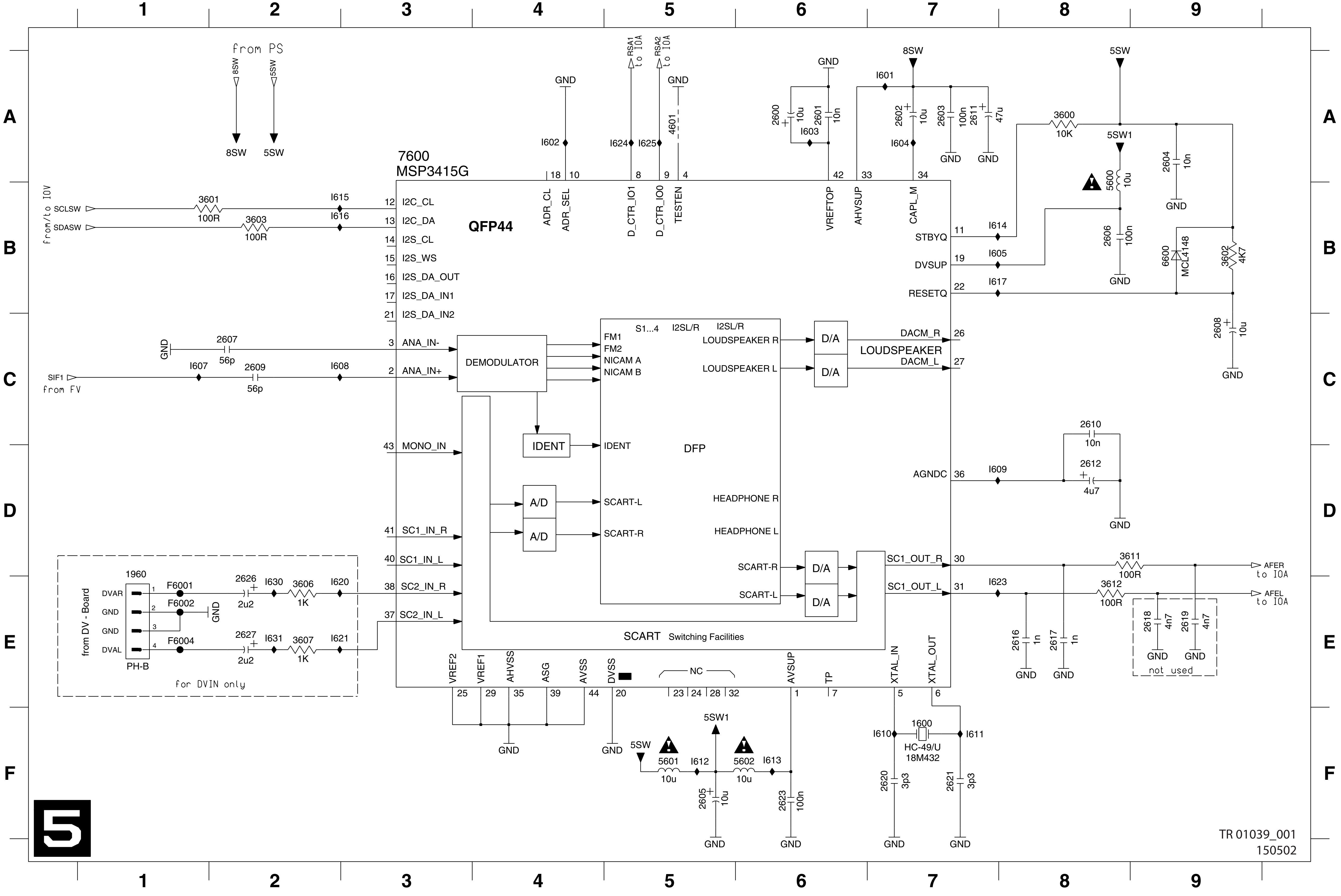
I317	C3
I318	C11
I319	C10
I320	C10
I321	D5
I322	D6
I323	D11
I324	E3
I325	E5
I326	E9
I327	F10
I329	F10
I330	F3
I331	F3
I332	F7
I333	F11
I334	F11
I335	F6
I336	F7
I337	F10
I338	F11
I339	G7
I340	G4
I342	I12
I343	H5
I344	H6
I345	H8
I346	H13
I347	H10
I348	I3
I349	H10
I350	I5
I351	I6
I352	I10
I353	I13
I354	I12
I355	I7
I356	H12
I357	H11
I361	I8

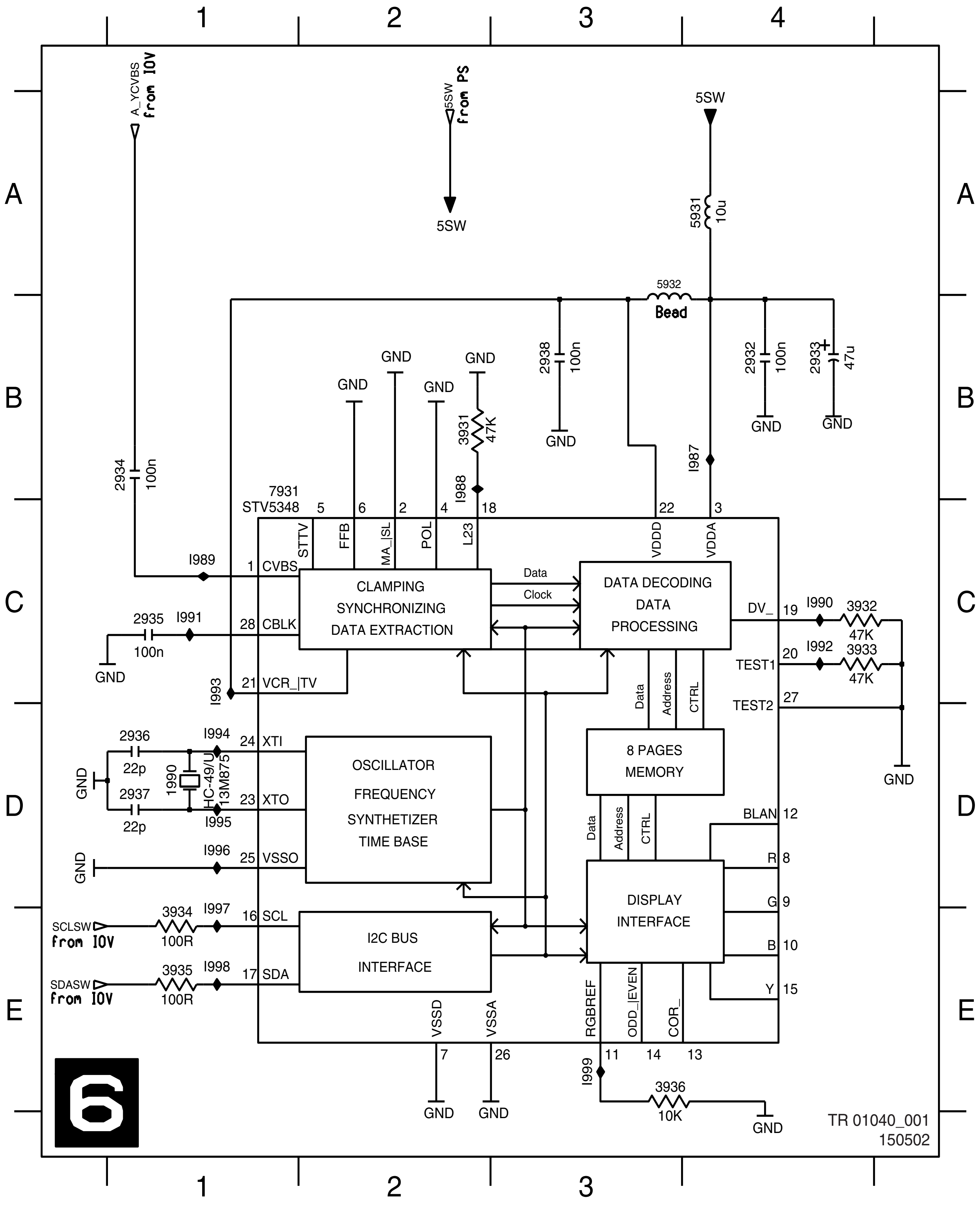
Analog Board: Multi Sound Processing (MSP)


from PS
8SW
5SW
7600
MSP3415G
QFP44
from/to IOV
SCLSW
SDASW
3601 100R
3603 100R
I615
I616
12 I2C_CL
13 I2C_DA
14 I2S_CL
15 I2S_WS
16 I2S_DA_OUT
17 I2S_DA_IN1
21 I2S_DA_IN2
3 ANA_IN-
2 ANA_IN+
43 MONO_IN
41 SC1_IN_R
40 SC1_IN_L
38 SC2_IN_R
37 SC2_IN_L
GND
2607 56p
2609 56p
I607
I608
SIF1
from FV
18 ADR_CL
10 ADR_SEL
8 D_CTR_IO1
9 D_CTR_IO0
4 TESTEN
I602
I624
I625
RSA1 to IOA
RSA2 to IOA
4601
42 VREFTOP
33 AHVSUP
34 CAPL_M
2600 10u
2601 10n
I603
I601
2602 10u
2603 100n
2611 47u
I604
11 STBYQ
19 DVSUP
22 RESETQ
I614
I605
I617
3600 10K
5SW1
5600 10u
2606 100n
2604 10n
6600 MCL4148
3602 4K7
2608 10u
DEMODULATOR
IDENT
DFP
S1...4
I2SL/R
FM1
FM2
NICAM A
NICAM B
LOUDSPEAKER R
LOUDSPEAKER L
D/A
LOUDSPEAKER
DACM_R 26
DACM_L 27
A/D
SCART-L
SCART-R
HEADPHONE R
HEADPHONE L
SC1_OUT_R 30
SC1_OUT_L 31
SCART Switching Facilities
36 AGNDC
I609
2610 10n
2612 4u7
3611 100R
3612 100R
I623
AFER to IOA
AFEL to IOA
2616 1n
2617 1n
2618 4n7
2619 4n7
not used
1960
from DV - Board
DVAR
GND
GND
DVAL
PH-B
F6001
F6002
F6004
2626 2u2
2627 2u2
I630
I631
3606 1K
3607 1K
I620
I621
for DVIN only
VREF2 25
VREF1 29
AHVSS 35
ASG 39
AVSS 44
DVSS 20
NC 23 24 28 32
AVSUP 1
TP 7
XTAL_IN 5
XTAL_OUT 6
5601 10u
5602 10u
I612
I613
2605 10u
2623 100n
1600 HC-49/U 18M432
I610
I611
2620 3p3
2621 3p3
TR 01039_001
150502
5

1600	F7
1960	E1
2600	A6
2601	A6
2602	A7
2603	A7
2604	A9
2605	F5
2606	B8
2607	C2
2608	C9
2609	C2
2610	C8
2611	A7
2612	D8
2616	E8
2617	E8
2618	E9
2619	E9
2620	F7
2621	F7
2623	F6
2626	E2
2627	E2
3600	A8
3601	B1
3602	B9
3603	B2
3606	E2
3607	E2
3611	D8
3612	E8
4601	A5
5600	A8
5601	F5
5602	F6
6600	B9
7600	A3
F6001	E1
F6002	E1
F6004	E1
I601	A7
I602	A4
I603	A6
I604	A7
I605	B7
I607	C1
I608	C2
I609	D7
I610	F7
I611	F7
I612	F5
I613	F6
I614	B7
I615	B2
I616	B2
I617	B7
I620	E2
I621	E2
I623	E7
I624	A5
I625	A5
I630	E2
I631	E2

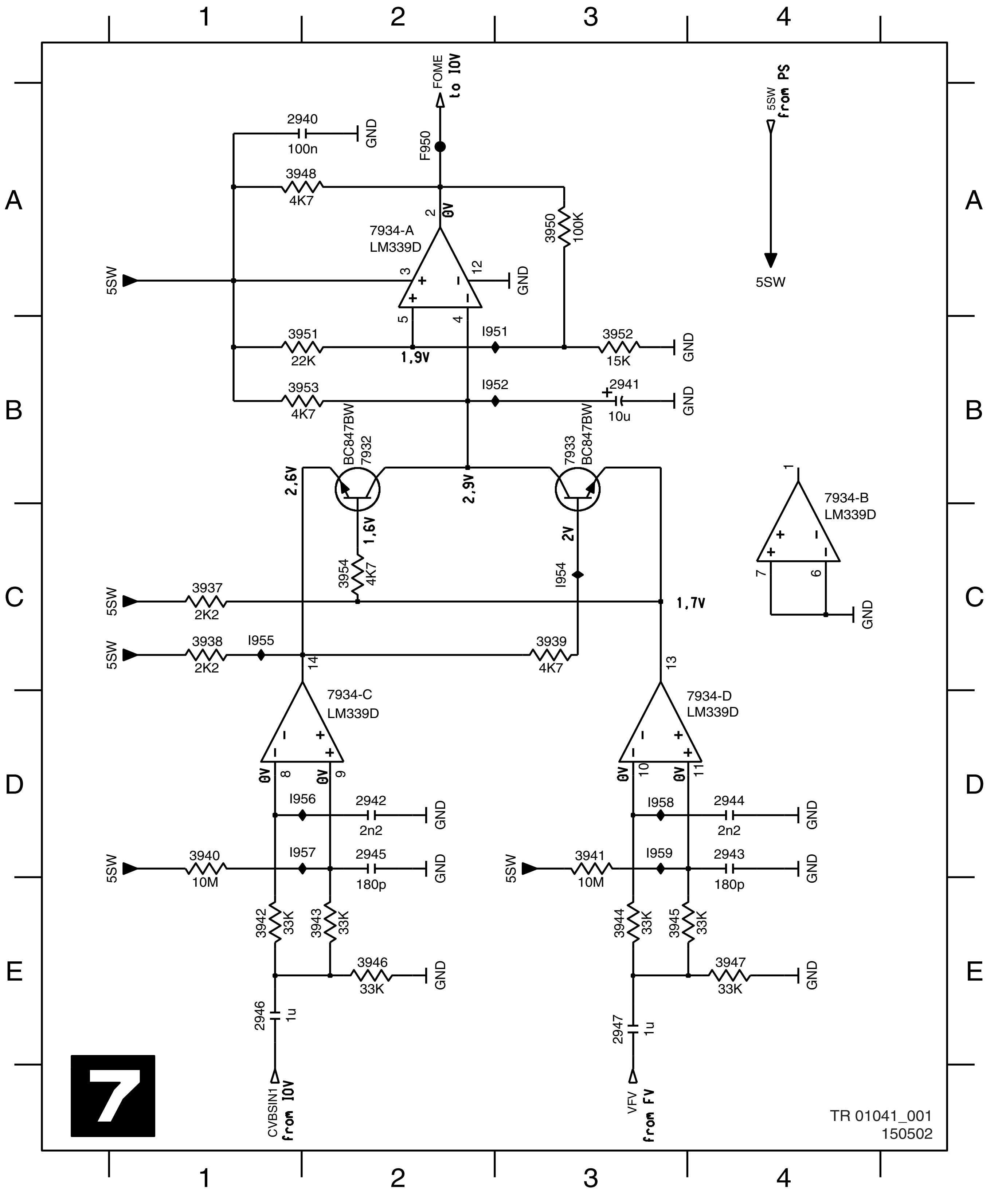
Analog Board: VPS (VPS)

1990 D1	2934 B1	2937 D1	3932 C4	3935 E1	5932 A3	I988 B2	I991 C1	I994 D1	I997 E1
2932 B4	2935 C1	2938 B3	3933 C4	3936 E3	7931 B2	I989 C1	I992 C4	I995 D1	I998 E1
2933 B4	2936 D1	3931 B2	3934 E1	5931 A4	I987 B4	I990 C4	I993 C1	I996 D1	I999 E3


1
2
3
4
A
B
C
D
E
A_YCVBS
from 10V
5SW
from PS
5SW
5SW
5931
10u
5932
Bead
GND
GND
GND
GND
3931
47K
2938
100n
GND
2932
100n
2933
47u
GND
GND
I987
I988
2934
100n
7931
STV5348
5
6
2
4
18
22
3
STTV
FFB
MA_ISL
POL
L23
VDDD
VDDA
I989
1
CVBS
CLAMPING
SYNCHRONIZING
DATA EXTRACTION
Data
Clock
DATA DECODING
DATA
PROCESSING
DV_
19
I990
3932
47K
2935
100n
I991
28
CBLK
GND
I993
21
VCR_ITV
TEST1
20
I992
3933
47K
TEST2
27
GND
2936
22p
I994
24
XTI
OSCILLATOR
FREQUENCY
SYNTHETIZER
TIME BASE
Data
Address
CTRL
8 PAGES
MEMORY
GND
1990
HC-49/U
13M875
2937
22p
I995
23
XTO
Data
Address
CTRL
BLAN
12
GND
I996
25
VSSO
R
8
DISPLAY
INTERFACE
G
9
SCLSW
from 10V
3934
100R
I997
16
SCL
I2C BUS
INTERFACE
B
10
SDASW
from 10V
3935
100R
I998
17
SDA
Y
15
VSSD
VSSA
RGBREF
ODD_IEVEN
COR_
7
26
11
14
13
I999
3936
10K
GND
GND
GND
TR 01040_001
150502
6

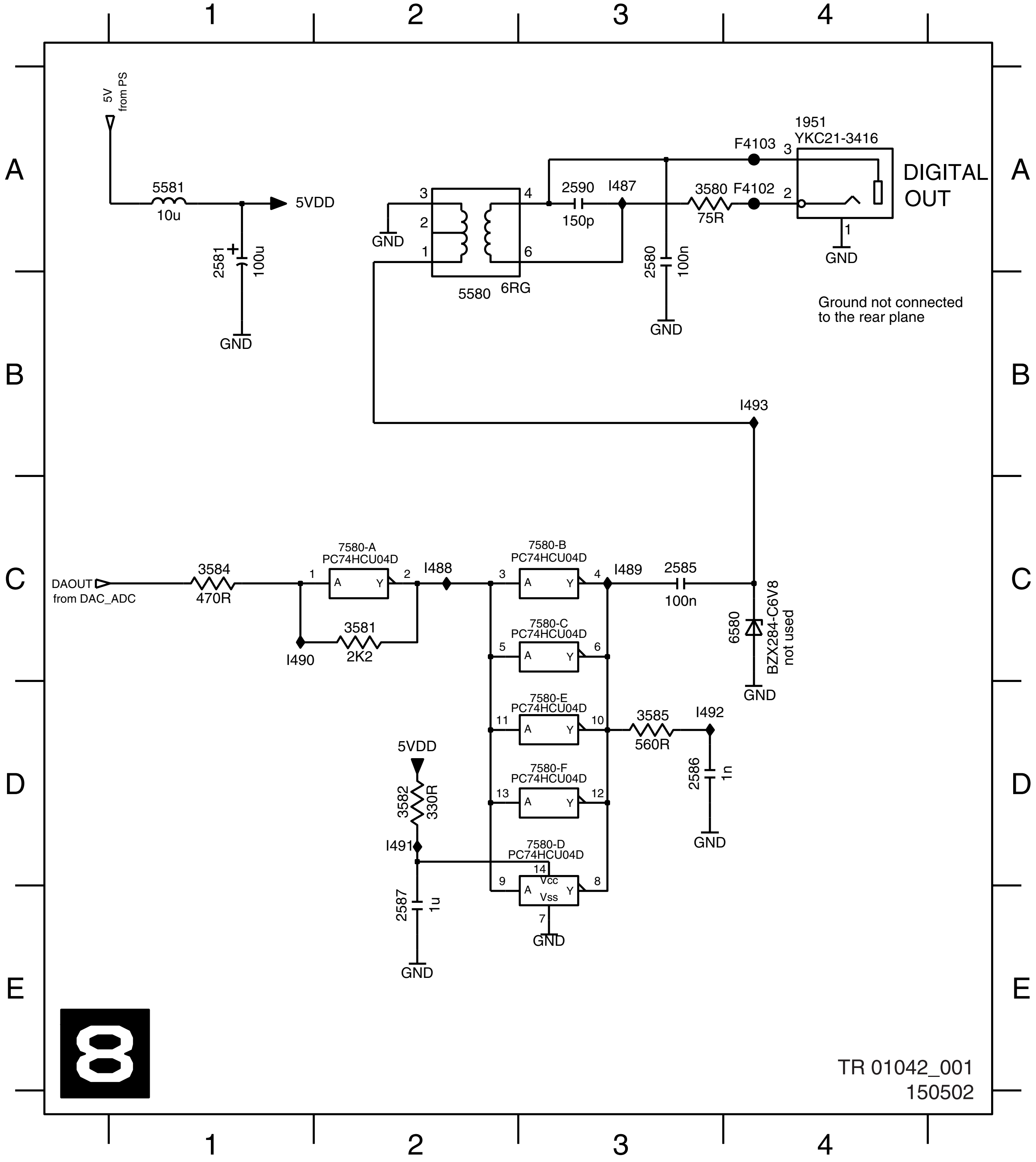
Analog Board: Follow Me (FOME)

2940 A2	2944 D4	3937 C1	3941 D3	3945 E3	3950 A3	3954 C2	7934-B B4	I951 B3	I956 D2
2941 B3	2945 D2	3938 C1	3942 E1	3946 E2	3951 B2	7932 B2	7934-C C2	I952 B3	I957 D2
2942 D2	2946 E1	3939 C3	3943 E2	3947 E4	3952 B3	7933 B3	7934-D D3	I954 C3	I958 D3
2943 D4	2947 E3	3940 D1	3944 E3	3948 A1	3953 B2	7934-A A2	F950 A2	I955 C1	I959 D3


1
2
3
4
A
B
C
D
E
FOME
to 10V
F950
2940
100n
GND
3948
4K7
7934-A
LM339D
2
0V
3
12
GND
5SW
3950
100K
5SW
from PS
5SW
5
4
3951
22K
1,9V
I951
3952
15K
GND
3953
4K7
I952
2941
10u
GND
BC847BW
7932
2,6V
2,9V
7933
BC847BW
1,6V
2V
3954
4K7
I954
7934-B
LM339D
1
7
6
GND
5SW
3937
2K2
1,7V
5SW
3938
2K2
I955
3939
4K7
14
13
7934-C
LM339D
7934-D
LM339D
0V
8
0V
9
0V
10
0V
11
I956
2942
2n2
GND
I958
2944
2n2
GND
5SW
3940
10M
I957
2945
180p
GND
5SW
3941
10M
I959
2943
180p
GND
3942
33K
3943
33K
3946
33K
GND
3944
33K
3945
33K
3947
33K
GND
2946
1u
2947
1u
CVBSIN1
from 10V
VFV
from FV
TR 01041_001
150502
7

Analog Board: Digital In/Out (DIGIO)

1951 A4	2585 C3	2590 A3	3582 D2	5580 B2	7580-A C2	7580-D D3	F4102 A4	I488 C2	I491 D2
2580 A3	2586 D3	3580 A3	3584 C1	5581 A1	7580-B C3	7580-E D3	F4103 A4	I489 C3	I492 D3
2581 A1	2587 E2	3581 C2	3585 D3	6580 C4	7580-C C3	7580-F D3	I487 A3	I490 C1	I493 B4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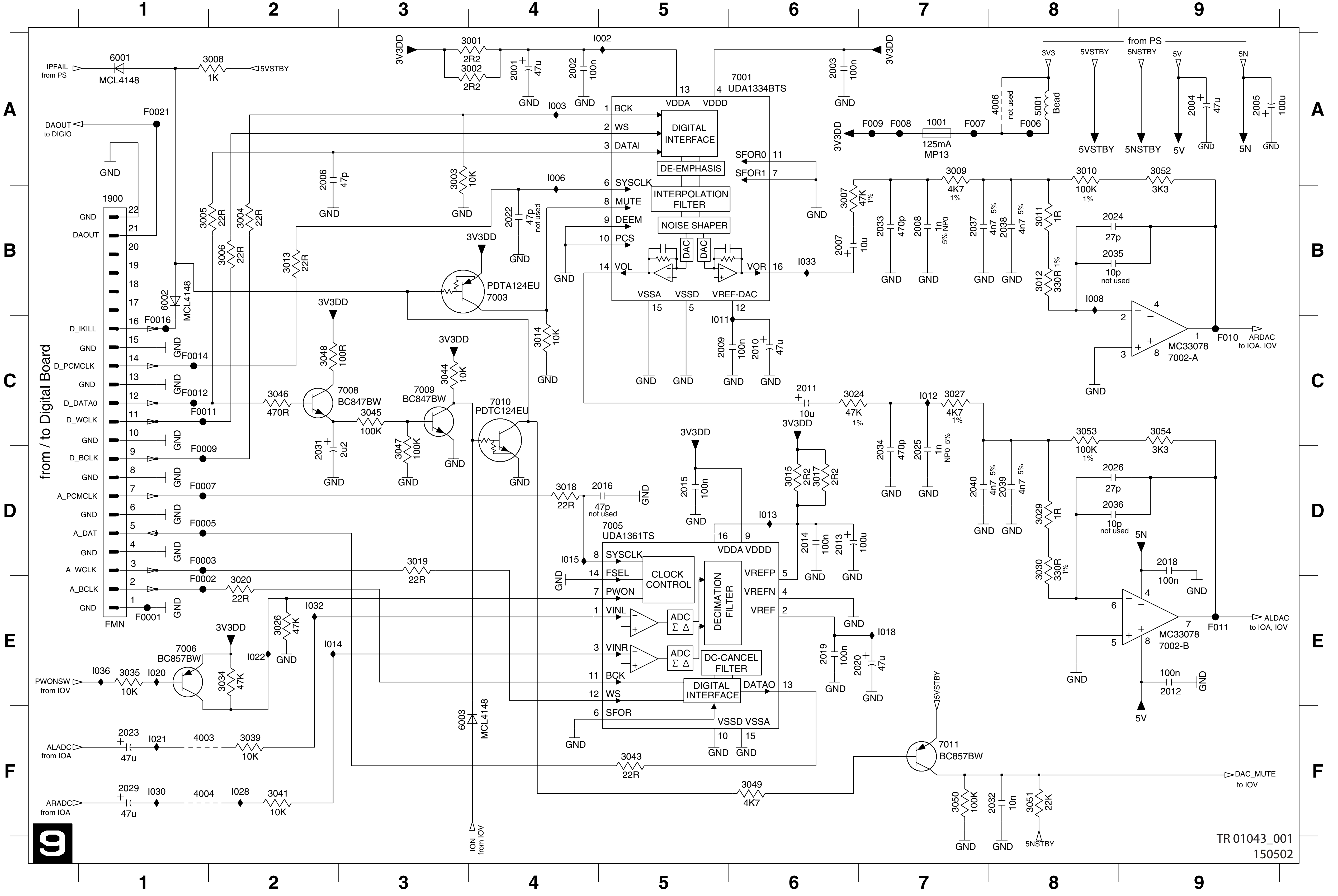
2
3
4
A
B
C
D
E
5V
from PS
5581
10u
5VDD
2581
100u
GND
3
2
1
4
6
GND
5580
6RG
2590
150p
I487
3580
75R
F4102
F4103
1951
YKC21-3416
3
2
1
DIGITAL
OUT
GND
2580
100n
GND
Ground not connected
to the rear plane
I493
DAOUT
from DAC_ADC
3584
470R
7580-A
PC74HCU04D
1
A
Y
2
I488
3581
2K2
I490
7580-B
PC74HCU04D
3
4
I489
2585
100n
6580
BZX284-C6V8
not used
GND
7580-C
PC74HCU04D
5
6
7580-E
PC74HCU04D
11
10
3585
560R
I492
2586
1n
GND
7580-F
PC74HCU04D
13
12
5VDD
3582
330R
I491
7580-D
PC74HCU04D
14
Vcc
Vss
9
8
7
GND
2587
1u
GND
8
TR 01042_001
150502

Analog Board: Audio Converter(DAC_ADC)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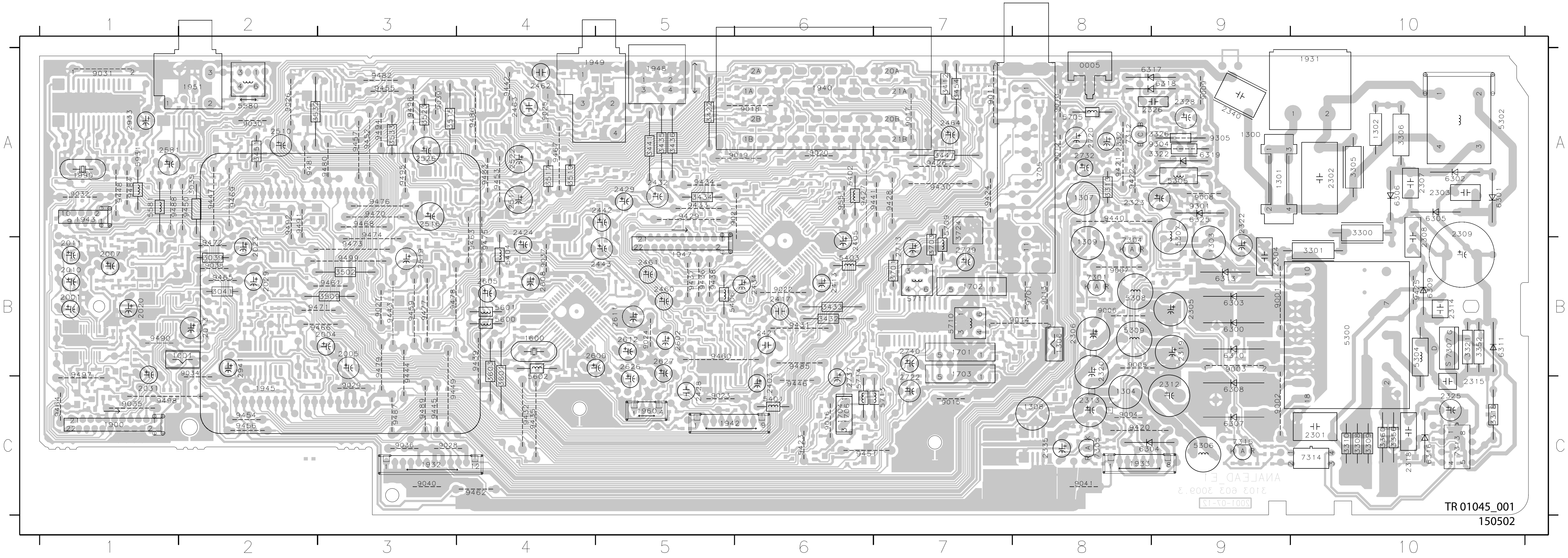
5
6
7
8
9
A
B
C
D
E
F
IPFAIL from PS
6001 MCL4148
3008 1K
5VSTBY
DAOUT to DIGIO
F0021
GND
1900
FMN
from / to Digital Board
GND
DAOUT
D_IKILL
GND
D_PCMCLK
GND
D_DATA0
D_WCLK
GND
D_BCLK
GND
A_PCMCLK
GND
A_DAT
GND
A_WCLK
A_BCLK
GND
F0016
F0014
F0012
F0011
F0009
F0007
F0005
F0003
F0002
F0001
6002 MCL4148
3005 22R
3004 22R
3006 22R
3013 22R
2006 47p
3V3DD
3001 2R2
3002 2R2
2001 47u
2002 100n
I002
I003
3003 10K
I006
2022 47p not used
7001 UDA1334BTS
BCK
WS
DATAI
SYSCLK
MUTE
DEEM
PCS
VOL
VDDA
VDDD
DIGITAL INTERFACE
DE-EMPHASIS
INTERPOLATION FILTER
NOISE SHAPER
DAC
SFOR0
SFOR1
VOR
VSSA
VSSD
VREF-DAC
I011
2009 100n
2010 47u
2003 100n
3V3DD
PDTA124EU 7003
3048 100R
7008 BC847BW
3046 470R
3045 100K
2031 2u2
3047 100K
7009 BC847BW
3044 10K
7010 PDTC124EU
3014 10K
3018 22R
2016 47p not used
3019 22R
3020 22R
I032
3026 47K
I022
I014
7006 BC857BW
3034 47K
PWONSW from IOV
I036
3035 10K
I020
6003 MCL4148
ION from IOV
ALADC from IOA
2023 47u
I021
4003
3039 10K
ARADC from IOA
2029 47u
I030
4004
I028
3041 10K
7005 UDA1361TS
SYSCLK
FSEL
PWON
VINL
VINR
BCK
WS
SFOR
CLOCK CONTROL
DECIMATION FILTER
ADC Σ Δ
DC-CANCEL FILTER
DIGITAL INTERFACE
VDDA VDDD
VREFP
VREFN
VREF
DATAO
VSSD VSSA
I015
2015 100n
I013
3015 2R2
3017 2R2
2014 100n
2013 100u
2019 100n
2020 47u
I018
3043 22R
3049 4K7
7011 BC857BW
5VSTBY
DAC_MUTE to IOV
3050 100K
2032 10n
3051 22K
5NSTBY
from PS
3V3
5VSTBY
5NSTBY
5V
5N
4006 not used
5001 Bead
3V3DD
F009
F008
1001 125mA MP13
F007
F006
2004 47u
2005 100u
3007 47K 1%
2007 10u
I033
2033 470p
2008 1n 5% NP0
3009 4K7 1%
2037 4n7 5%
2038 4n7 5%
3011 1R
3012 330R 1%
3010 100K 1%
3052 3K3
2024 27p
2035 10p not used
I008
MC33078 7002-A
F010
ARDAC to IOA, IOV
2011 10u
3024 47K 1%
2034 470p
I012
2025 1n NP0 5%
3027 4K7 1%
2040 4n7 5%
2039 4n7 5%
3053 100K 1%
3054 3K3
2026 27p
2036 10p not used
3029 1R
3030 330R 1%
2018 100n
MC33078 7002-B
F011
ALDAC to IOA, IOV
2012 100n
GND
TR 01043_001 150502

1001	A7
1900	B1
2001	A4
2002	A4
2003	A6
2004	A9
2005	A9
2006	A2
2007	B6
2008	B7
2009	C5
2010	C6
2011	C6
2012	E9
2013	D6
2014	D6
2015	D5
2016	D5
2018	D9
2019	E6
2020	E7
2022	B4
2023	F1
2024	B8
2025	D7
2026	D8
2029	F1
2031	D2
2032	F7
2033	B7
2034	D7
2035	B8
2036	D8
2037	B7
2038	B8
2039	D8
2040	D7
3001	A4
3002	A4
3003	A3
3004	B2
3005	B1
3006	B2
3007	B6
3008	A2
3009	A7
3010	A8
3011	B8
3012	B8
3013	B2
3014	C4
3015	D6
3017	D6
3018	D4
3019	D3
3020	E2
3024	C6
3026	E2
3027	C7
3029	D8
3030	D8
3034	E2
3035	E1
3039	F2
3041	F2
3043	F5
3044	C3
3045	C3
3046	C2
3047	D3
3048	C2
3049	F6
3050	F7
3051	F7
3052	A9
3053	C8
3054	C9
4003	F1
4004	F1
4006	A8
5001	A8
6001	A1
6002	B1
6003	F3
7001	A6
7002-A	C9
7002-B	E9
7003	B4
7005	D5
7006	E1
7008	C2
7009	C3
7010	C4
7011	F6
F0001	E1
F0002	E1
F0003	D1
F0005	D1
F0007	D1
F0009	D1
F0011	C1
F0012	C1
F0014	C1
F0016	C1
F0021	A1
F006	A8
F007	A7
F008	A7
F009	A7
F010	C9
F011	E9
I002	A5
I003	A4
I006	A4
I008	B8
I011	C5
I012	C7
I013	D6
I014	E2
I015	D4
I018	E7
I020	E1
I021	F1
I022	E2
I028	F2
I030	F1
I032	E2
I033	B6
I036	E1

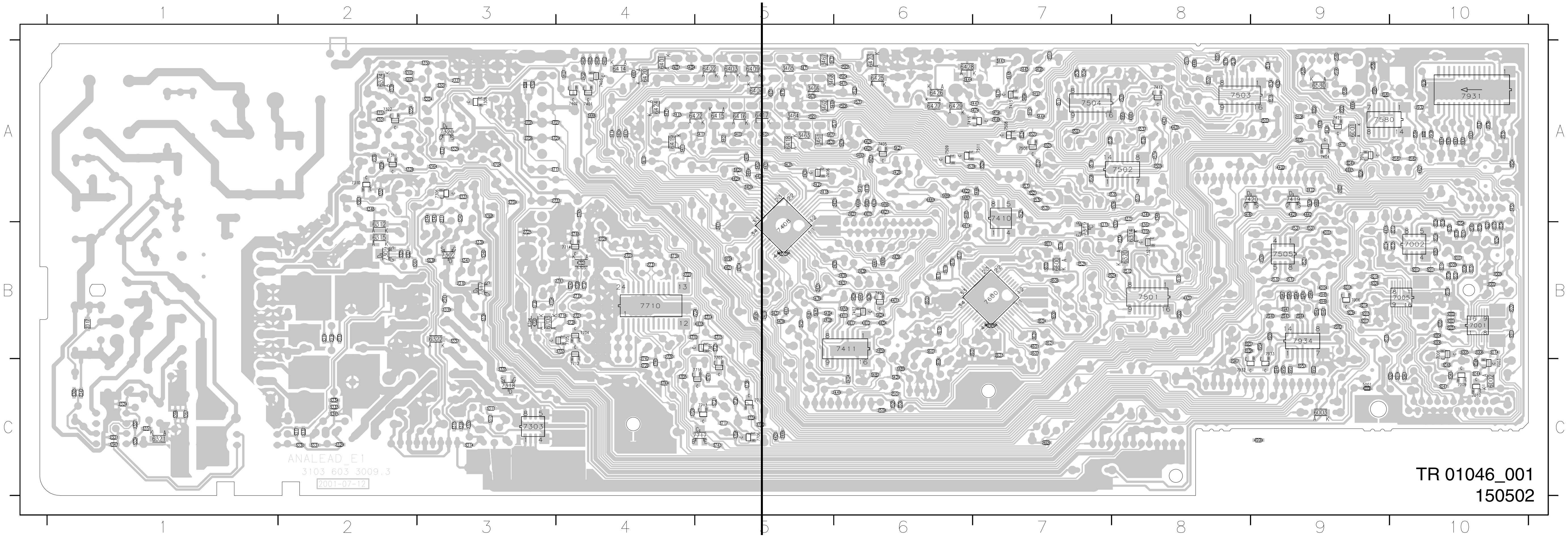
Layout Analog Board (Top View)

0005	A8
1001	B2
1300	A9
1301	A9
1302	A10
1303	B9
1304	C8
1306	B8
1307	A8
1308	C8
1309	B8
1600	B4
1701	B7
1702	B7
1703	B7
1704	C6
1705	A8
1706	C6
1900	C1
1931	A10
1932	C3
1933	C8
1940	A6
1942	C5
1943	A1
1945	C2
1947	B5
1948	A5
1949	A4
1951	A2
1960	C5
1990	A1
2001	B1
2004	B3
2005	B3
2007	B1
2010	B1
2011	B1
2013	B2
2020	B1
2023	B2
2029	B2
2031	C1
2301	C10
2302	A10
2303	A10
2304	B9
2305	B9
2306	B8
2307	A10
2308	B10
2309	A10
2312	C9
2313	C8
2314	B10
2315	C10
2318	C10
2319	B9
2320	B8
2322	A9
2323	A8
2325	C10
2326	A9
2328	A9
2332	A8
2335	C8
2340	A9
2403	C6
2405	B6
2413	B6
2417	B6
2421	B6
2424	A4
2428	C5
2429	A5
2432	A5
2434	B6
2442	A5
2443	B5
2460	B5
2461	B5
2462	A4
2463	A4
2464	A7
2510	A2
2511	A4
2516	A3
2519	B3
2522	A4
2526	A3
2581	A1
2600	B5
2602	B5
2605	B4
2608	B4
2611	B5
2612	B5
2626	B5
2627	B5
2713	B7
2720	A8
2722	C7
2729	B7
2732	A8
2737	C6
2740	B7
2933	A1
2941	B2
3035	A2
3039	B2
3041	B2
3300	A10
3301	B10
3305	A10
3306	A10
3308	C10
3309	C10
3310	C10
3313	A8
3318	C10
3321	B10
3322	A9
3326	A9
3352	B10
3356	C10
3360	C10
3412	A7
3422	A5
3432	B6
3433	B6
3434	A5
3435	A5
3436	A5
3441	A5
3447	A7
3451	A2
3454	A7
3502	B3
3509	B3
3515	A3
3517	A4
3519	A4
3523	A3
3532	A2
3533	A3
3601	B4
3603	B4
3701	B7
3703	B7
3724	A7
5300	B10
5302	A10
5304	B10
5305	A9
5306	C9
5307	A9
5308	B8
5309	B8
5401	C6
5402	A6
5403	B6
5404	B4
5406	B5
5580	A2
5581	A1
5600	B4
5601	B4
5602	C4
5705	A8
5709	A7
5710	B7
5711	B7
5713	C7
5714	C6
5931	A1
6300	B9
6301	A10
6302	A10
6303	B9
6304	C8
6305	A10
6306	A10
6307	C9
6308	C9
6309	B10
6310	B9
6311	B10
6313	B9
6316	C10
6317	A8
6318	A9
6319	A9
6325	A9
7301	B8
7304	B8
7305	C8
7307	B10
7312	A8
7313	C10
7314	C10
7315	C9
9001	B9
9002	C9
9003	B9
9004	C8
9005	B8
9006	B8
9007	B8
9008	A9
9009	A9
9010	A8
9011	A7
9012	A8
9013	B8
9014	B8
9015	C7
9016	C6
9017	A7
9018	A6
9019	A6
9020	A6
9021	A5
9022	B6
9023	C5
9024	B5
9025	A4
9026	A2
9027	B3
9028	C3
9029	C3
9030	A2
9031	A1
9032	A1
9034	B2
9035	C1
9036	C3
9037	B4
9038	B2
9039	A3
9040	C3
9041	C8
9301	A9
9304	A9
9305	A9
9420	C8
9421	A8
9422	A8
9423	C6
9424	A7
9425	B10
9426	A7
9427	A6
9428	A7
9429	A5
9430	A7
9431	B6
9432	C4
9433	A5
9434	A5
9435	C4
9436	B5
9437	B5
9438	B5
9439	B4
9440	A8
9441	A6
9442	A4
9443	B3
9444	B3
9445	C3
9446	C6
9447	A2
9448	A1
9449	C3
9450	A2
9451	C6
9452	A3
9453	A4
9454	C2
9455	A3
9456	C2
9457	A3
9459	B3
9460	B5
9461	B3
9462	C4
9463	B4
9464	C1
9465	B2
9466	B3
9467	A4
9468	A3
9469	A2
9470	A3
9471	B3
9472	B2
9473	B3
9474	A3
9475	B4
9476	A3
9477	B3
9478	B3
9479	B3
9480	A3
9481	A2
9482	A3
9483	A4
9484	A1
9485	B6
9486	A4
9487	C3
9488	A1
9489	C3
9490	B1
9491	A2
9492	A2
9494	A3
9495	A3
9496	A3
9497	B1
9498	C1
9499	B3
9551	A6
9701	B8



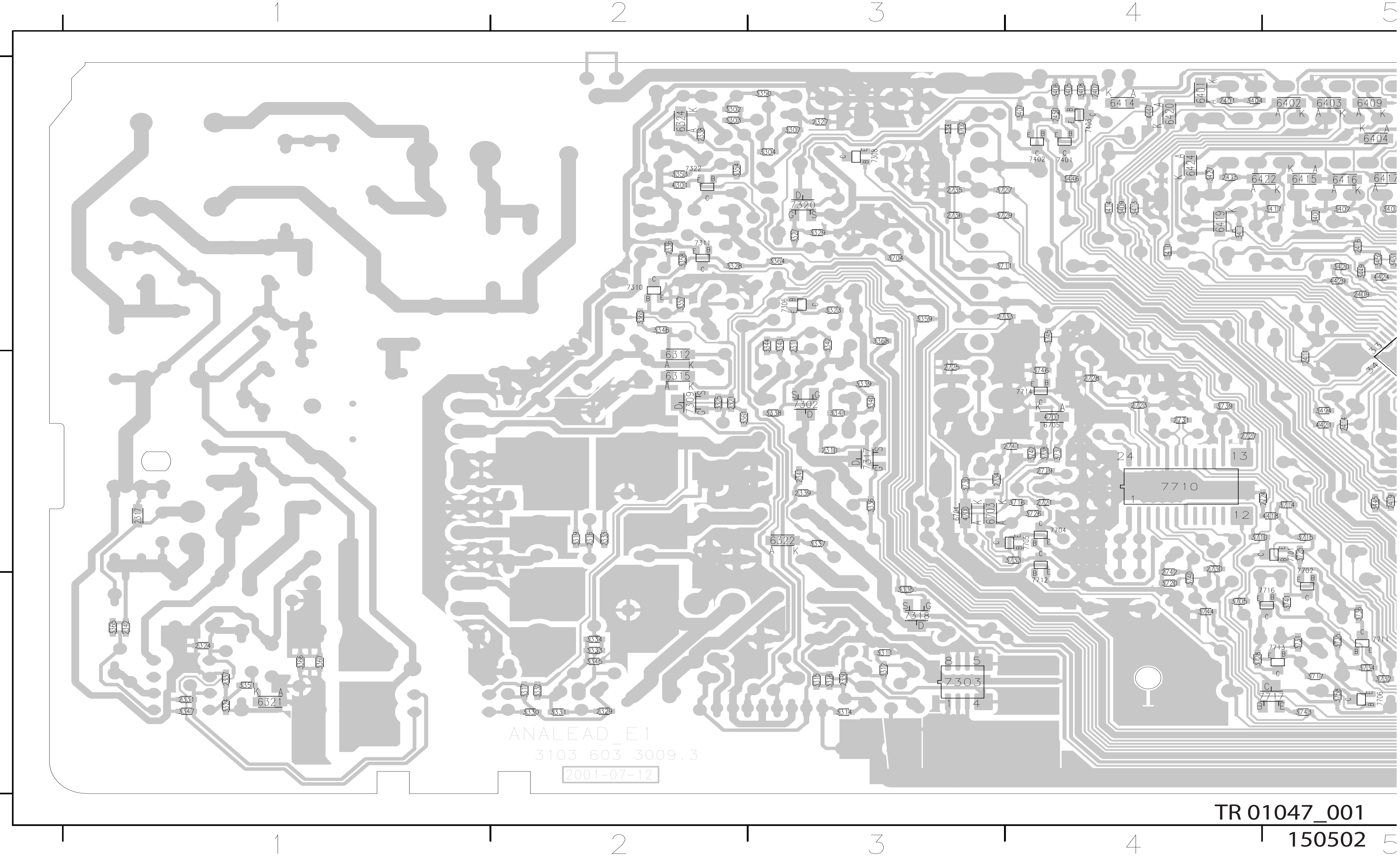
Layout Analog Board (Overview Bottom View)

2002	B10
2003	B10
2006	B10
2008	B10
2009	B10
2012	B10
2014	B9
2015	B9
2016	B9
2018	B10
2019	B10
2022	B10
2024	B9
2025	B10
2026	B10
2032	A9
2033	B10
2034	B10
2035	B10
2036	B10
2037	B10
2038	B10
2039	B10
2040	B10
2310	B3
2311	A3
2316	B2
2317	B1
2321	B2
2324	C1
2327	A3
2329	C2
2330	C3
2331	C1
2333	B2
2334	B8
2336	A2
2337	C1
2338	A2
2339	B3
2341	B3
2342	C1
2401	A4
2402	A4
2404	C6
2406	A9
2407	A9
2408	B5
2409	A5
2410	A6
2411	B5
2412	A9
2414	B5
2415	A4
2416	A5
2418	A5
2419	B5
2420	A6
2422	A5
2423	A6
2425	A7
2427	A6
2430	A5
2433	B5
2435	B6
2436	B6
2437	B6
2438	B6
2439	B6
2440	B6
2441	B6
2444	A6
2445	A7
2446	C5
2447	A7
2448	A7
2449	C6
2450	A4
2459	B6
2501	A5
2502	B8
2503	A9
2504	A6
2505	A6
2506	A6
2507	C6
2508	C6
2509	A8
2512	B8
2513	A7
2514	A8
2515	A8
2517	A6
2518	A8
2520	A5
2521	B9
2523	A6
2524	B8
2525	B7
2527	A6
2530	B9
2531	B9
2532	B9
2535	A8
2536	A7
2580	A9
2585	A9
2586	A9
2587	A10
2590	A9
2601	B6
2603	B6
2604	B7
2606	B7
2607	B7
2609	C7
2610	B6
2616	B6
2617	B6
2618	B6
2619	B7
2620	B7
2621	B7
2623	B7
2719	B4
2721	B4
2723	B4
2724	B5
2725	B3
2727	B4
2728	B4
2730	B4
2731	B4
2733	A3
2734	B3
2735	A3
2736	A3
2741	B4
2742	B4
2932	A10
2934	A10
2935	A10
2936	A10
2937	A10
2938	A10
2940	B9
2942	B9
2943	B9
2944	B9
2945	B9
2946	B9
2947	C8
3001	B10
3002	B10
3003	B10
3004	B10
3005	B10
3006	B10
3007	B10
3008	A9
3009	B10
3010	B10
3011	B10
3012	B10
3013	B10
3014	B10
3015	B9
3017	B9
3018	B9
3019	C10
3020	C10
3024	B10
3026	B9
3027	B10
3029	B10
3030	B10
3034	B9
3043	C10
3044	C10
3045	C10
3046	C10
3047	C10
3048	C10
3049	A9
3050	A9
3051	A8
3052	B10
3053	B10
3054	B10
3302	A2
3303	A2
3304	A3
3307	A3
3311	C3
3312	C3
3314	C3
3315	C3
3316	C3
3317	C2
3319	B2
3323	A3
3324	C1
3325	B2
3327	A3
3328	A2
3329	A3
3330	C2
3331	C2
3332	C2
3333	C2
3334	C2
3335	C3
3336	B3
3337	B3
3338	B3
3339	B3
3340	B3
3341	B3
3342	A3
3343	A3
3344	A3
3345	C2
3346	A2
3347	C1
3348	A8
3349	A8
3350	A3
3351	C1
3353	A2
3354	A2
3355	B8
3357	A2
3358	A2
3359	A3
3361	B2
3362	B8
3363	A2
3364	A3
3365	C1
3366	C1
3367	C1
3368	A3
3371	A8
3372	B8
3373	B7
3400	A9
3401	A5
3402	A5
3403	A5
3404	A4
3405	A4
3406	A4
3407	A4
3408	A4
3409	A4
3410	A4
3411	A4
3413	A4
3414	A4
3415	A9
3416	A9
3417	A5
3418	A9
3419	A8
3420	A5
3421	A6
3423	A6
3424	B6
3425	A5
3426	B6
3427	A4
3428	B6
3429	C6
3431	A5
3437	B5
3438	B5
3439	B5
3440	A8
3442	B6
3443	A7
3444	A7
3445	B5
3446	A4
3448	A7
3449	A5
3450	A7
3452	A5
3453	A10
3455	B5
3456	A7
3457	A7
3458	A9
3459	B6
3460	A9
3461	A5
3462	A5
3463	A5
3464	A5
3465	A5
3466	A5
3467	A5
3468	A5
3469	A5
3470	A5
3471	A5
3472	A5
3473	A7
3474	A7
3475	A6
3476	A5
3477	A5
3478	A6
3481	B5
3482	C6
3483	B5
3484	B5
3485	A6
3486	A7
3487	A6
3488	A6
3489	C6
3490	A6
3491	A6
3492	A6
3493	A6
3494	B5
3495	A7
3496	A7
3501	B9
3503	A7
3504	A7
3505	C6
3506	C6
3507	A8
3508	A7
3510	B8
3511	A7
3512	B9
3513	A8
3514	A9
3516	A9
3518	A7
3520	A7
3521	A7
3522	A7
3524	A7
3525	A7
3526	A8
3527	A7
3528	A6
3529	A7
3530	A7
3531	A7
3534	A9
3535	A8
3536	A8
3537	A8
3538	A7
3580	A9
3581	A9
3582	A10
3584	A10
3585	A9
3600	B7
3602	B7
3606	C6
3607	B6
3611	B7
3612	B6
3702	A3
3704	A3
3705	C4
3710	B4
3711	A3
3714	B5
3715	B5
3716	B4
3717	C5
3720	C4
3725	B5
3726	B4
3727	A3
3728	C4
3729	A3
3730	B3
3731	C5
3732	C5
3733	B4
3734	C5
3735	C5
3736	C5
3737	B4
3738	B4
3739	B4
3740	C4
3741	C5
3742	B4
3743	C5
3744	C4
3745	A4
3746	B4
3758	C5
3931	A10
3932	A10
3933	A10
3934	A10
3935	A10
3936	A10
3937	B8
3938	B8
3939	B9
3940	B9
3941	B9
3942	B9
3943	B9
3944	B9
3945	B9
3946	B9
3947	B9
3948	C9
3950	C9
3951	C9
3952	C9
3953	C9
3954	B9
3955	A8
4003	B9
4004	B9
4006	C9
4301	A2
4401	A5
4402	A9
4411	B5
4412	B6
4413	B6
4414	B6
4415	A6
4416	B9
4417	B6
4418	B5
4419	A6
4420	C5
4421	B5
4422	A6
4423	A6
4424	A5
4425	A6
4426	A6
4427	A10
4428	A9
4429	A5
4430	A9
4431	A8
4433	B6
4434	B6
4435	A8
4437	B8
4442	A9
4443	A8
4444	A9
4445	A9
4446	A8
4447	A4
4448	A6
4449	A6
4601	B7
4700	B3
4701	B4
4999	C9
5001	C9
5704	A3
5932	A10
6001	A9
6002	C10
6003	C9
6312	B2
6314	B8
6315	B2
6320	B8
6321	C1
6322	B3
6324	A2
6401	A4
6402	A5
6403	A5
6404	A5
6409	A5
6414	A4
6415	A5
6416	A5
6417	A5
6418	A5
6419	A4
6420	A4
6422	A5
6423	A6
6424	A4
6425	A6
6426	A6
6427	A6
6428	A6
6429	A6
6580	A9
6600	B7
6703	B3
6704	B3
6705	B4
7001	B10
7002	B10
7003	C10
7005	B10
7006	B9
7008	B10
7009	C10
7010	C10
7011	A9
7302	B3
7303	C3
7306	A3
7308	A3
7309	B2
7310	A2
7311	A2
7317	B3
7318	C3
7319	B7
7320	A3
7321	B8
7322	A2
7401	A4
7402	A4
7403	A4
7404	A9
7405	A6
7406	A5
7407	B6
7408	B5
7409	B6
7410	A7
7411	B6
7412	A8
7415	A7
7416	A6
7419	A9
7420	A9
7421	A9
7501	B8
7502	A8
7503	A8
7504	A7
7505	B9
7506	A7
7508	A7
7509	A6
7511	A7
7580	A9
7600	B7
7701	B5
7702	B5
7704	B4
7705	B4
7706	C5
7710	B4
7711	C5
7712	C4
7713	C5
7714	B4
7716	C5
7717	C5
7931	A10
7932	C8
7933	B9
7934	B9

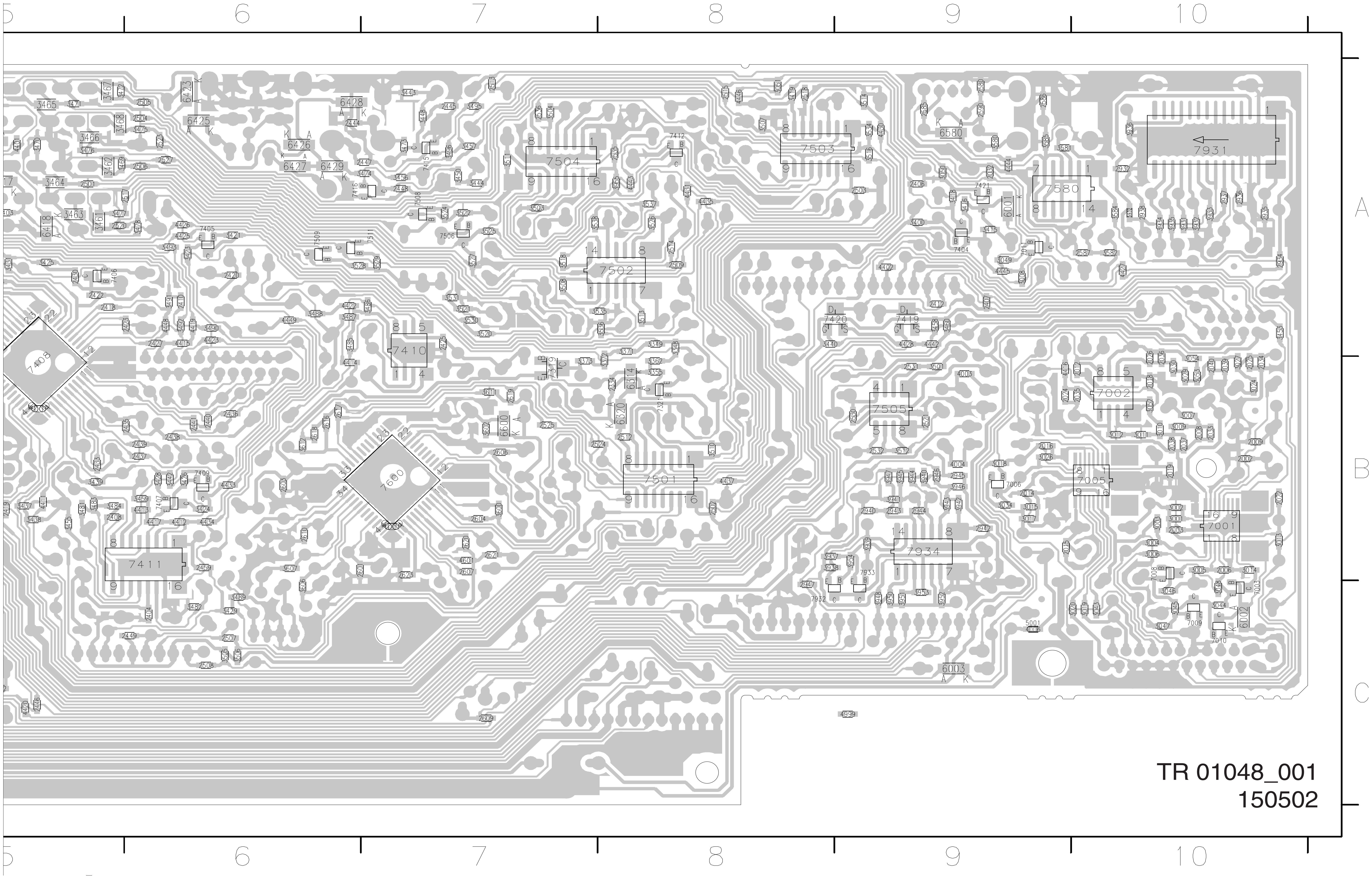


TR 01046_001
150502

Layout Analog Board (Part 1 Bottom View)

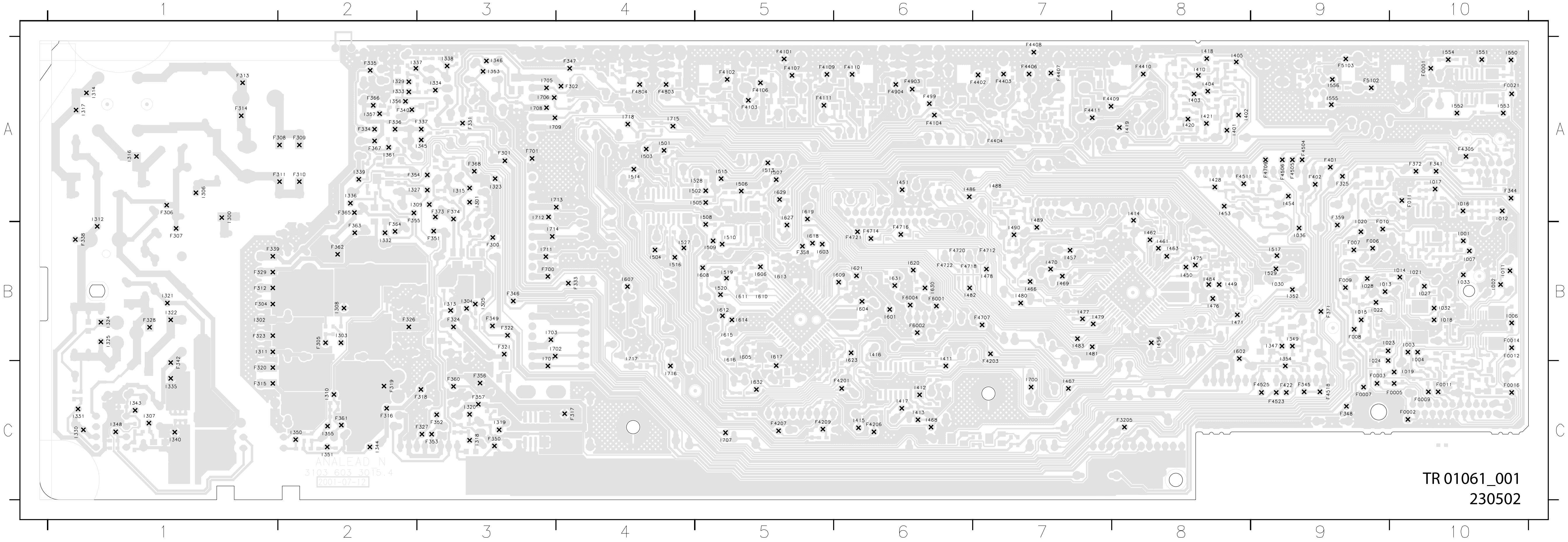

1
2
3
4
5
A
B
C
7710
24
13
12
7303
6322
6312
6315
6321
6324
6401
6402
6403
6409
6404
6414
6420
6422
6415
6416
6424
6419
6703
7320
7302
7317
7318
7309
ANALEAD_E1
3103 603 3009.3
2001-07-12
TR 01047_001
150502

Layout Analog Board (Part 2 Bottom View)


5
6
7
8
9
10
A
B
C
7504
7503
7931
7580
7502
7408
7410
7420
7419
7002
7505
7600
7501
7005
7001
7934
7411
6428
6425
6426
6427
6429
6580
6001
6600
6314
6320
6002
6003
6418
3465
3467
3468
3466
3462
3464
3463
3461
TR 01048_001
150502

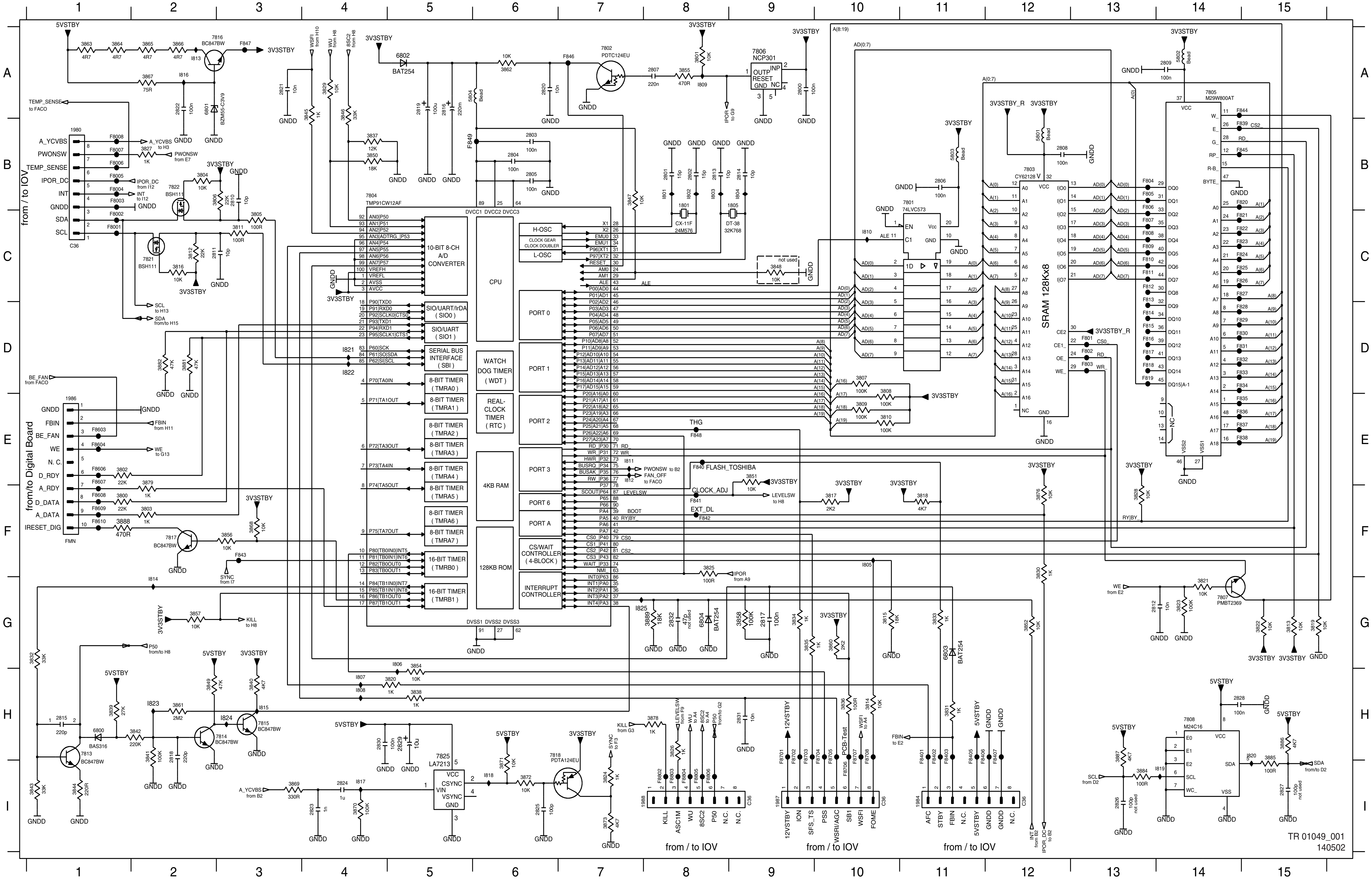
Test points overview Analog Board

F0001	A10
F0002	C10
F0003	C9
F0005	C10
F0007	C9
F0009	C10
F0011	C10
F0012	C10
F0014	B10
F0016	C10
F0021	A10
F006	B9
F007	B9
F008	B9
F009	B9
F010	B9
F011	A10
F300	B3
F301	A3
F302	A4
F304	B1
F305	B2
F306	A1
F307	B1
F308	A2
F309	A2
F310	A2
F311	A2
F312	B1
F313	A1
F314	A1
F315	C1
F316	C2
F317	C4
F318	C3
F319	C2
F320	C1
F3205	C8
F321	B3
F322	B3
F323	B1
F324	B3
F325	A9
F326	B2
F327	C3
F328	B1
F329	B1
F331	A3
F333	B4
F334	A2
F335	A2
F336	A2
F337	A3
F338	B1
F339	B1
F340	A2
F341	A10
F342	C1
F344	A10
F345	C9
F346	B3
F347	A4
F348	C9
F349	B3
F350	C3
F351	B3
F352	C3
F353	C3
F354	A3
F355	A2
F356	C3
F357	C3
F358	B5
F359	B9
F360	C3
F361	C2
F362	B2
F363	B2
F364	B2
F365	A2
F366	A2
F367	A2
F368	A3
F371	B9
F372	A10
F373	A3
F374	A3
F401	A9
F402	A9
F4101	A5
F4102	A5
F4103	A5
F4104	A6
F4106	A5
F4107	A5
F4109	A5
F4110	A6
F4111	A5
F4201	C6
F4203	B7
F4206	C6
F4207	C5
F4209	C5
F422	C9
F4305	A10
F4402	A7
F4403	A7
F4404	A7
F4406	A7
F4407	A7
F4408	A7
F4409	A7
F4410	A8
F4411	A7
F4504	A9
F4505	A9
F4506	A9
F4511	A8
F4518	C9
F4523	C9
F4525	C9
F4707	B7
F4709	A9
F4712	B7
F4714	B6
F4716	B6
F4718	B6
F4720	B6
F4721	B6
F4722	B6
F4803	A4
F4804	A4
F4903	A6
F4904	A6
F499	A6
F5102	A9
F5103	A9
F6001	B6
F6002	B6
F6004	B6
F700	B3
F701	A3
I001	B10
I002	B10
I003	B10
I004	B10
I006	B10
I007	B10
I011	B10
I012	A10
I013	B9
I014	B10
I015	B9
I016	A10
I017	A10
I018	B10
I019	C10
I020	B9
I021	B10
I022	B9
I023	B9
I024	B9
I027	B10
I028	B9
I030	B9
I032	B10
I033	B10
I036	B9
I300	A1
I301	A3
I303	B2
I304	B3
I305	B3
I306	A1
I307	C1
I308	B2
I309	A3
I310	C2
I311	B1
I312	B1
I313	B3
I314	A1
I315	A3
I316	A1
I317	A1
I318	C3
I319	C3
I320	C3
I321	B1
I322	B1
I323	A3
I324	B1
I325	B1
I327	A3
I329	A2
I330	C1
I331	C1
I332	B2
I333	A2
I334	A3
I335	C1
I336	A2
I337	A2
I338	A3
I339	A2
I340	C1
I343	C1
I344	C2
I345	A3
I346	A3
I347	B9
I348	C1
I349	B9
I350	C2
I351	C2
I352	B9
I353	A3
I354	C9
I355	C2
I356	A2
I357	A2
I361	A2
I401	A8
I402	A8
I403	A8
I404	A8
I405	A8
I410	A8
I411	C6
I412	C6
I413	C6
I414	A8
I415	C6
I416	B6
I417	C6
I418	A8
I419	A8
I420	A8
I421	A8
I428	A8
I449	B8
I450	B8
I451	A6
I453	A8
I454	A9
I456	B8
I457	B7
I461	B8
I462	B8
I463	B8
I466	B7
I467	C7
I468	C6
I469	B7
I470	B7
I471	B8
I475	B8
I476	B8
I477	B7
I478	B7
I479	B7
I480	B7
I481	B7
I482	B6
I483	B7
I484	B8
I486	A6
I488	A7
I489	B7
I490	B7
I501	A4
I502	A5
I503	A4
I504	B4
I505	A5
I506	A5
I507	A5
I508	B5
I509	B5
I510	B5
I513	A5
I514	A4
I515	A5
I516	B4
I517	B9
I519	B5
I520	B5
I527	B4
I528	A5
I529	B9
I550	A10
I551	A10
I552	A10
I553	A10
I554	A10
I555	A9
I556	A9
I601	B6
I602	B8
I603	B5
I604	B6
I605	B5
I606	B5
I607	B4
I608	B5
I609	B6
I610	B5
I611	B5
I612	B5
I613	B5
I614	B5
I615	B5
I616	B5
I617	C5
I618	B5
I619	A5
I620	B6
I621	B6
I623	B6
I627	B5
I629	A5
I630	B6
I631	B6
I632	C5
I700	C7
I701	C3
I702	B3
I703	B3
I705	A3
I706	A3
I707	C5
I708	A3
I709	A3
I711	B3
I712	A3
I713	A4
I714	B3
I715	A4
I716	C4
I717	C4
I718	A4



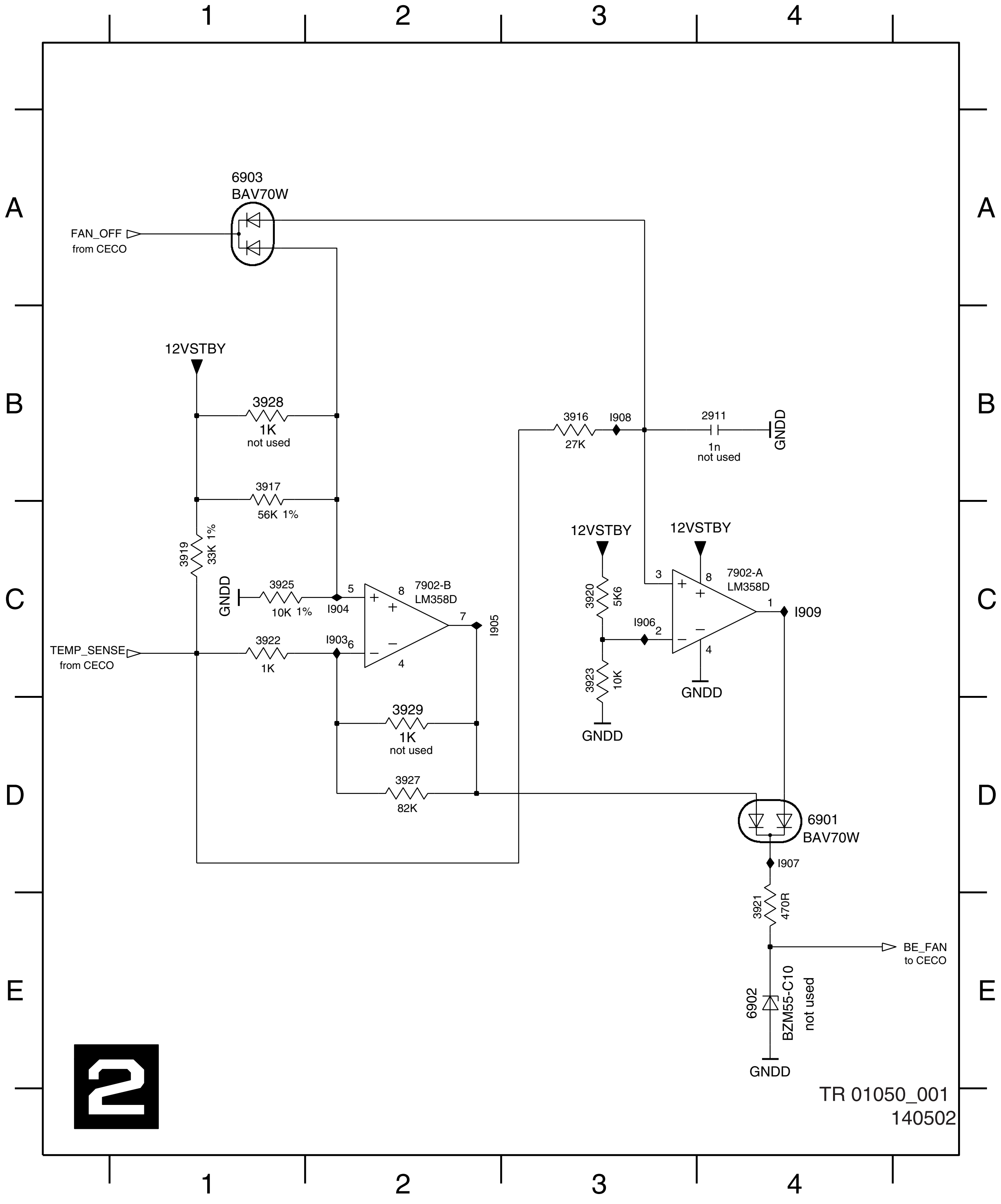
UPC12 Sub PCB: Central Controller (CECO)

1801	B8
1805	B9
1980	B1
1984	I11
1986	E1
1987	I9
1988	I8
2800	A9
2801	B8
2802	B8
2803	B6
2804	B6
2805	B6
2806	B11
2807	A8
2808	B12
2809	A14
2810	B3
2811	C2
2812	G13
2813	B8
2814	B9
2815	H1
2816	A5
2817	G9
2818	H2
2819	A5
2820	A6
2821	A3
2822	A2
2823	I4
2824	I4
2825	I6
2826	I13
2827	I15
2828	H15
2829	H5
2830	H4
2831	H9
2832	G8
3800	F1
3801	A8
3802	E1
3803	F2
3804	B2
3805	C3
3806	B2
3807	D10
3808	D10
3809	E10
3810	E10
3811	C3
3812	C2
3813	G15
3814	H10
3815	G10
3816	C2
3817	F10
3818	F11
3819	G15
3820	H5
3821	F14
3822	G15
3823	G14
3824	I7
3825	F8
3826	H8
3827	B2
3828	F13
3829	A4
3830	F12
3831	H11
3832	G1
3833	G11
3834	G9
3835	G9
3836	H10
3837	B4
3838	H5
3839	H1
3840	H3
3841	H2
3842	H2
3843	I1
3844	I1
3845	A4
3846	A4
3847	B7
3848	C9
3849	H2
3850	B4
3851	E9
3852	G12
3854	G5
3855	A8
3856	F3
3857	G2
3858	G9
3860	G10
3861	H2
3862	A6
3863	A1
3864	A1
3865	A2
3866	A2
3867	A2
3868	F3
3869	I3
3870	I4
3871	I6
3872	I6
3873	I7
3876	F12
3878	H8
3879	E2
3881	D2
3882	D2
3884	H14
3885	H15
3886	H15
3887	H13
3888	F1
3889	G8
5801	B12
5802	A14
5803	B11
5804	A5
6800	H1
6801	A2
6802	A5
6803	G11
6804	G8
7801	B11
7802	A7
7803	B12
7804	B4
7805	A14
7806	A9
7807	G14
7808	H14
7813	H1
7814	H2
7815	H3
7816	A3
7817	F2
7818	H6
7821	C2
7822	B2
7825	H5
F8001	C1
F8002	C1
F8003	B1
F8004	B1
F8005	B1
F8006	B1
F8007	B1
F8008	B1
F801	D13
F802	D13
F803	D13
F804	B13
F805	B13
F806	B13
F807	C13
F808	C13
F809	C13
F810	C13
F811	C13
F812	C13
F813	C13
F814	D13
F815	D13
F816	D13
F817	D13
F818	D13
F819	D13
F820	B15
F821	C15
F822	C15
F823	C15
F824	C15
F825	C15
F826	C15
F827	C15
F828	D15
F829	D15
F830	D15
F831	D15
F832	D15
F833	D15
F834	D15
F835	E15
F836	E15
F837	E15
F838	E15
F839	B15
F840	E8
F8401	H11
F8402	H11
F8403	H11
F8405	H11
F8406	H11
F8407	H12
F841	F8
F842	F8
F843	F3
F844	A15
F845	B15
F846	A7
F847	A3
F848	E8
F849	B5
F8603	E1
F8604	E1
F8606	E1
F8607	E1
F8608	F1
F8609	F1
F8610	F1
F8701	H9
F8702	H9
F8703	H9
F8704	H10
F8705	H10
F8706	I10
F8707	H10
F8708	H10
F8802	I8
F8803	I8
F8804	I8
F8805	I8
F8806	I8
I801	B8
I802	B8
I803	B8
I804	B9
I805	F10
I806	G5
I807	H4
I808	H4
I809	A8
I810	C10
I811	E7
I812	E7
I813	A2
I814	G2
I815	H3
I816	A2
I817	I4
I818	I6
I819	H14
I820	H15
I821	D4
I822	D4
I823	H2
I824	H3
I825	G7


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
A B C D E F G H I
5VSTBY
3V3STBY
7816 BC847BW
7802 PDTC124EU
7806 NCP301
7805 M29W800AT
7804 TMP91CW12AF
10-BIT 8-CH A/D CONVERTER
CPU
H-OSC
CLOCK GEAR CLOCK DOUBLER
L-OSC
SIO/UART/IrDA (SIO0)
SIO/UART (SIO1)
SERIAL BUS INTERFACE (SBI)
8-BIT TIMER (TMRA0)
8-BIT TIMER (TMRA1)
8-BIT TIMER (TMRA2)
8-BIT TIMER (TMRA3)
8-BIT TIMER (TMRA4)
8-BIT TIMER (TMRA5)
8-BIT TIMER (TMRA6)
8-BIT TIMER (TMRA7)
16-BIT TIMER (TMRB0)
16-BIT TIMER (TMRB1)
WATCH DOG TIMER (WDT)
REAL-CLOCK TIMER (RTC)
4KB RAM
128KB ROM
PORT 0
PORT 1
PORT 2
PORT 3
PORT 6
PORT A
CS/WAIT CONTROLLER (4-BLOCK)
INTERRUPT CONTROLLER
7801 74LVC573
7803 CY62128V
SRAM 128Kx8
1801 CX-11F 24M576
1805 DT-38 32K768
1980
A_YCVBS
PWONSW
TEMP_SENSE
IPOR_DC
INT
GNDD
SDA
SCL
from / to IOV
1986
BE_FAN
FBIN
WE
N.C.
D_RDY
A_RDY
D_DATA
A_DATA
IRESET_DIG
from/to Digital Board
7822 BSH111
7821 BSH111
7817 BC847BW
7813 BC847BW
7814 BC847BW
7815 BC847BW
7807 PMBT2369
7808 M24C16
7825 LA7213
7818 PDTA124EU
6802 BAT254
6801 BZM55-C3V9
6800 BAS316
6803 BAT254
6804 BAT254
THG
FLASH_TOSHIBA
CLOCK_ADJ
EXT_DL
LEVELSW
PWONSW
FAN_OFF
KILL
SYNC
P50
1988
KILL ASC1M WU 8SC2 P50 N.C. N.C.
from / to IOV
1987
12VSTBY ION SFS_TS PSS WSRI/AGC SB1 WSFI FOME
from / to IOV
1984
AFC STBY FBIN N.C. 5VSTBY GNDD GNDD N.C.
from / to IOV
not used
TR 01049_001
140502

UPC12 Sub PCB: Fan Control (FACO)

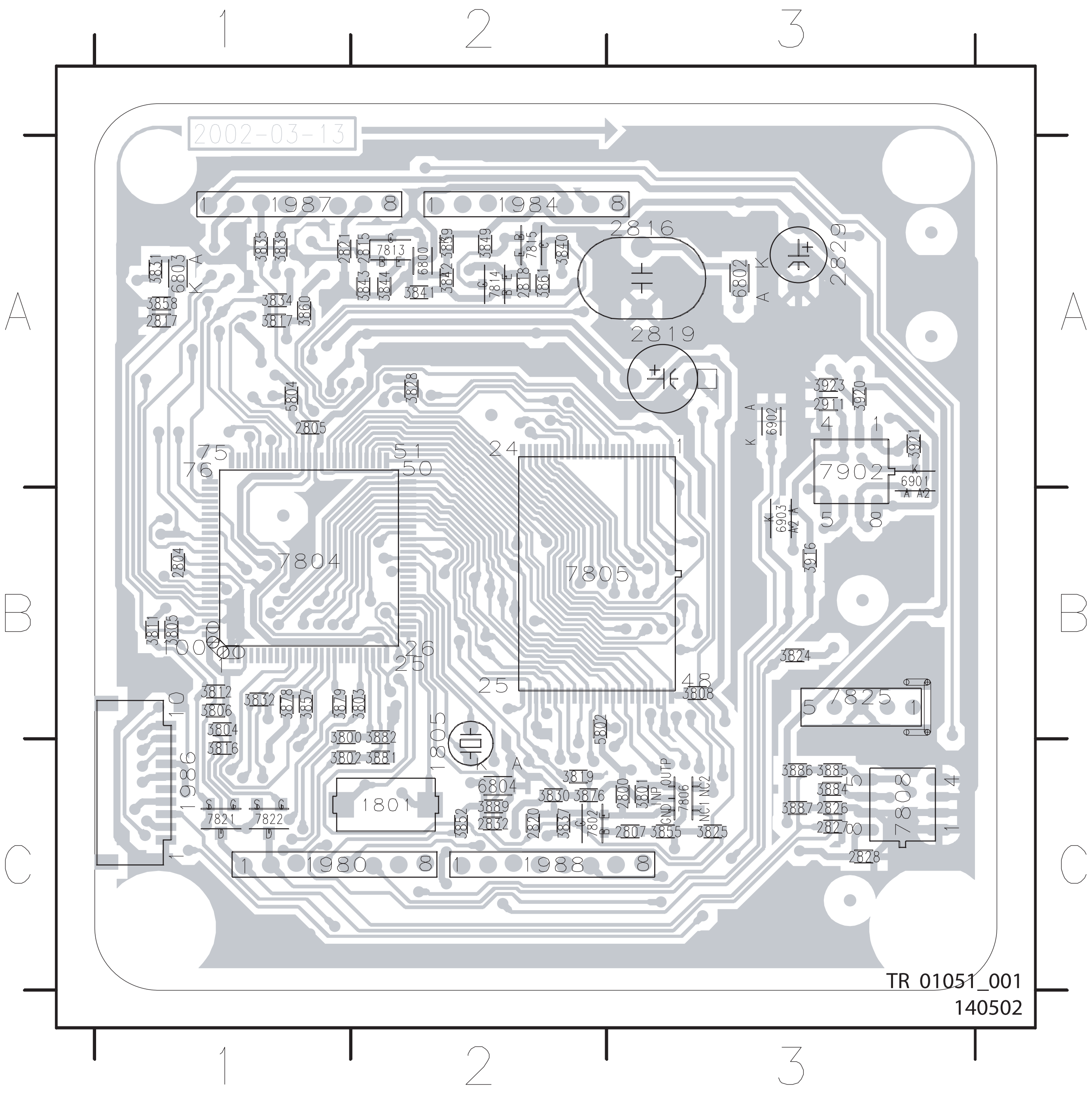
2911 B4	3919 C1	3922 C1	3927 D2	6901 D4	7902-A C4	I904 C2	I907 D4
3916 B3	3920 C3	3923 C3	3928 B1	6902 E4	7902-B C2	I905 C2	I908 B3
3917 B1	3921 E4	3925 C1	3929 D2	6903 A1	I903 C2	I906 C3	I909 C4



1
2
3
4
A
B
C
D
E
6903
BAV70W
FAN_OFF
from CECO
12VSTBY
3928
1K
not used
3917
56K 1%
3919
33K 1%
GNDD
3925
10K 1%
I904
5
8
7902-B
LM358D
7
I905
TEMP_SENSE
from CECO
3922
1K
I903
6
4
3929
1K
not used
3927
82K
3916
27K
I908
2911
1n
not used
GNDD
12VSTBY
3920
5K6
I906
2
3923
10K
GNDD
12VSTBY
3
8
7902-A
LM358D
1
I909
4
GNDD
6901
BAV70W
I907
3921
470R
BE_FAN
to CECO
6902
BZM55-C10
not used
GNDD
2
TR 01050_001
140502

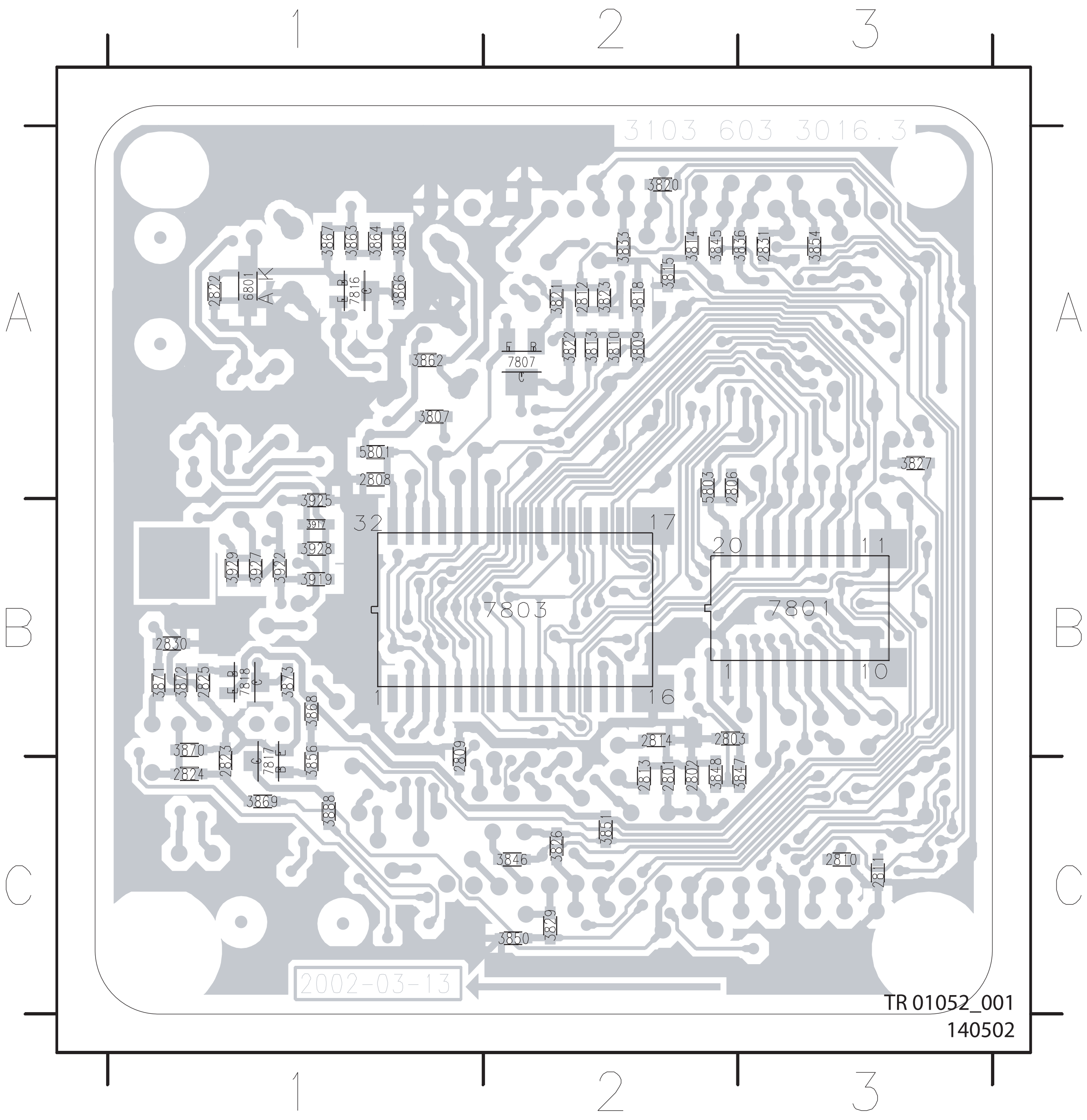
Layout UPC 12 Sub PCB (Top View)

1801	C2	2820	C2	3811	B1	3840	A2	3882	B2	6901	A3
1805	C2	2821	A1	3812	B1	3841	A2	3884	C3	6902	A3
1980	C1	2826	C3	3816	C1	3842	A2	3885	C3	6903	B3
1984	A2	2827	C3	3817	A1	3843	A2	3886	C3	7802	C2
1986	C1	2828	C3	3819	C2	3844	A2	3887	C3	7804	B1
1987	A1	2829	A3	3824	B3	3849	A2	3889	C2	7805	B2
1988	C2	2832	C2	3825	C3	3852	C2	3916	B3	7806	C3
2800	C3	2911	A3	3828	A2	3855	C3	3920	A3	7808	C3
2804	B1	3800	B1	3830	C2	3857	B1	3921	A3	7813	A2
2805	A1	3801	C3	3831	A1	3858	A1	3923	A3	7814	A2
2807	C3	3802	C1	3832	B1	3860	A1	5802	B2	7815	A2
2815	A2	3803	B2	3834	A1	3861	A2	5804	A1	7821	C1
2816	A3	3804	B1	3835	A1	3876	C2	6800	A2	7822	C1
2817	A1	3805	B1	3837	C2	3878	B1	6802	A3	7825	B3
2818	A2	3806	B1	3838	A1	3879	B1	6803	A1	7902	A3
2819	A3	3808	B3	3839	A2	3881	C2	6804	C2		

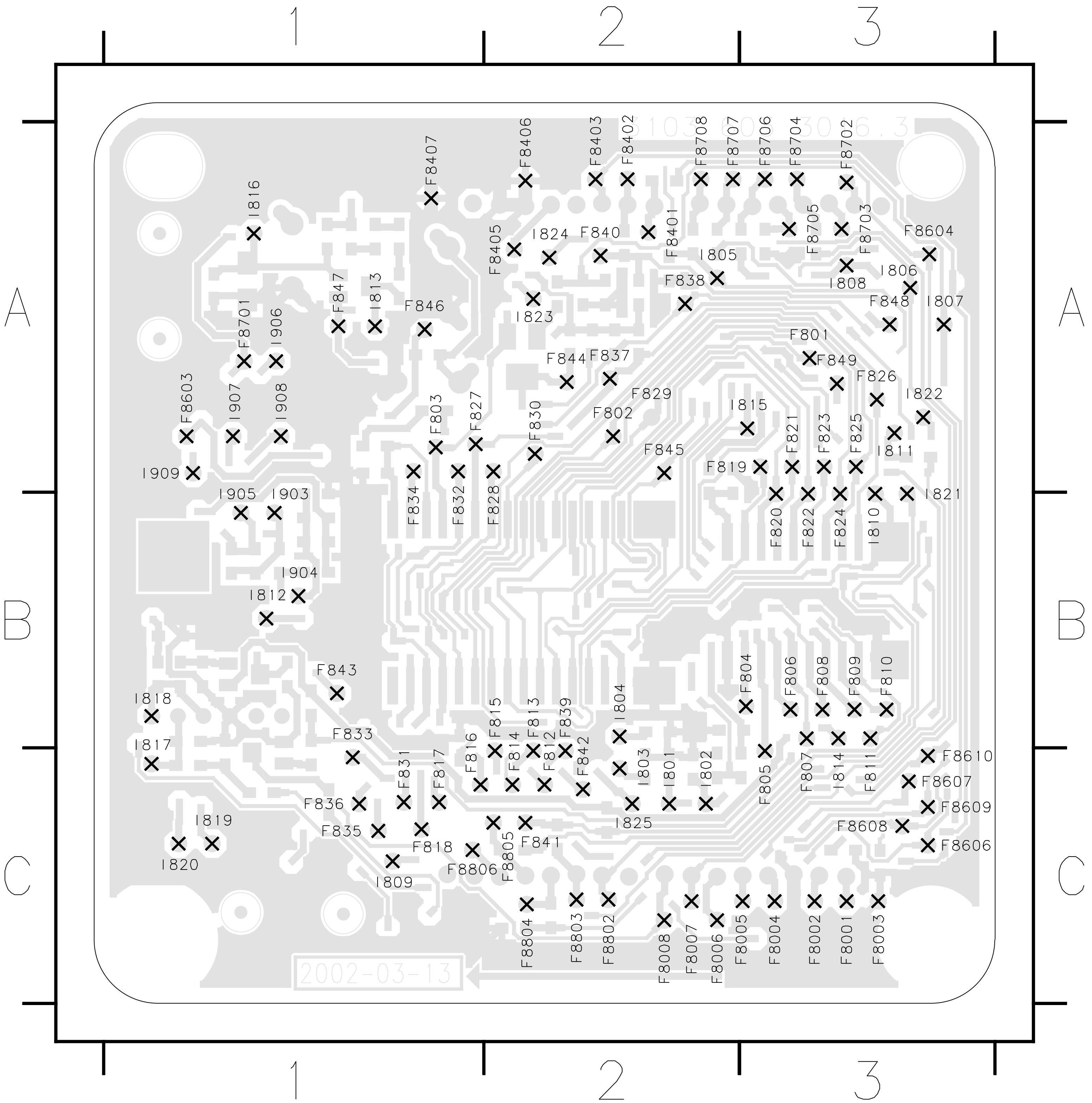


Layout UPC 12 Sub PCB (Bottom View)

2801	C2	2823	C1	3820	A2	3848	C2	3869	C1	3929	B1
2802	C2	2824	C1	3821	A2	3850	C2	3870	B1	5801	A1
2803	B2	2825	B1	3822	A2	3851	C2	3871	B1	5803	A2
2806	A2	2830	B1	3823	A2	3854	A3	3872	B1	6801	A1
2808	A1	2831	A3	3826	C2	3856	C1	3873	B1	7801	B3
2809	B1	3807	A1	3827	A3	3862	A1	3888	C1	7803	B2
2810	C3	3809	A2	3829	C2	3863	A1	3917	B1	7807	A2
2811	C3	3810	A2	3833	A2	3864	A1	3919	B1	7816	A1
2812	A2	3813	A2	3836	A3	3865	A1	3922	B1	7817	C1
2813	C2	3814	A2	3845	A2	3866	A1	3925	B1	7818	B1
2814	B2	3815	A2	3846	C2	3867	A1	3927	B1		
2822	A1	3818	A2	3847	C3	3868	B1	3928	B1		



Tests points overview UPC12 Sub PCB

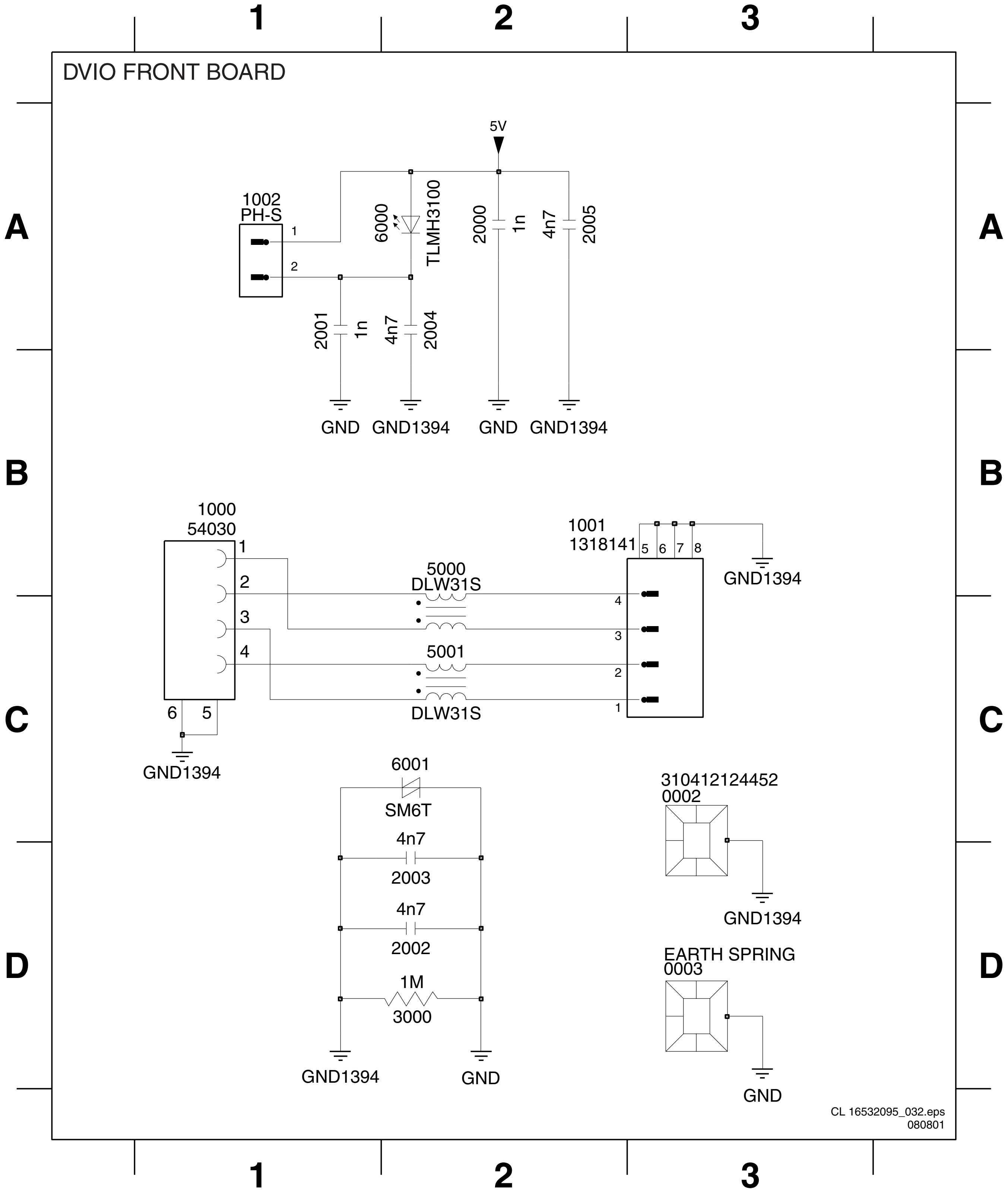


F8001	C3
F8002	C3
F8003	C3
F8004	C3
F8005	C3
F8006	C2
F8008	C2
F8009	C2
F801	A3
F802	A2
F803	A1
F804	B3
F805	C3
F806	B3
F807	B3
F808	B3
F809	B3
F810	B3
F811	B3
F812	C2
F813	C2
F814	C2
F815	C2
F816	C1
F817	C1
F818	C1
F819	A3
F820	B3
F821	A3
F822	B3
F823	A3
F824	B3
F825	A3
F826	A3
F827	A1
F828	A2
F830	A2
F831	C1
F832	A1
F833	C1
F834	A1
F835	C1
F836	C1
F837	A2
F838	A2
F839	C2
F840	A2
F8401	A2
F8402	A2
F8403	A2
F8405	A2
F8406	A2
F8407	A1
F841	C2
F842	C2
F843	B1
F844	A2
F845	A2
F846	A1
F847	A1
F848	A3
F849	A3
F8603	A1
F8604	A3
F8606	C3
F8607	C3
F8608	C3
F8609	C3
F8610	C3
F8701	A1
F8702	A3
F8703	A3
F8704	A3
F8705	A3
F8706	A3
F8707	A2
F8708	A2
F8802	C2
F8803	C2
F8804	C2
F8805	C2
F8806	C1
I801	C2
I802	C2
I803	C2
I804	B2
I805	A2
I806	A3
I807	A3
I808	A3
I809	C1
I810	B3
I811	A3
I812	B1
I813	A1
I814	B3
I815	A3
I816	A1
I817	C1
I818	B1
I819	C1
I820	C1
I821	B3
I822	A3
I823	A2
I824	A2
I825	C2
I903	B1
I904	B1
I905	B1
I906	A1
I907	A1
I908	A1
I909	A1

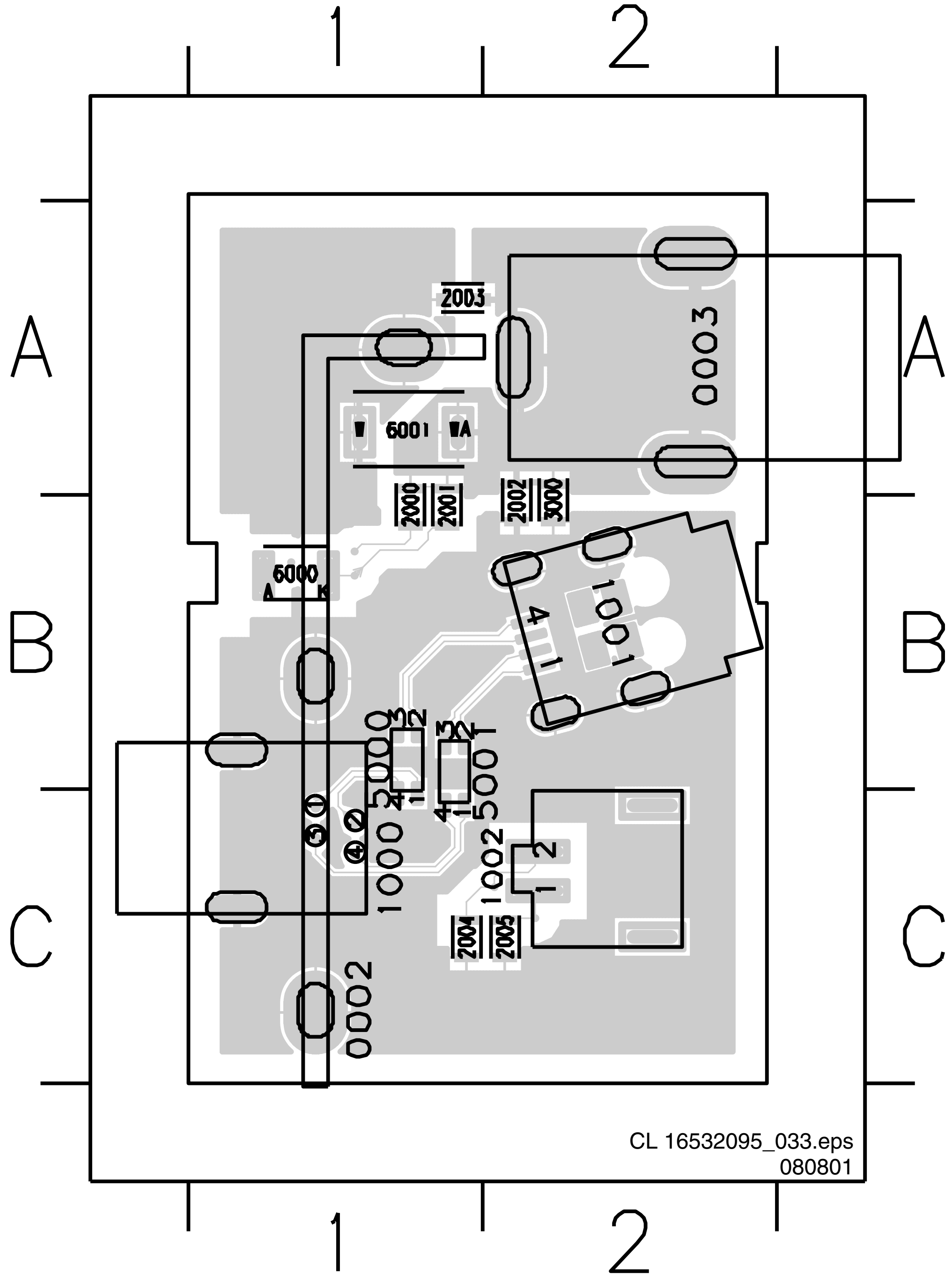
TR 01053_001
140502

DVIO Front Board

0002	**C3**
0003	**D3**
1000	**B1**
1001	**B2**
1002	**A1**
2000	**A2**
2001	**A1**
2002	**D2**
2003	**D2**
3000	**D2**
5000	**B2**
5001	**C2**
6000	**A2**
6001	**C2**

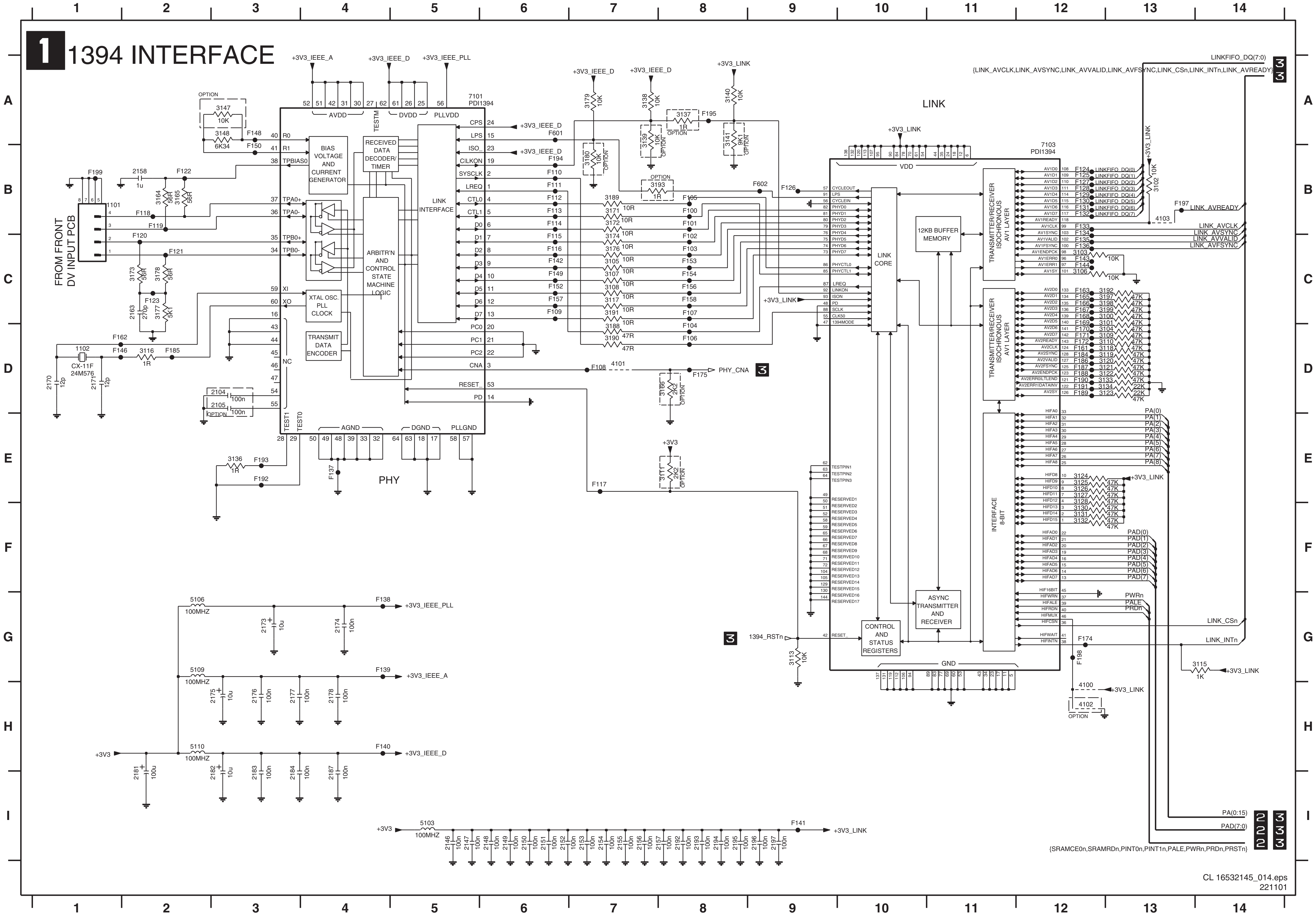

1
2
3
A
B
C
D
DVIO FRONT BOARD
5V
1002
PH-S
1
2
6000
TLMH3100
2000
1n
4n7
2005
2001
1n
4n7
2004
GND
GND1394
GND
GND1394
1000
54030
1
2
3
4
6
5
GND1394
5000
DLW31S
5001
DLW31S
1001
1318141
5
6
7
8
4
3
2
1
GND1394
6001
SM6T
4n7
2003
4n7
2002
1M
3000
GND1394
GND
310412124452
0002
GND1394
EARTH SPRING
0003
GND
CL 16532095_032.eps
080801

Layout DVIO Front Board


1
2
A
B
C
2003
0003
6001
2000
2001
2002
3000
6000
1001
4
1
1000
5000
5001
1002
2004
2005
0002
CL 16532095_033.eps
080801

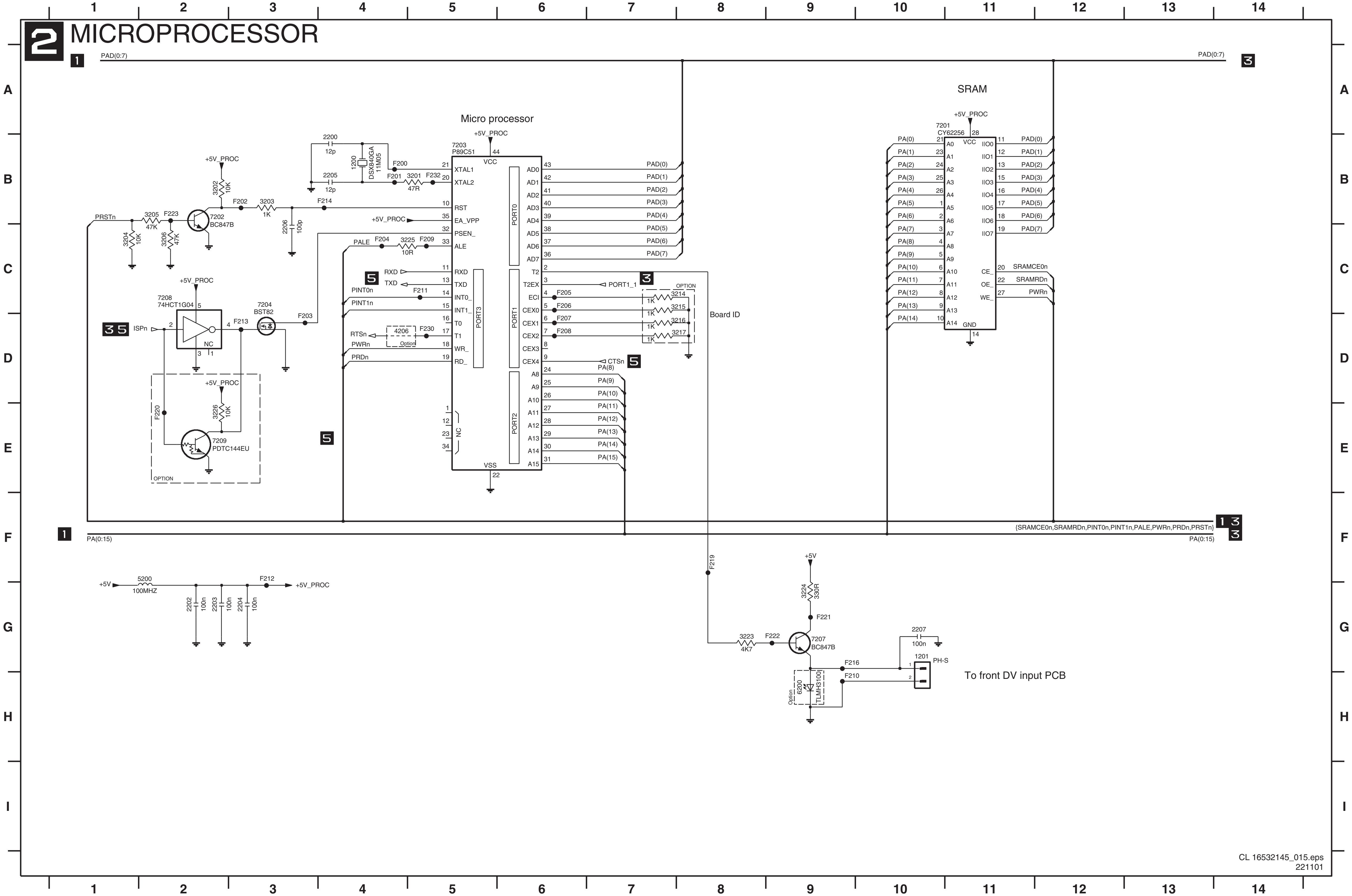
0002	C1
0003	A2
1000	C1
1001	B2
1002	C2
2000	B1
2001	B1
2002	B2
2003	A1
2004	C1
2005	C2
3000	B2
5000	B2
5001	B2
6000	B1
6001	A1

DVIO Board: 1394 Interface


1 1394 INTERFACE
FROM FRONT DV INPUT PCB
7101 PDI1394
BIAS VOLTAGE AND CURRENT GENERATOR
RECEIVED DATA DECODER/ TIMER
LINK INTERFACE
ARBITR'N AND CONTROL STATE MACHINE LOGIC
XTAL OSC. PLL CLOCK
TRANSMIT DATA ENCODER
AVDD
DVDD
PLLVDD
AGND
DGND
PLLGND
PHY
+3V3_IEEE_A
+3V3_IEEE_D
+3V3_IEEE_PLL
+3V3_LINK
+3V3
LINK
7103 PDI1394
VDD
GND
LINK CORE
12KB BUFFER MEMORY
TRANSMITTER/RECEIVER ISOCHRONOUS AV1 LAYER
TRANSMITTER/RECEIVER ISOCHRONOUS AV2 LAYER
INTERFACE 8-BIT
ASYNC TRANSMITTER AND RECEIVER
CONTROL AND STATUS REGISTERS
LINKFIFO_DQ(7:0)
(LINK_AVCLK,LINK_AVSYNC,LINK_AVVALID,LINK_AVFSYNC,LINK_CSn,LINK_INTn,LINK_AVREADY)
LINK_AVREADY
LINK_AVCLK
LINK_AVSYNC
LINK_AVVALID
LINK_AVFSYNC
LINK_CSn
LINK_INTn
PA(0:15)
PAD(7:0)
(SRAMCE0n,SRAMRDn,PINT0n,PINT1n,PALE,PWRn,PRDn,PRSTn)
PHY_CNA
1394_RSTn
OPTION
CX-11F 24M576
100MHZ
CL 16532145_014.eps
221101

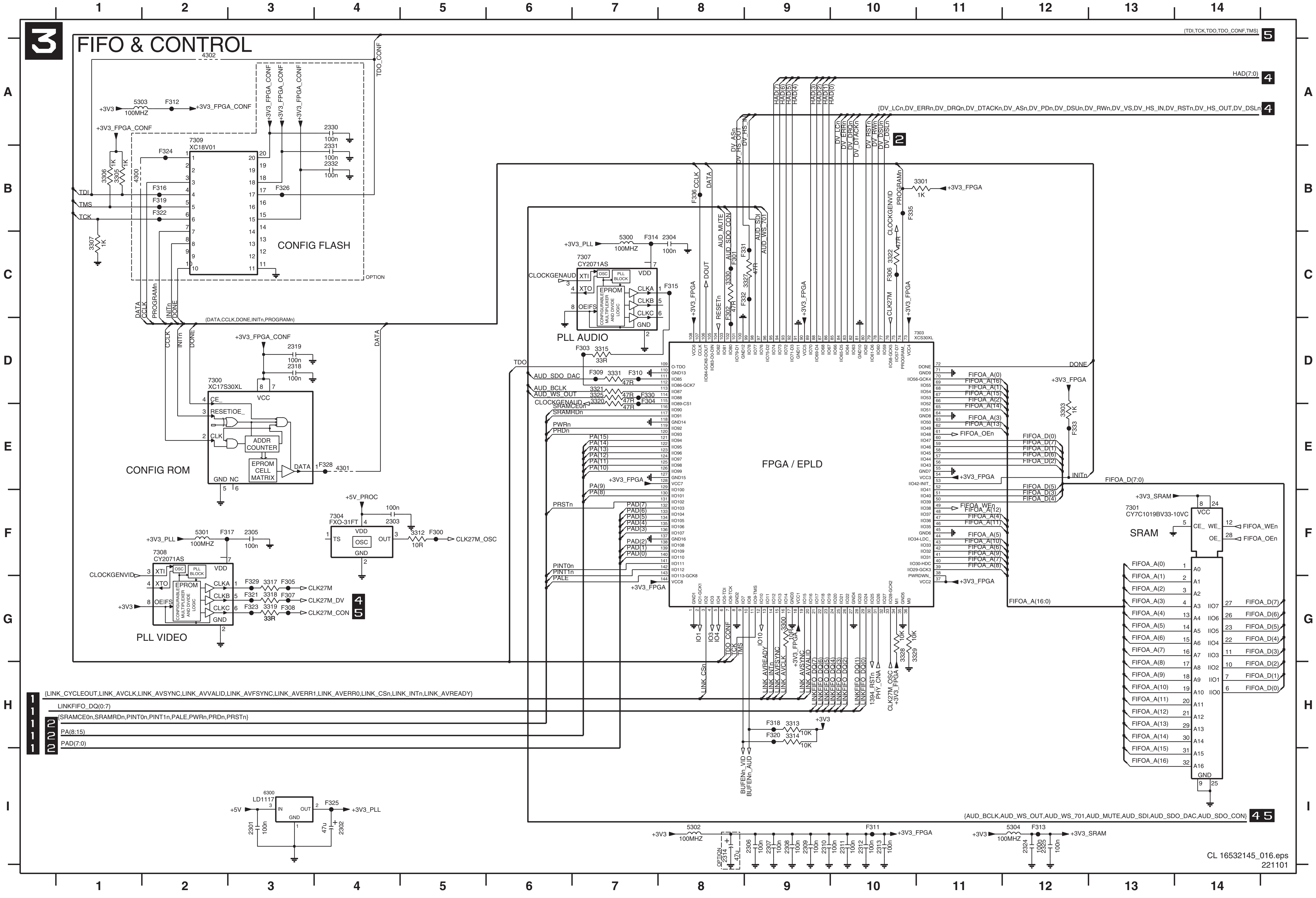
1101	B1	3180	B7	F184	D12
1102	D1	3188	D7	F185	D2
2104	D3	3189	B7	F186	D12
2105	D3	3190	D7	F187	D12
2146	I5	3191	C7	F188	D12
2147	I5	3192	C13	F189	D12
2148	I6	3193	B7	F190	D12
2149	I6	3197	C13	F191	D12
2150	I6	3198	C13	F192	E3
2151	I6	3199	C13	F193	E3
2152	I6	4100	H12	F194	B6
2153	I7	4101	D7	F195	A8
2154	I7	4102	H12	F197	B13
2155	I7	4103	B13	F198	G12
2156	I7	5103	I5	F199	B1
2157	I8	5106	G2	F601	A6
2158	B2	5109	G2	F602	B9
2163	C2	5110	H2		
2170	D1	7101	A5		
2171	D1	7103	B12		
2173	G3	F100	B8		
2174	G4	F101	B8		
2175	H3	F102	C8		
2176	H3	F103	C8		
2177	H3	F104	D8		
2178	H4	F105	B8		
2181	I2	F106	D8		
2182	I3	F107	C8		
2183	I3	F108	D7		
2184	I3	F109	C6		
2187	I4	F110	B6		
2192	I8	F111	B6		
2193	I8	F112	B6		
2194	I8	F113	B6		
2195	I8	F114	B6		
2196	I9	F115	C6		
2197	I9	F116	C6		
3100	C13	F117	E7		
3101	D13	F118	B2		
3102	B13	F119	B2		
3103	C12	F120	C2		
3104	D13	F121	C2		
3105	C7	F122	B2		
3106	C12	F123	C2		
3107	C7	F124	B12		
3108	C7	F125	B12		
3109	D13	F126	B9		
3110	D13	F127	B12		
3111	E8	F128	B12		
3113	G9	F129	B12		
3115	G14	F130	B12		
3116	D2	F131	B12		
3117	C7	F132	B12		
3118	D13	F133	B12		
3119	D13	F134	C12		
3120	D13	F135	C12		
3121	D13	F136	C12		
3122	D13	F137	E4		
3123	D13	F138	G4		
3124	E12	F139	G4		
3125	E12	F140	H4		
3126	E12	F141	I9		
3127	E12	F142	C6		
3128	F12	F143	C12		
3130	F12	F144	C12		
3131	F12	F146	D1		
3132	F12	F148	A3		
3133	D13	F149	C6		
3134	D13	F150	B3		
3136	E3	F152	C6		
3137	A8	F153	C8		
3138	A7	F154	C8		
3139	A7	F156	C8		
3140	A8	F157	C6		
3141	A8	F158	C8		
3147	A3	F161	D12		
3148	A3	F162	D1		
3164	B2	F163	C12		
3165	B2	F165	C12		
3166	D8	F166	C12		
3171	B7	F167	C12		
3172	B7	F168	C12		
3173	C2	F169	D12		
3174	C7	F170	D12		
3176	C7	F171	D12		
3177	C2	F172	D12		
3178	C2	F174	G12		
3179	A7	F175	D8		

DVIO Board: Microprocessor


2 MICROPROCESSOR
1 2 3 4 5 6 7 8 9 10 11 12 13 14
A B C D E F G H I
PAD(0:7)
Micro processor
7203
P89C51
+5V_PROC
VCC
XTAL1
XTAL2
RST
EA_VPP
PSEN_
ALE
RXD
TXD
INT0_
INT1_
T0
T1
WR_
RD_
NC
VSS
PORT0
PORT1
PORT2
PORT3
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7
T2 T2EX ECI CEX0 CEX1 CEX2 CEX3 CEX4
A8 A9 A10 A11 A12 A13 A14 A15
PAD(0) PAD(1) PAD(2) PAD(3) PAD(4) PAD(5) PAD(6) PAD(7)
PA(8) PA(9) PA(10) PA(11) PA(12) PA(13) PA(14) PA(15)
PORT1_1
CTSn
OPTION
3214 3215 3216 3217
1K
Board ID
2200
12p
2205
12p
1200
DSX840GA
11M05
F200 F201
3201
47R
F232
+5V_PROC
3202
10K
F202
3203
1K
F214
2206
100p
PRSTn
3205
47K
F223
3204
10K
3206
47K
7202
BC847B
PALE
F204
3225
10R
F209
RXD
TXD
PINT0n
PINT1n
F211
RTSn
PWRn
PRDn
4206
Option
F230
7208
74HCT1G04
ISPn
F213
NC
7204
BST82
F203
F220
3226
10K
7209
PDTC144EU
OPTION
SRAM
7201
CY62256
VCC
GND
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14
IIO0 IIO1 IIO2 IIO3 IIO4 IIO5 IIO6 IIO7
CE_ OE_ WE_
PA(0) PA(1) PA(2) PA(3) PA(4) PA(5) PA(6) PA(7) PA(8) PA(9) PA(10) PA(11) PA(12) PA(13) PA(14)
SRAMCE0n
SRAMRDn
PWRn
{SRAMCE0n,SRAMRDn,PINT0n,PINT1n,PALE,PWRn,PRDn,PRSTn}
PA(0:15)
+5V
5200
100MHZ
F212
+5V_PROC
2202 100n
2203 100n
2204 100n
F219
+5V
3224
330R
F221
3223
4K7
F222
7207
BC847B
2207
100n
1201
PH-S
F216
F210
6200
TLMH3100
Option
To front DV input PCB
CL 16532145_015.eps
221101

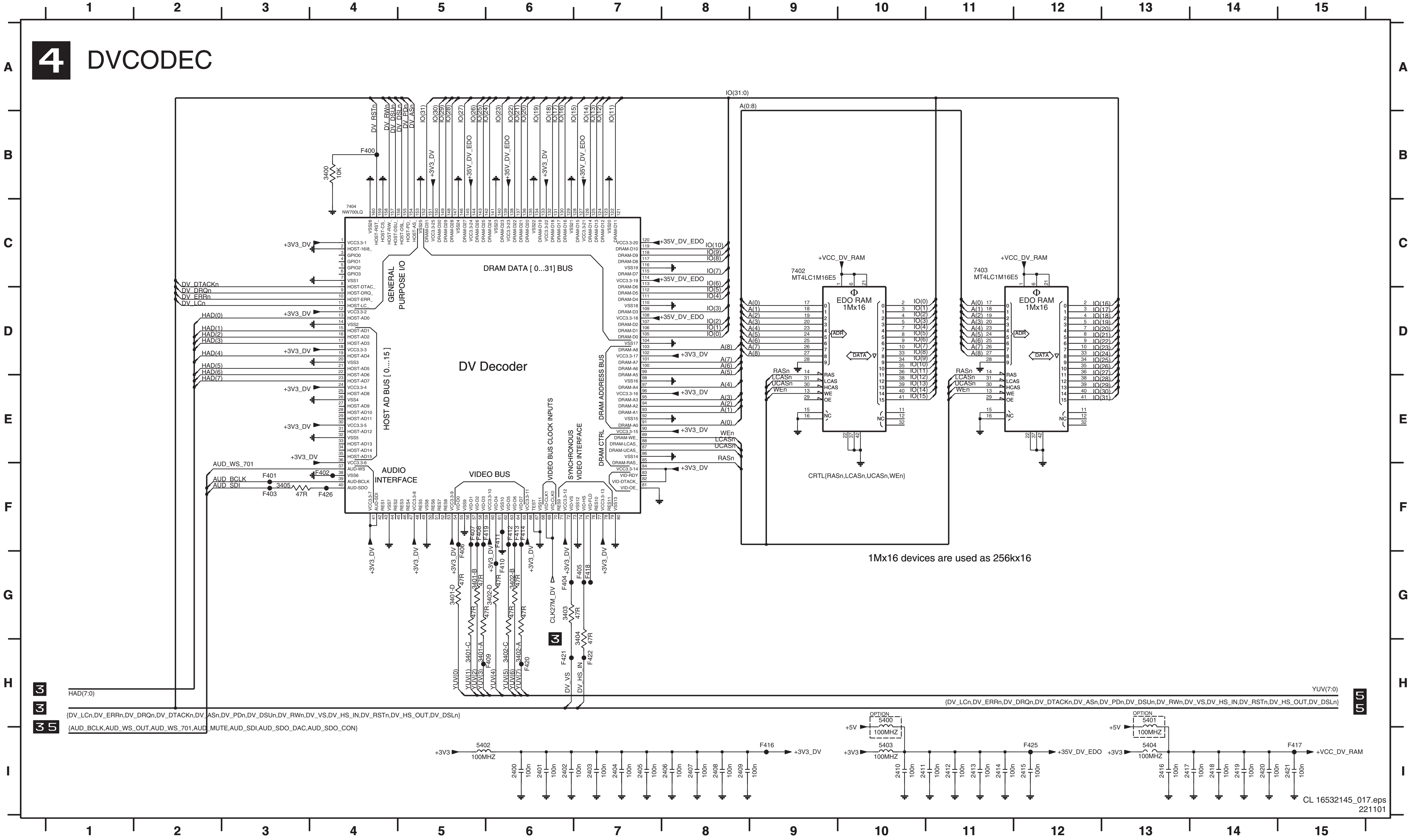
1200	B4
1201	G10
2200	B4
2202	G2
2203	G2
2204	G3
2205	B4
2206	C3
2207	G10
3201	B5
3202	B2
3203	B3
3204	C1
3205	B2
3206	C2
3214	C8
3215	C8
3216	D8
3217	D8
3223	G8
3224	G9
3225	C4
3226	E2
4206	D4
5200	F2
6200	H9
7201	A10
7202	B2
7203	B5
7204	C3
7207	G9
7208	C2
7209	E2
F200	B4
F201	B4
F202	B3
F203	D3
F204	C4
F205	C6
F206	C6
F207	D6
F208	D6
F209	C5
F210	G9
F211	C5
F212	F3
F213	D3
F214	B4
F216	G9
F219	F8
F220	E2
F221	G9
F222	G9
F223	B2
F230	D5
F232	B5

DVIO Board: Fifo & Control


3
FIFO & CONTROL
CONFIG FLASH
7309
XC18V01
CONFIG ROM
7300
XC17S30XL
PLL AUDIO
7307
CY2071AS
PLL VIDEO
7308
CY2071AS
7304
FXO-31FT
FPGA / EPLD
7303
XCS30XL
SRAM
7301
CY7C1019BV33-10VC
6300
LD1117
+3V3_FPGA_CONF
+3V3_FPGA
+3V3_PLL
+3V3_SRAM
+5V_PROC
CLK27M
CLK27M_DV
CLK27M_CON
CLK27M_OSC
HAD(7:0)
(TDI,TCK,TDO,TDO_CONF,TMS)
{DV_LCn,DV_ERRn,DV_DRQn,DV_DTACKn,DV_ASn,DV_PDn,DV_DSUn,DV_RWn,DV_VS,DV_HS_IN,DV_RSTn,DV_HS_OUT,DV_DSLn}
{DATA,CCLK,DONE,INITn,PROGRAMn}
{LINK_CYCLEOUT,LINK_AVCLK,LINK_AVSYNC,LINK_AVVALID,LINK_AVFSYNC,LINK_AVERR1,LINK_AVERR0,LINK_CSn,LINK_INTn,LINK_AVREADY}
LINKFIFO_DQ(0:7)
{SRAMCE0n,SRAMRDn,PINT0n,PINT1n,PALE,PWRn,PRDn,PRSTn}
PA(8:15)
PAD(7:0)
{AUD_BCLK,AUD_WS_OUT,AUD_WS_701,AUD_MUTE,AUD_SDI,AUD_SDO_DAC,AUD_SDO_CON}
FIFOA_A(16:0)
FIFOA_D(7:0)
BUFENn_VID
BUFENn_AUD
CL 16532145_016.eps
221101

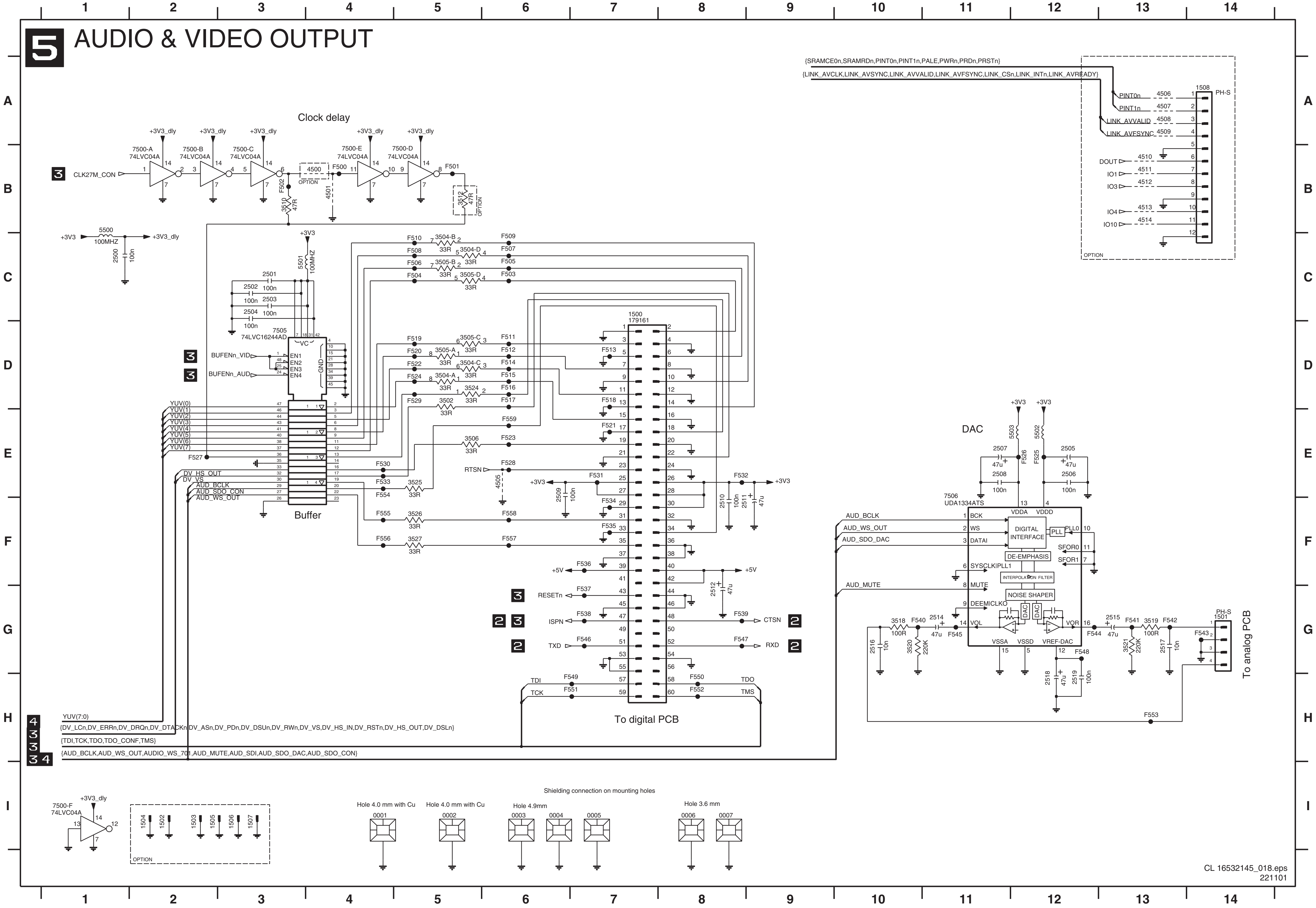
2301	I3
2302	I4
2303	F4
2304	C8
2305	F3
2306	I9
2307	I9
2308	I9
2309	I9
2310	I9
2311	I10
2312	I10
2313	I10
2314	I8
2318	D3
2319	D3
2324	I12
2325	I12
2330	A4
2331	B4
2332	B4
3300	G9
3301	B11
3303	E12
3305	B1
3306	B1
3307	C1
3312	F5
3313	H9
3314	H9
3315	D7
3317	G3
3318	G3
3319	G3
3320	D7
3321	D7
3322	C10
3325	D7
3327	C9
3328	G10
3329	G11
3330	C8
3331	D7
4300	B1
4301	E4
4302	A2
5300	C7
5301	F2
5302	I8
5303	A1
5304	I12
6300	I3
7300	D2
7301	F13
7303	D10
7304	F4
7307	C7
7308	F2
7309	A2
F300	F5
F301	C8
F302	C8
F303	D7
F304	D7
F305	G3
F306	C10
F307	G3
F308	G3
F309	D7
F310	D7
F311	I10
F312	A2
F313	I12
F314	C7
F315	C8
F316	B2
F317	F2
F318	H9
F319	B2
F320	H9
F321	G3
F322	B2
F323	G3
F324	B2
F325	I4
F326	B3
F328	E4
F329	G3
F330	D7
F331	C8
F332	C8
F333	E12
F335	B10
F336	B8

DVIO Board: DVCODEC


4 DVCODEC
DV Decoder
7404
NW700LQ
GENERAL PURPOSE I/O
HOST AD BUS [0....15]
AUDIO INTERFACE
VIDEO BUS
VIDEO BUS CLOCK INPUTS
SYNCHRONOUS VIDEO INTERFACE
DRAM CTRL
DRAM ADDRESS BUS
DRAM DATA [0...31] BUS
IO(31:0)
A(0:8)
7402
MT4LC1M16E5
7403
MT4LC1M16E5
EDO RAM 1Mx16
+VCC_DV_RAM
CRTL{RASn,LCASn,UCASn,WEn}
1Mx16 devices are used as 256kx16
DV_DTACKn
DV_DRQn
DV_ERRn
DV_LCn
DV_RSTn
DV_RWn
DV_DSLn
DV_DSUn
DV_PDn
DV_ASn
HAD(0)
HAD(1)
HAD(2)
HAD(3)
HAD(4)
HAD(5)
HAD(6)
HAD(7)
AUD_WS_701
AUD_BCLK
AUD_SDI
+3V3_DV
+35V_DV_EDO
3400 10K
3405 47R
3401-A 47R
3401-B 47R
3401-C 47R
3401-D 47R
3402-A 47R
3402-B 47R
3402-C 47R
3402-D 47R
3403 47R
3404 47R
CLK27M_DV
DV_VS
DV_HS_IN
YUV(0)
YUV(1)
YUV(2)
YUV(3)
YUV(4)
YUV(5)
YUV(6)
YUV(7)
HAD(7:0)
YUV(7:0)
{DV_LCn,DV_ERRn,DV_DRQn,DV_DTACKn,DV_ASn,DV_PDn,DV_DSUn,DV_RWn,DV_VS,DV_HS_IN,DV_RSTn,DV_HS_OUT,DV_DSLn}
{AUD_BCLK,AUD_WS_OUT,AUD_WS_701,AUD_MUTE,AUD_SDI,AUD_SDO_DAC,AUD_SDO_CON}
+3V3
5402 100MHZ
F416
+5V
OPTION
5400 100MHZ
5403 100MHZ
F425
5401 100MHZ
5404 100MHZ
F417
2400 100n
2401 100n
2402 100n
2403 100n
2404 100n
2405 100n
2406 100n
2407 100n
2408 100n
2409 100n
2410 100n
2411 100n
2412 100n
2413 100n
2414 100n
2415 100n
2416 100n
2417 100n
2418 100n
2419 100n
2420 100n
2421 100n
CL 16532145_017.eps
221101

2400	I6
2401	I6
2402	I6
2403	I7
2404	I7
2405	I7
2406	I8
2407	I8
2408	I8
2409	I8
2410	I10
2411	I10
2412	I11
2413	I11
2414	I11
2415	I12
2416	I13
2417	I13
2418	I14
2419	I14
2420	I14
2421	I15
3400	B4
3401-A	H5
3401-B	G5
3401-C	H5
3401-D	G5
3402-A	H6
3402-B	G6
3402-C	H6
3402-D	G6
3403	G6
3404	G7
3405	F3
5400	H10
5401	H13
5402	I5
5403	I10
5404	I13
7402	C9
7403	C11
7404	C4
F400	B4
F401	F3
F402	F4
F403	F3
F404	G6
F405	G7
F406	F5
F407	F5
F408	F5
F409	H6
F410	G6
F411	F6
F412	F6
F413	F6
F414	F6
F416	I9
F417	I15
F418	G7
F419	F6
F420	H6
F421	H6
F422	H7
F425	I12
F426	F4

DVIO Board: Audio & Video Output


5
AUDIO & VIDEO OUTPUT
Clock delay
CLK27M_CON
7500-A 74LVC04A
7500-B 74LVC04A
7500-C 74LVC04A
7500-E 74LVC04A
7500-D 74LVC04A
+3V3_dly
4500
OPTION
F500
F501
F502
3510 47R
3512 47R
4501
+3V3
5500 100MHZ
2500 100n
5501 100MHZ
2501
2502 100n
2503 100n
2504 100n
7505 74LVC16244AD
BUFENn_VID
BUFENn_AUD
EN1
EN2
EN3
EN4
VC
GND
YUV(0)
YUV(1)
YUV(2)
YUV(3)
YUV(4)
YUV(5)
YUV(6)
YUV(7)
F527
DV_HS_OUT
DV_VS
AUD_BCLK
AUD_SDO_CON
AUD_WS_OUT
Buffer
3504-A 33R
3504-B 33R
3504-C 33R
3504-D 33R
3505-A 33R
3505-B 33R
3505-C 33R
3505-D 33R
3502 33R
3524 33R
3506 33R
3525 33R
3526 33R
3527 33R
RTSN
4505
2509 100n
1500 179161
To digital PCB
+5V
RESETn
ISPN
TXD
CTSN
RXD
TDI
TCK
TDO
TMS
2510 100n
2511 47u
2512 47u
{SRAMCE0n,SRAMRDn,PINT0n,PINT1n,PALE,PWRn,PRDn,PRSTn}
{LINK_AVCLK,LINK_AVSYNC,LINK_AVVALID,LINK_AVFSYNC,LINK_CSn,LINK_INTn,LINK_AVREADY}
PINT0n
PINT1n
LINK_AVVALID
LINK_AVFSYNC
DOUT
IO1
IO3
IO4
IO10
4506
4507
4508
4509
4510
4511
4512
4513
4514
1508 PH-S
DAC
5502
5503
2505 47u
2506 100n
2507 47u
2508 100n
7506 UDA1334ATS
AUD_BCLK
AUD_WS_OUT
AUD_SDO_DAC
AUD_MUTE
BCK
WS
DATAI
SYSCLKIPLL1
MUTE
DEEMICLKO
VOL
VDDA
VDDD
DIGITAL INTERFACE
PLL
PLL0
SFOR0
SFOR1
DE-EMPHASIS
INTERPOLATION FILTER
NOISE SHAPER
DAC
VOR
VSSA
VSSD
VREF-DAC
3518 100R
3519 100R
3520 220K
3521 220K
2514 47u
2515 47u
2516 10n
2517 10n
2518 47u
2519 100n
1501 PH-S
To analog PCB
YUV(7:0)
{DV_LCn,DV_ERRn,DV_DRQn,DV_DTACKn,DV_ASn,DV_PDn,DV_DSUn,DV_RWn,DV_VS,DV_HS_IN,DV_RSTn,DV_HS_OUT,DV_DSLn}
{TDI,TCK,TDO,TDO_CONF,TMS}
{AUD_BCLK,AUD_WS_OUT,AUDIO_WS_701,AUD_MUTE,AUD_SDI,AUD_SDO_DAC,AUD_SDO_CON}
7500-F 74LVC04A
1504
1502
1503
1505
1506
1507
Shielding connection on mounting holes
Hole 4.0 mm with Cu
Hole 4.9mm
Hole 3.6 mm
0001
0002
0003
0004
0005
0006
0007
CL 16532145_018.eps
221101

0001	I4
0002	I5
0003	I6
0004	I6
0005	I7
0006	I8
0007	I8
1500	C7
1501	G14
1502	I2
1503	I2
1504	I2
1505	I2
1506	I3
1507	I3
1508	A14
2500	C1
2501	C3
2502	C3
2503	C3
2504	C3
2505	E12
2506	E12
2507	E11
2508	E11
2509	E6
2510	F8
2511	F8
2512	G8
2514	G11
2515	G13
2516	G10
2517	G13
2518	H12
2519	H12
3502	D5
3504-A	D5
3504-B	C5
3504-C	D5
3504-D	C5
3505-A	D5
3505-B	C5
3505-C	D5
3505-D	C5
3506	E5
3510	B3
3511	B4
3512	B5
3518	G10
3519	G13
3520	G10
3521	G13
3524	D5
3525	E5
3526	F5
3527	F5
4500	B4
4505	E6
4506	A13
4507	A13
4508	A13
4509	A13
4510	B13
4511	B13
4512	B13
4513	B13
4514	B13
5500	B1
5501	C3
5502	E12
5503	E12
7500-A	B2
7500-B	B2
7500-C	B3
7500-D	B4
7500-E	B4
7500-F	I1
7505	D3
7506	F11
F500	B4
F501	B5
F502	B3
F503	C6
F504	C5
F505	C6
F506	C5
F507	C6
F508	C5
F509	C6
F510	C5
F511	D6
F512	D6
F513	D7
F514	D6
F515	D6
F516	D6
F517	D6
F518	D7
F519	D5
F520	D5
F521	E7
F522	D5
F523	E6
F524	D5
F525	E12
F526	E12
F527	E2
F528	E6
F529	D5
F530	E4
F531	E7
F532	E8
F533	E4
F534	F7
F535	F7
F536	F7
F537	G7
F538	G7
F539	G8
F540	G10
F541	G13
F542	G13
F543	G14
F544	G12
F545	G11
F546	G7
F547	G8
F548	G12
F549	H7
F550	H8
F551	H7
F552	H8
F553	H13
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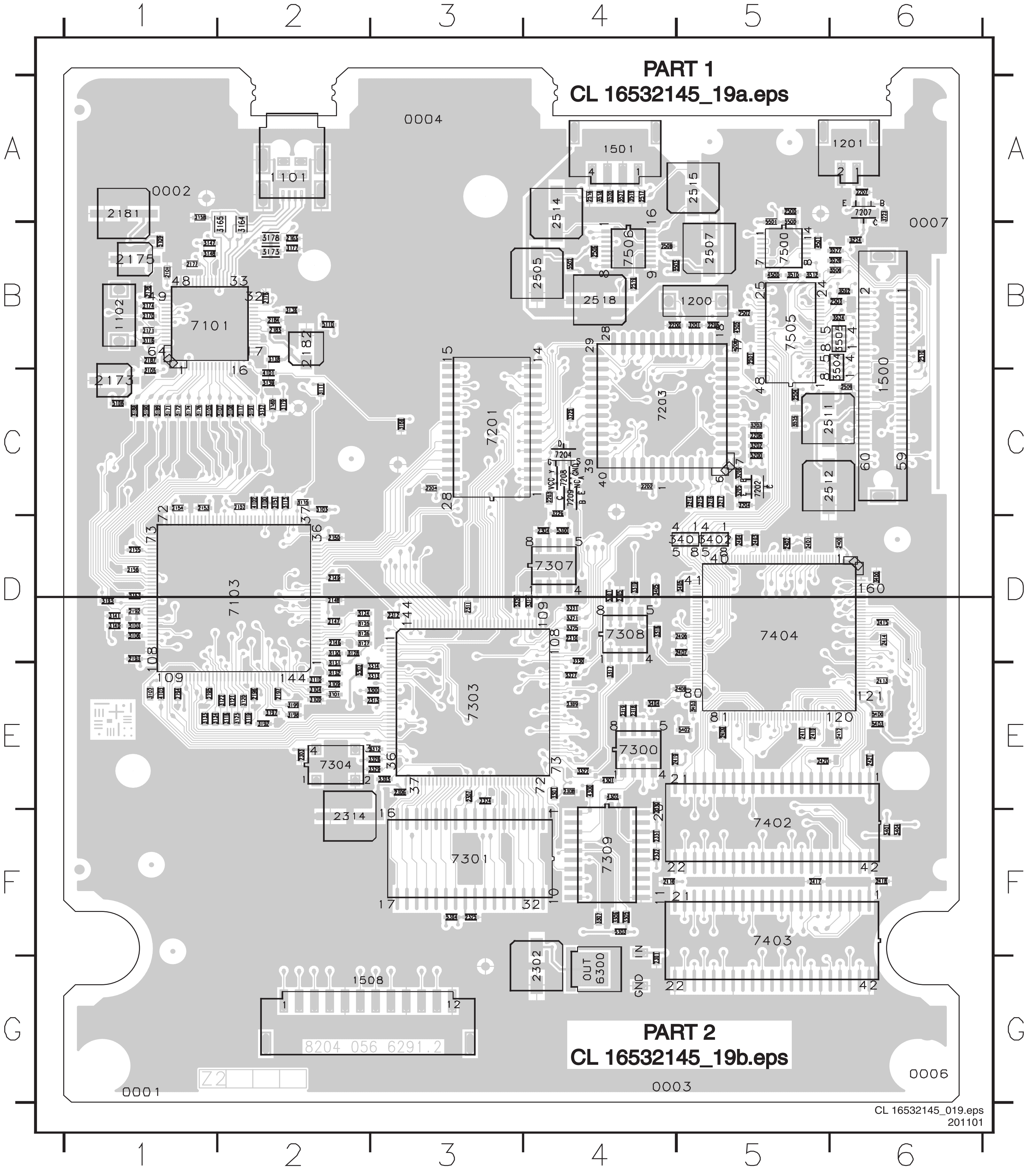
F556	F4
F557	F6
F558	F6
F559	E6

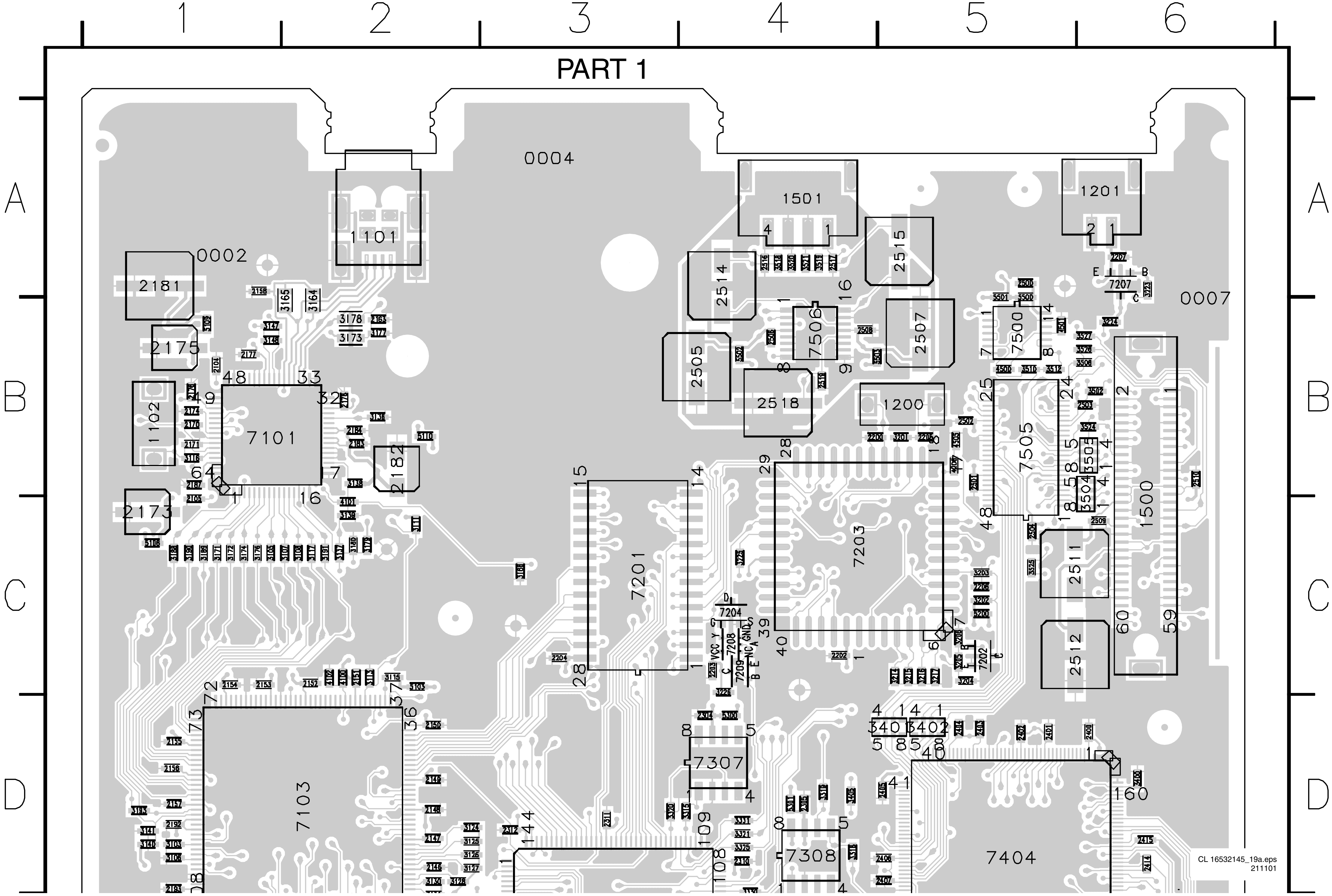
Layout DVIO Board (Overview Top View)


PART 1
CL 16532145_19a.eps
PART 2
CL 16532145_19b.eps
1
2
3
4
5
6
A
B
C
D
E
F
G
0004
0002
0007
0001
0003
0006
1101
1501
1201
2181
2175
2514
2515
7506
2507
2505
2518
1200
7500
7505
1500
1102
7101
2182
2173
7201
7203
7204
2511
2512
7103
7307
7308
7404
7303
7304
7300
2314
7402
7301
7309
7403
2302
OUT
6300
IN
GND
1508
8204 056 6291.2
Z2
CL 16532145_019.eps
201101

1101	A2	2332	F4	3130	D2	3331	D4	7403	F5
1102	B1	2400	D6	3131	E2	3400	D6	7404	D5
1200	B5	2401	D5	3132	E2	3401	D5	7500	B5
1201	A6	2402	D5	3133	E1	3402	D5	7505	B5
1500	C6	2403	D5	3134	E1	3403	E5	7506	B4
1501	A4	2404	D5	3136	B2	3404	E4		
1508	G2	2405	D5	3137	C2	3405	D4		
2104	B1	2406	D5	3138	B2	3502	B6		
2105	C1	2407	D5	3139	C2	3504	B6		
2146	D2	2408	E5	3140	D1	3505	B6		
2147	D2	2409	E5	3141	D1	3506	B6		
2148	D2	2410	E5	3147	B1	3510	B5		
2149	D2	2411	E5	3148	B1	3512	B5		
2150	D2	2412	E6	3164	B2	3518	A4		
2151	C2	2413	E6	3165	B2	3519	A4		
2152	C2	2414	D6	3166	C3	3520	A4		
2153	C1	2415	D6	3171	C1	3521	A4		
2154	C1	2416	F4	3172	C1	3524	B6		
2155	D1	2417	F5	3173	B2	3525	C5		
2156	D1	2418	F6	3174	C1	3526	B6		
2157	D1	2419	E4	3176	C1	3527	B6		
2158	A1	2420	E5	3177	B2	4100	C2		
2163	B2	2421	E6	3178	B2	4101	C2		
2170	B1	2500	A5	3179	C2	4102	C2		
2171	B1	2501	B5	3180	C2	4103	E1		
2173	C1	2502	B5	3188	C1	4206	B5		
2174	B1	2503	B6	3189	C1	4300	E4		
2175	B1	2504	C5	3190	C1	4301	E4		
2176	B1	2505	B4	3191	C2	4302	E4		
2177	B1	2506	B4	3192	E2	4500	B5		
2178	B2	2507	B5	3193	D1	4501	B5		
2181	A1	2508	B4	3197	E2	4505	B5		
2182	B2	2509	C6	3198	E2	5103	C2		
2183	B2	2510	B6	3199	E2	5106	C1		
2184	B2	2511	C5	3201	B5	5109	B1		
2187	B1	2512	C5	3202	C5	5110	B2		
2192	D1	2514	A4	3203	C5	5200	C5		
2193	D1	2515	A5	3204	C5	5300	D4		
2194	E1	2516	A4	3205	C5	5301	D4		
2195	E1	2517	A4	3206	C5	5302	E2		
2196	E2	2518	B4	3214	C5	5303	F4		
2197	E2	2519	B4	3215	C5	5304	F3		
2200	B4	3100	E2	3216	C5	5400	E6		
2202	C4	3101	E2	3217	C5	5401	F6		
2203	C4	3102	E1	3223	A6	5402	E5		
2204	C3	3103	D1	3224	B6	5403	E6		
2205	B5	3104	E2	3225	C4	5404	F6		
2206	C5	3105	C1	3226	C4	5500	A5		
2207	A6	3106	D1	3300	E3	5501	A5		
2301	G4	3107	C2	3301	E4	5502	B4		
2302	G4	3108	C2	3303	E3	5503	B4		
2303	E2	3109	E2	3305	F4	6300	G4		
2304	D4	3110	E2	3306	F4	7101	B1		
2305	D4	3111	C2	3307	F4	7103	D2		
2306	E3	3113	C2	3312	E3	7201	C3		
2307	E3	3115	C2	3313	E3	7202	C5		
2308	E4	3116	B1	3314	E3	7203	C4		
2309	E4	3117	C2	3315	D4	7204	C4		
2310	D4	3118	E2	3317	E4	7207	A6		
2311	D3	3119	E2	3318	D4	7208	C4		
2312	D3	3120	E2	3319	D4	7209	C4		
2313	E3	3121	E2	3320	D3	7300	E4		
2314	F2	3122	E2	3321	D4	7301	F3		
2318	E4	3123	E2	3322	E4	7303	E3		
2319	E4	3124	D2	3325	D4	7304	E2		
2324	E3	3125	D2	3327	E4	7307	D4		
2325	F3	3126	D2	3328	E3	7308	D4		
2330	E4	3127	D2	3329	E3	7309	F4		
2331	F4	3128	D2	3330	D4	7402	F5		

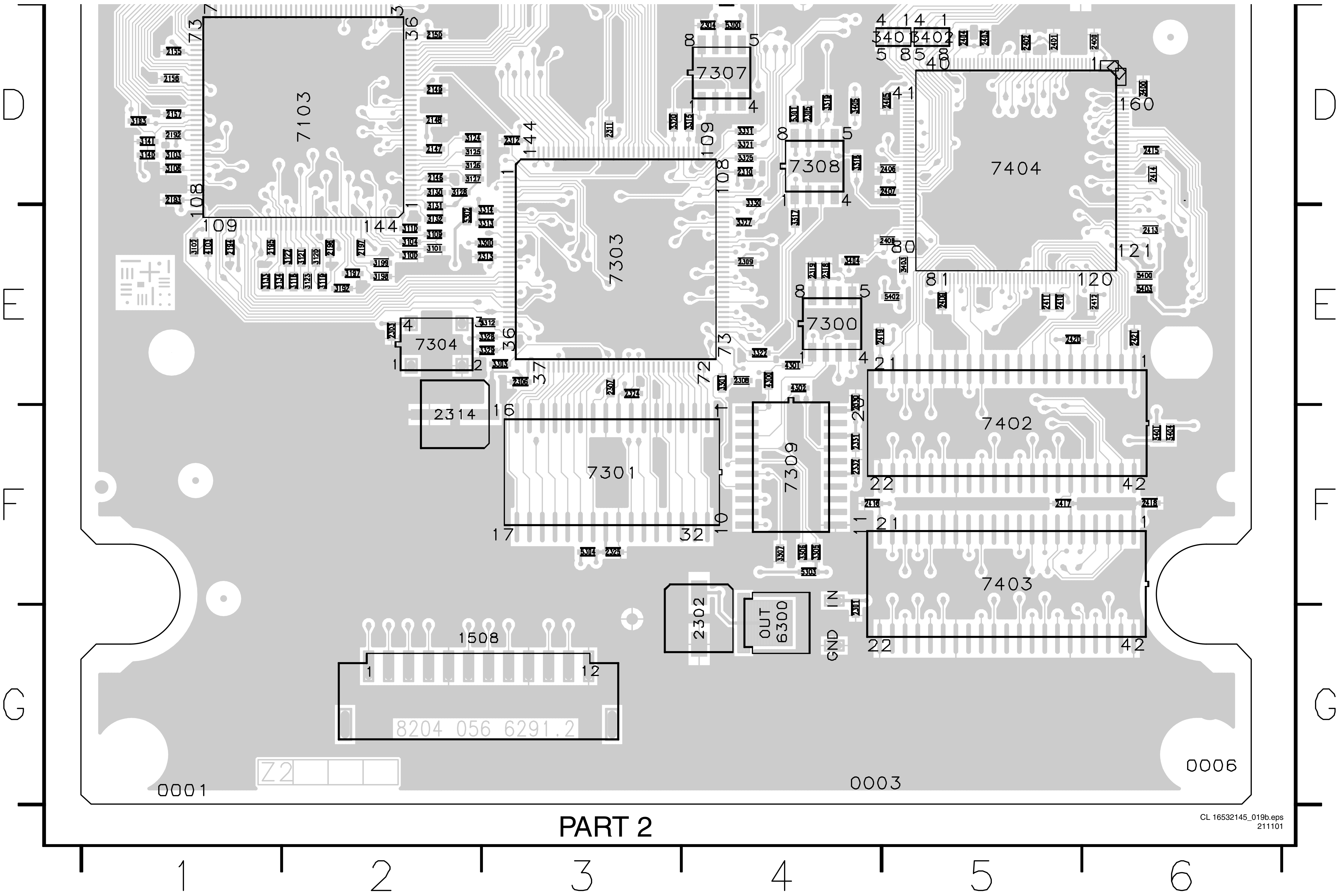
TR 01024_0

Layout DVIO Board (Part 1 Top View)


1
2
3
4
5
6
A
B
C
D
PART 1
0004
0002
0007
1101
1501
1201
2181
2175
1102
2173
7101
2182
2514
2515
2505
2518
7506
2507
1200
7500
7505
7207
1500
7201
7203
2511
2512
7204
7208
7209
7202
3401
3402
7307
7308
7103
7404
3164
3165
3178
3173
3503
3504

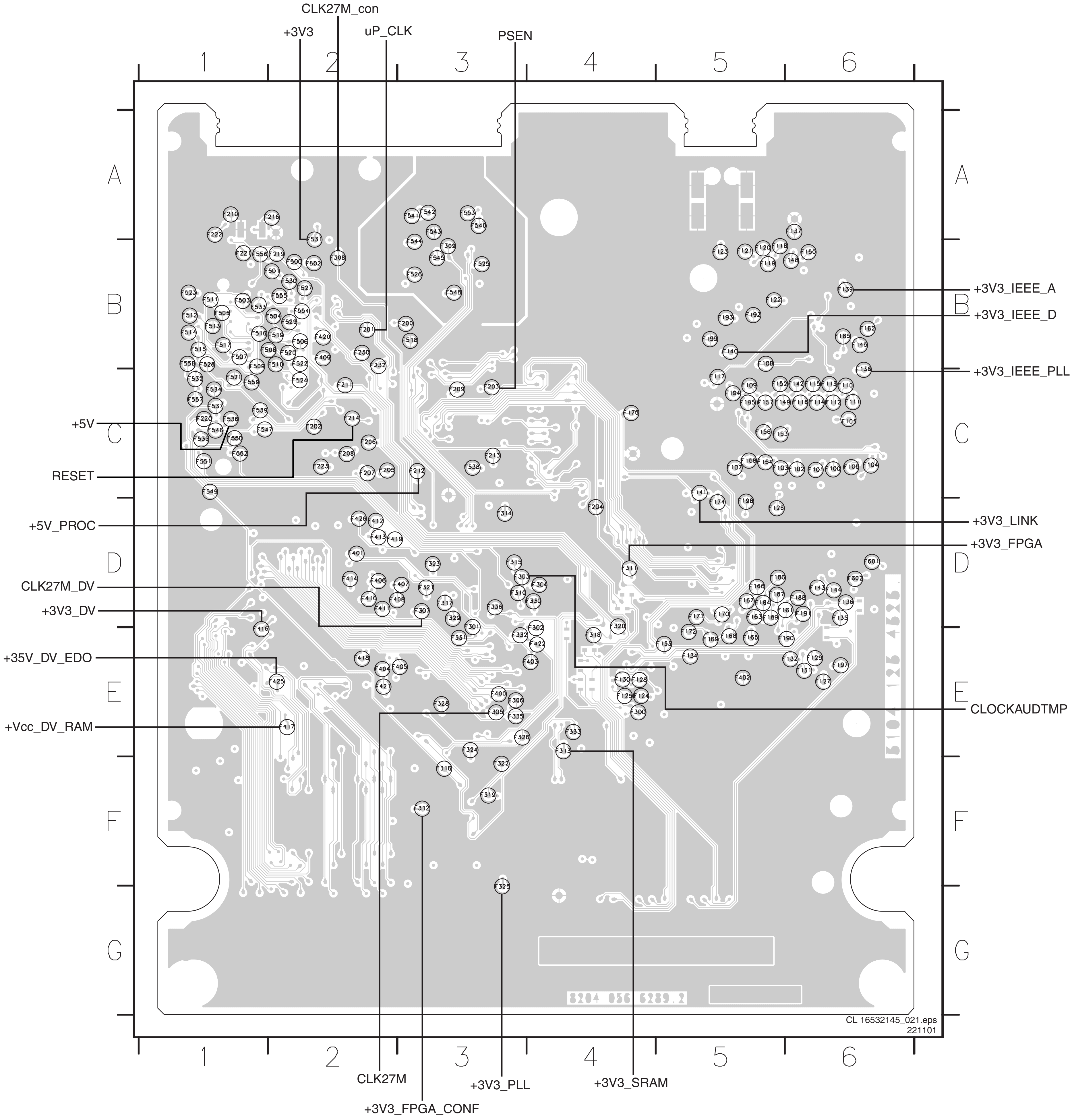
CL 16532145_19a.eps
211101

Layout DVIO Board (Part 2 Top View)


7103
73
37
36
108
109
144
1
7303
144
1
108
109
36
37
72
73
7307
8
5
1
4
3401
3402
7404
40
41
1
160
80
81
120
121
7308
8
5
1
4
7300
8
5
1
4
7304
4
3
1
2
2314
7301
16
17
32
7309
1
10
11
20
7402
21
1
22
42
7403
21
1
22
42
2302
OUT
6300
IN
GND
1508
1
12
8204 056 6291.2
Z2
0001
0003
0006
PART 2
D
E
F
G
1
2
3
4
5
6

CL 16532145_019b.eps
211101

Layout DVIO Board (Testlands Bottom View)



F100	C6
F100	C6
F101	C6
F101	C6
F102	C6
F102	C6
F103	C5
F103	C5
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F104	C6
F105	C6
F105	C6
F106	C6
F106	C6
F107	C5
F107	C5
F108	B5
F108	B5
F109	C5
F109	C5
F110	C6
F110	C6
F111	C6
F111	C6
F112	C6
F112	C6
F113	C6
F113	C6
F114	C6
F114	C6
F115	C6
F115	C6
F116	C6
F116	C6
F117	C5
F117	C5
F118	B5
F118	B5
F119	B5
F119	B5
F120	B5
F120	B5
F121	B5
F121	B5
F122	B5
F122	B5
F123	B5
F123	B5
F124	E4
F124	E4
F125	E4
F125	E4
F126	D5
F126	D5
F127	E6
F127	E6
F128	E4
F128	E4
F129	E6
F129	E6
F130	E4
F130	E4
F131	E6
F131	E6
F132	E6
F132	E6
F133	E5
F133	E5
F134	E5
F134	E5
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F135	D6
F136	D6
F136	D6
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F137	A6
F138	C6
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F139	B6
F139	B6
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F140	B5
F141	C5
F141	C5
F142	C6
F142	C6
F143	D6
F143	D6
F144	D6
F144	D6
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F146	B6
F148	B6
F148	B6
F149	C5
F149	C5
F150	B6
F150	B6
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F152	C5
F153	C5
F153	C5
F154	C5
F154	C5
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F156	C5
F157	C5
F157	C5
F158	C5
F158	C5
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F187	D5
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F189	D5
F190	E6
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F191	D6
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F208	C2
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F211	C2
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F219	B2
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F220	C1
F220	C1
F221	B1
F221	B1
F222	A1
F222	A1
F223	C2
F223	C2
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F232	B2
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F303	D3
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F421	E2
F421	E2
F422	E4
F422	E4
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F501	B2
F502	B2
F502	B2
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F523	B1
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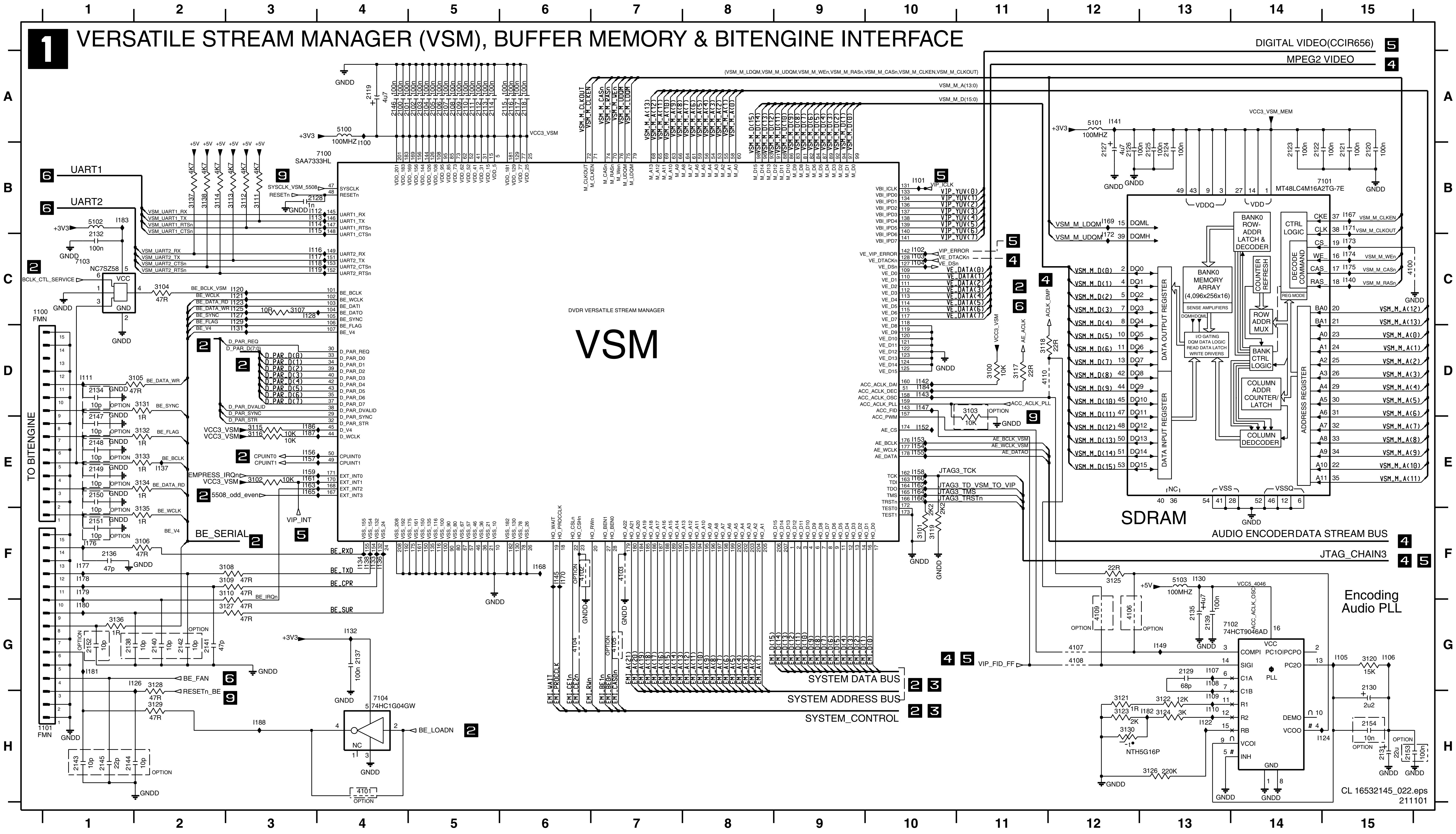
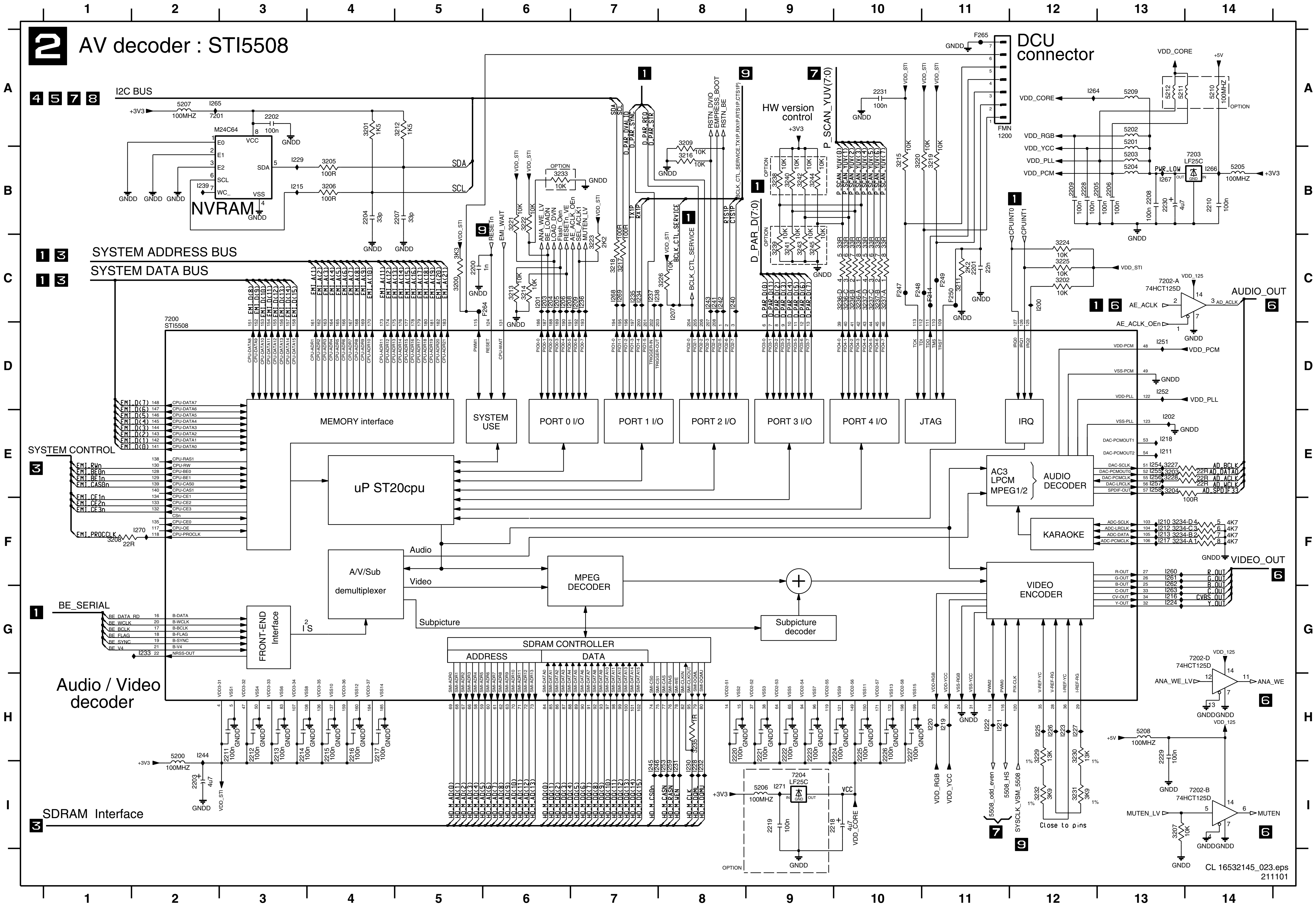
F531	B2
F532	C1
F532	C1
F533	B1
F533	B1
F534	C1
F534	C1
F535	C1
F535	C1
F536	C1
F536	C1
F537	C1
F537	C1
F538	C3
F538	C3
F539	C1
F539	C1
F540	A3
F540	A3
F541	A3
F541	A3
F542	A3
F542	A3
F543	A3
F543	A3
F544	B3
F544	B3
F545	B3
F545	B3
F546	C1
F546	C1
F547	C1
F547	C1
F548	B3
F548	B3
F549	C1
F549	C1
F550	C1
F550	C1
F551	C1
F551	C1
F552	C1
F552	C1
F553	A3
F553	A3
F554	B2
F554	B2
F555	B2
F555	B2
F556	B1
F556	B1
F557	C1

Digital Board: VSM, Buffer Memory and Bit Engine Interface

1100	C1	2106	A5	2114	A5	2122	B14	2130	G15	2139	G13	2147	D1	3102	E3	3110	F3	3118	D11	3126	H12	3134	E2	4103	F7	7101	B14
1101	H1	2107	A5	2115	A6	2123	B14	2131	H15	2140	G2	2148	E1	3103	D11	3111	B3	3119	F10	3127	G3	3135	E2	4104	G6	7102	G13
2100	A4	2108	A5	2116	A6	2124	B13	2132	B1	2141	G2	2149	E1	3104	C2	3112	B3	3120	G15	3128	G2	3136	G1	4105	G7	7103	C1
2101	A5	2109	A5	2117	A6	2125	B13	2134	D1	2142	G2	2150	E1	3105	D2	3113	B3	3121	G12	3129	H2	3137	B2	5100	A4	7104	H4
2102	A5	2110	A5	2118	A6	2126	B12	2135	G13	2143	H1	2151	F1	3106	F2	3114	B2	3122	H12	3130	H12	3138	B2	5101	A12		
2103	A5	2111	A5	2119	A4	2127	B12	2136	F1	2144	H1	2152	G1	3107	C3	3115	E3	3123	H12	3131	D2	4100	C15	5102	B1		
2104	A5	2112	A5	2120	B15	2128	B3	2137	G4	2145	H1	3100	D11	3108	F3	3116	E3	3124	H12	3132	E2	4101	H4	5103	F13		
2105	A5	2113	A5	2121	B15	2129	G13	2138	G1	2146	A4	3101	F10	3109	F3	3117	D11	3125	G14	3133	E2	4102	F6	7100	B4		

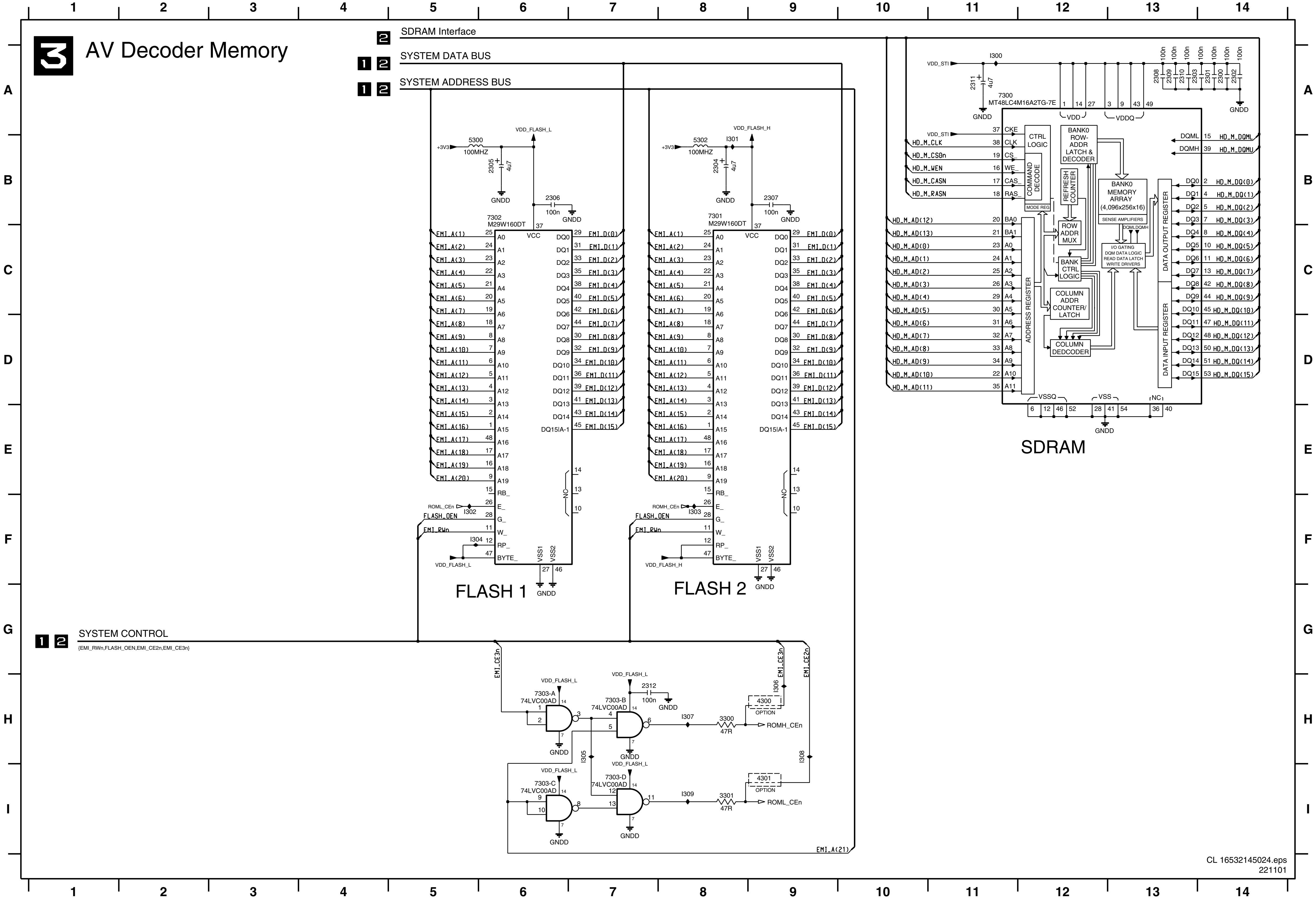

1
VERSATILE STREAM MANAGER (VSM), BUFFER MEMORY & BITENGINE INTERFACE
DIGITAL VIDEO(CCIR656)
MPEG2 VIDEO
VSM
DVDR VERSATILE STREAM MANAGER
7100
SAA7333HL
UART1
UART2
TO BITENGINE
BE_SERIAL
SDRAM
7101
MT48LC4M16A2TG-7E
BANK0 ROW-ADDR LATCH & DECODER
BANK0 MEMORY ARRAY (4,096x256x16)
SENSE AMPLIFIERS
I/O GATING DQM DATA LOGIC READ DATA LATCH WRITE DRIVERS
DATA OUTPUT REGISTER
DATA INPUT REGISTER
COUNTER REFRESH
ROW ADDR MUX
BANK CTRL LOGIC
COLUMN ADDR COUNTER/ LATCH
COLUMN DEDCODER
CTRL LOGIC
DECODE COMMAND
ADDRESS REGISTER
AUDIO ENCODERDATA STREAM BUS
JTAG_CHAIN3
SYSTEM DATA BUS
SYSTEM ADDRESS BUS
SYSTEM_CONTROL
Encoding Audio PLL
7102
74HCT9046AD
7103
NC7SZ58
7104
74HC1G04GW
BE_LOADN
VIP_FID_FF
BE_FAN
RESETn_BE
VIP_INT
5508_odd_event
EMPRESS_IRQn
CL 16532145_022.eps
211101

Digital Board: AV Decoder STI5508


2 AV decoder : STI5508
I2C BUS
NVRAM
M24C64
SYSTEM ADDRESS BUS
SYSTEM DATA BUS
SYSTEM CONTROL
BE_SERIAL
SDRAM Interface
DCU connector
HW version control
P_SCAN_YUV(7:0)
D_PAR_D(7:0)
AUDIO_OUT
VIDEO_OUT
7200 STI5508
MEMORY interface
SYSTEM USE
PORT 0 I/O
PORT 1 I/O
PORT 2 I/O
PORT 3 I/O
PORT 4 I/O
JTAG
IRQ
uP ST20cpu
AC3 LPCM MPEG1/2
AUDIO DECODER
KARAOKE
A/V/Sub demultiplexer
Audio
Video
Subpicture
MPEG DECODER
Subpicture decoder
VIDEO ENCODER
FRONT-END Interface
SDRAM CONTROLLER
ADDRESS
DATA
Audio / Video decoder
Close to pins
OPTION
CL 16532145_023.eps
211101

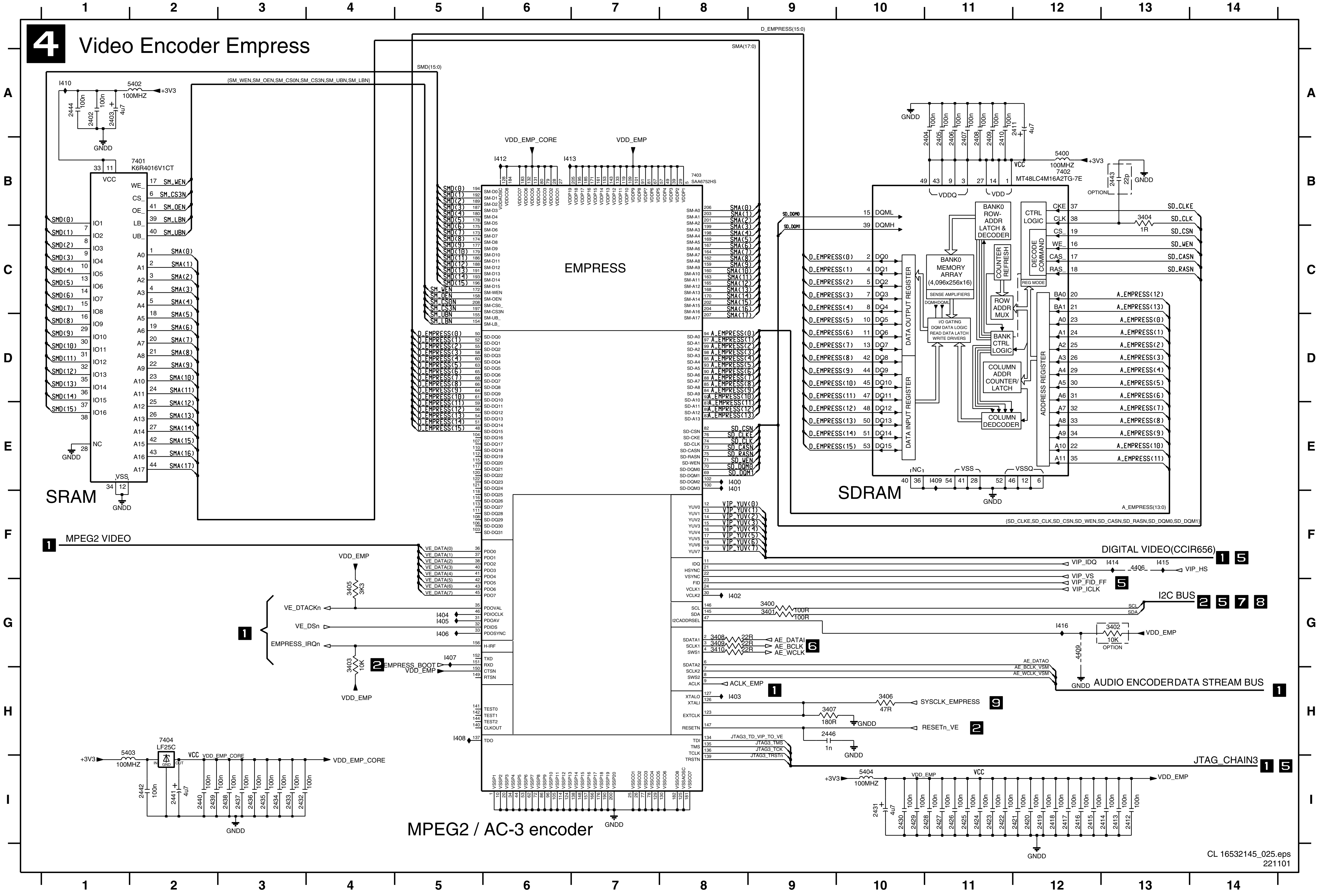
1200	A11
2200	C5
2201	C11
2202	A3
2203	I2
2204	B4
2205	B13
2206	B13
2207	B5
2208	B13
2209	B12
2210	B14
2211	H3
2212	H3
2213	H3
2214	H3
2215	H4
2216	H4
2217	H4
2218	I10
2219	I9
2220	H8
2221	H9
2222	H9
2223	H9
2224	H10
2225	H10
2226	H10
2227	H10
2228	B12
2229	H13
2230	B13
2231	A10
3200	C5
3201	A4
3202	C12
3203	E13
3204	E13
3205	B4
3206	B4
3207	I13
3208	F1
3209	A8
3211	C11
3212	A5
3213	C6
3214	C6
3215	B10
3216	B8
3217	C7
3218	C7
3219	B11
3220	B10
3221	B6
3222	B6
3223	C7
3224	C12
3225	C12
3226	C8
3227	E13
3228	E13
3229	H12
3230	H12
3231	I12
3232	I12
3233	B6
3234-A	F13
3234-B	F13
3234-C	F13
3234-D	F13
3235	H8
3236-A	C10
3236-B	C10
3236-C	C10
3236-D	C10
3237-A	C10
3237-B	C10
3237-C	C10
3237-D	C10
3238	B9
3239	C9
3240	B9
3241	C9
3242	B9
3243	C9
3244	B9
3245	C9
5200	H2
5201	A13
5202	A13
5203	B13
5204	B13
5205	B14
5206	I9
5207	A2
5208	H13
5209	A13
5210	A14
5211	A13
5212	A13
7200	C2
7201	A2
7202-A	C13
7202-B	I14
7202-D	G14
7203	B14
7204	I9
F214	C11
F247	C10
F248	C10
F249	C11
F250	C11
F264	C6
F265	A11

Digital Board: AV Decoder Memory


3
AV Decoder Memory
2 SDRAM Interface
1 2 SYSTEM DATA BUS
1 2 SYSTEM ADDRESS BUS
1 2 SYSTEM CONTROL
(EMI_RWn,FLASH_OEN,EMI_CE2n,EMI_CE3n)
7302 M29W160DT
FLASH 1
7301 M29W160DT
FLASH 2
7300 MT48LC4M16A2TG-7E
SDRAM
5300 100MHZ
5302 100MHZ
+3V3
VDD_FLASH_L
VDD_FLASH_H
VDD_STI
GNDD
CTRL LOGIC
COMMAND DECODE
MODE REG
BANK0 ROW-ADDR LATCH & DECODER
REFRESH COUNTER
BANK0 MEMORY ARRAY (4,096x256x16)
SENSE AMPLIFIERS
ROW ADDR MUX
BANK CTRL LOGIC
I/O GATING DQM DATA LOGIC READ DATA LATCH WRITE DRIVERS
COLUMN ADDR COUNTER/ LATCH
COLUMN DEDCODER
ADDRESS REGISTER
DATA OUTPUT REGISTER
DATA INPUT REGISTER
7303-A 74LVC00AD
7303-B 74LVC00AD
7303-C 74LVC00AD
7303-D 74LVC00AD
4300 OPTION
4301 OPTION
3300 47R
3301 47R
ROMH_CEn
ROML_CEn
EMI_CE3n
EMI_CE2n
EMI_A(21)
CL 16532145024.eps
221101

2300	A14
2301	A14
2302	A14
2303	A13
2304	B8
2305	B6
2306	B6
2307	B9
2308	A13
2309	A13
2310	A13
2311	A11
2312	H7
3300	H8
3301	I8
4300	H9
4301	I9
5300	B5
5302	B8
7300	A11
7301	B8
7302	B6
7303-A	H6
7303-B	H7
7303-C	I6
7303-D	I7

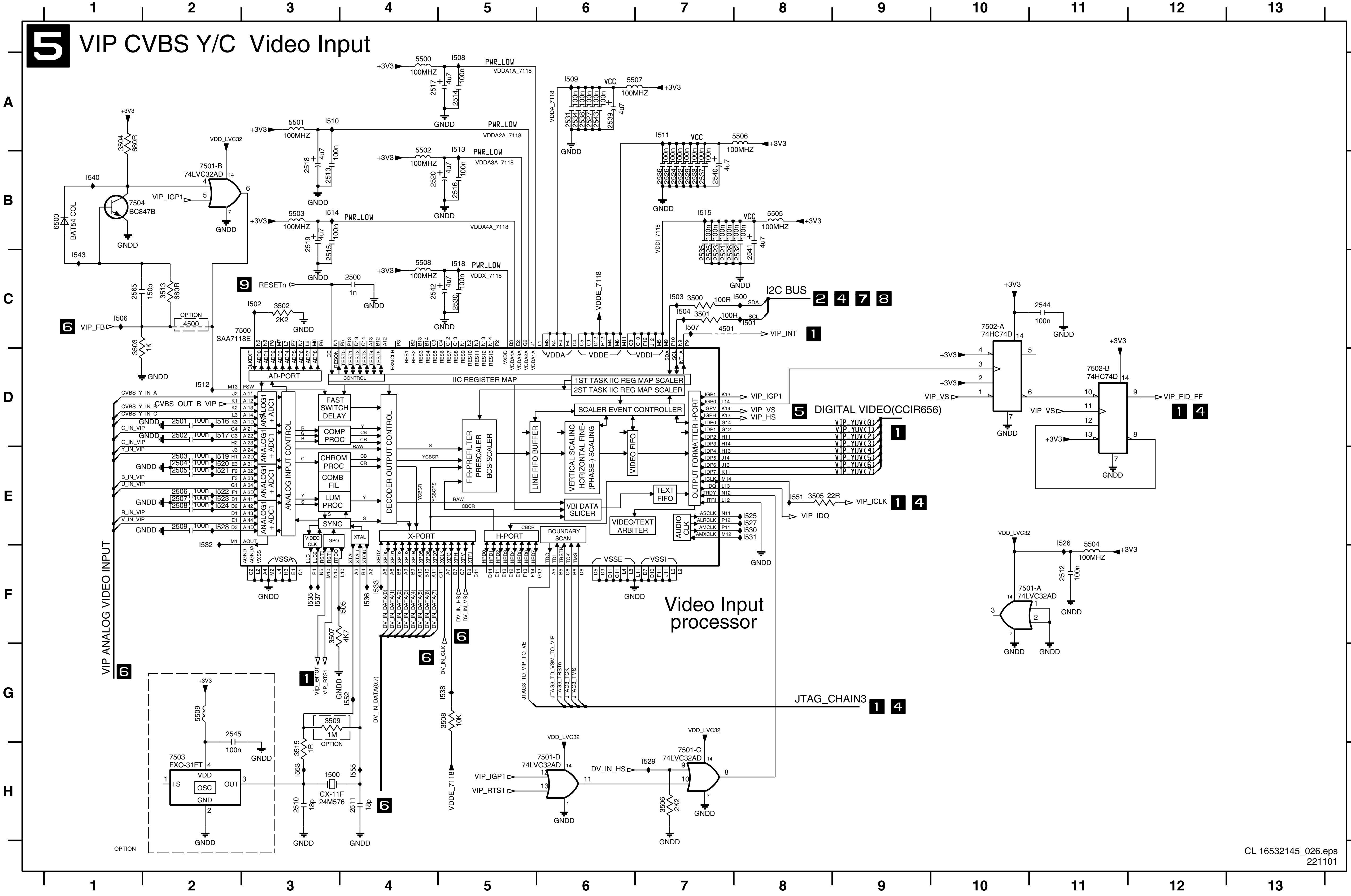
Digital Board: Video Encoder, Empress


4
Video Encoder Empress
SRAM
7401
K6R4016V1CT
EMPRESS
7403
SAA6752HS
SDRAM
7402
MT48LC4M16A2TG-7E
MPEG2 / AC-3 encoder
7404
LF25C
MPEG2 VIDEO
VE_DTACKn
VE_DSn
EMPRESS_IRQn
EMPRESS_BOOT
DIGITAL VIDEO(CCIR656)
VIP_IDQ
VIP_HS
VIP_VS
VIP_FID_FF
VIP_ICLK
I2C BUS
AE_DATAI
AE_BCLK
AE_WCLK
ACLK_EMP
AUDIO ENCODERDATA STREAM BUS
SYSCLK_EMPRESS
RESETn_VE
JTAG_CHAIN3
VDD_EMP_CORE
VDD_EMP
+3V3
GNDD
BANK0 MEMORY ARRAY (4,096x256x16)
DATA OUTPUT REGISTER
DATA INPUT REGISTER
ADDRESS REGISTER
CTRL LOGIC
DECODE COMMAND
COUNTER REFRESH
ROW ADDR MUX
BANK CTRL LOGIC
COLUMN ADDR COUNTER/ LATCH
COLUMN DEDCODER
BANK0 ROW-ADDR LATCH & DECODER
I/O GATING DQM DATA LOGIC READ DATA LATCH WRITE DRIVERS
SENSE AMPLIFIERS

CL 16532145_025.eps
221101

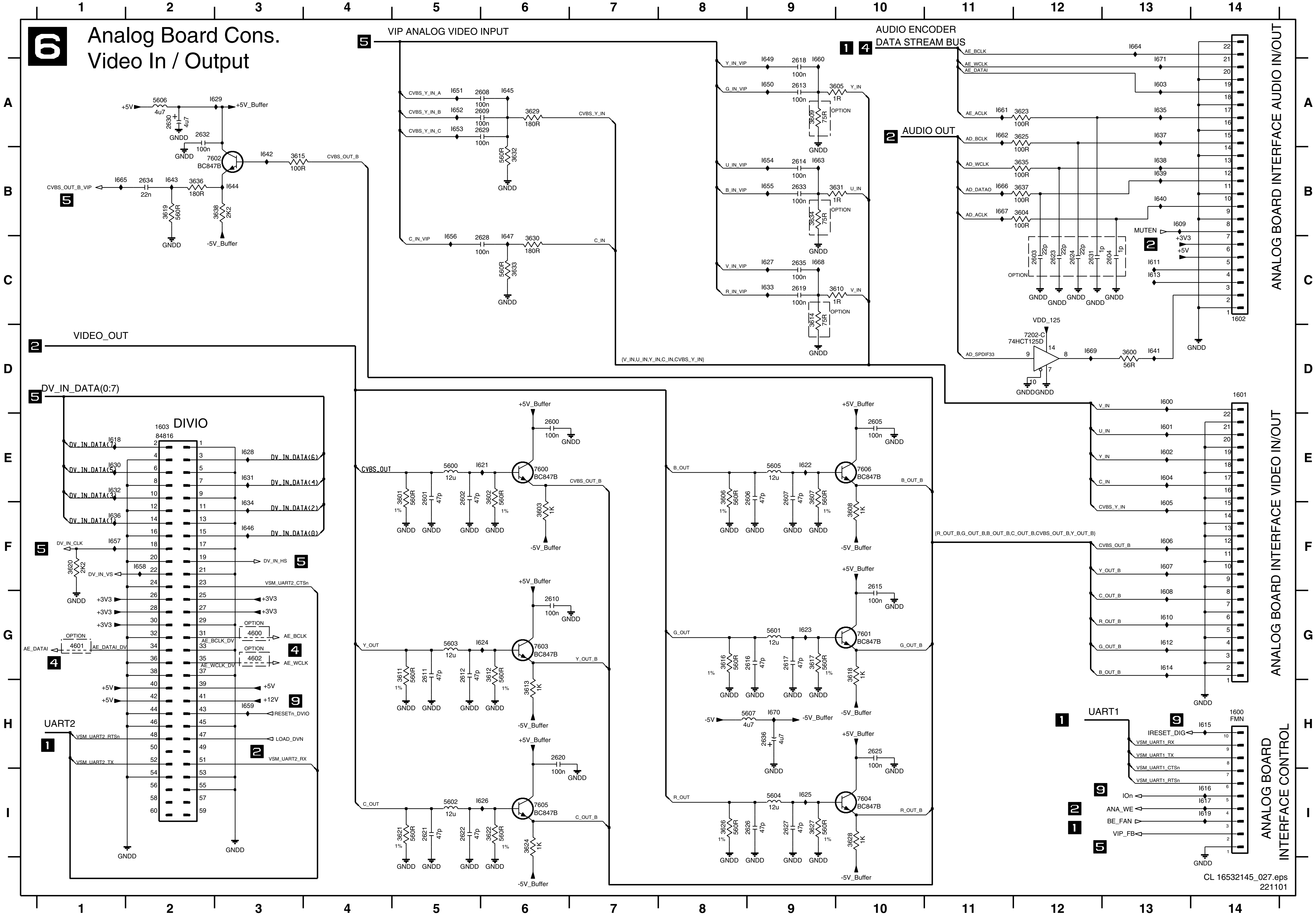
2402	A1
2403	A1
2404	B11
2405	B11
2406	B11
2407	B11
2408	B11
2409	B11
2410	B11
2411	A12
2412	I13
2413	I13
2414	I13
2415	I12
2416	I12
2417	I12
2418	I12
2419	I12
2420	I12
2421	I12
2422	I11
2423	I11
2424	I11
2425	I11
2426	I11
2427	I11
2428	I11
2429	I10
2430	I10
2431	I10
2432	I3
2433	I3
2434	I3
2435	I3
2436	I3
2437	I3
2438	I3
2439	I2
2440	I2
2441	I2
2442	I2
2443	B13
2444	A1
2446	H9
3400	G9
3401	G9
3402	G13
3403	G4
3404	B13
3405	G4
3406	H10
3407	H9
3408	G8
3409	G8
3410	G8
4406	F13
4409	G12
5400	B12
5402	A2
5403	H1
5404	I10
7401	B2
7402	B12
7403	B8
7404	H2

Digital Board: VIP CVBS Y/C Video Input


5 VIP CVBS Y/C Video Input
Video Input processor
7500 SAA7118E
I2C BUS 2 4 7 8
VIP_INT 1
DIGITAL VIDEO(CCIR656) 5
VIP_YUV(0) … VIP_YUV(7) 1
VIP_ICLK 1 4
VIP_IDQ
VIP_FID_FF 1 4
JTAG_CHAIN3 1 4
VIP ANALOG VIDEO INPUT 6
VIP_FB 6
RESETn 9
AD-PORT
IIC REGISTER MAP
1ST TASK IIC REG MAP SCALER
2ST TASK IIC REG MAP SCALER
SCALER EVENT CONTROLLER
ANALOG INPUT CONTROL
FAST SWITCH DELAY
COMP PROC
CHROM PROC
COMB FIL
LUM PROC
SYNC
DECODER OUTPUT CONTROL
FIR-PREFILTER PRESCALER BCS-SCALER
LINE FIFO BUFFER
VERTICAL SCALING HORIZONTAL FINE-(PHASE-) SCALING
VIDEO FIFO
OUTPUT FORMATTER I-PORT
TEXT FIFO
VBI DATA SLICER
VIDEO/TEXT ARBITER
AUDIO CLK
X-PORT
H-PORT
BOUNDARY SCAN
7501-A 74LVC32AD
7501-B 74LVC32AD
7501-C 74LVC32AD
7501-D 74LVC32AD
7502-A 74HC74D
7502-B 74HC74D
7503 FXO-31FT
7504 BC847B
6500 BAT54 COL
1500 CX-11F 24M576
OPTION
CL 16532145_026.eps
221101

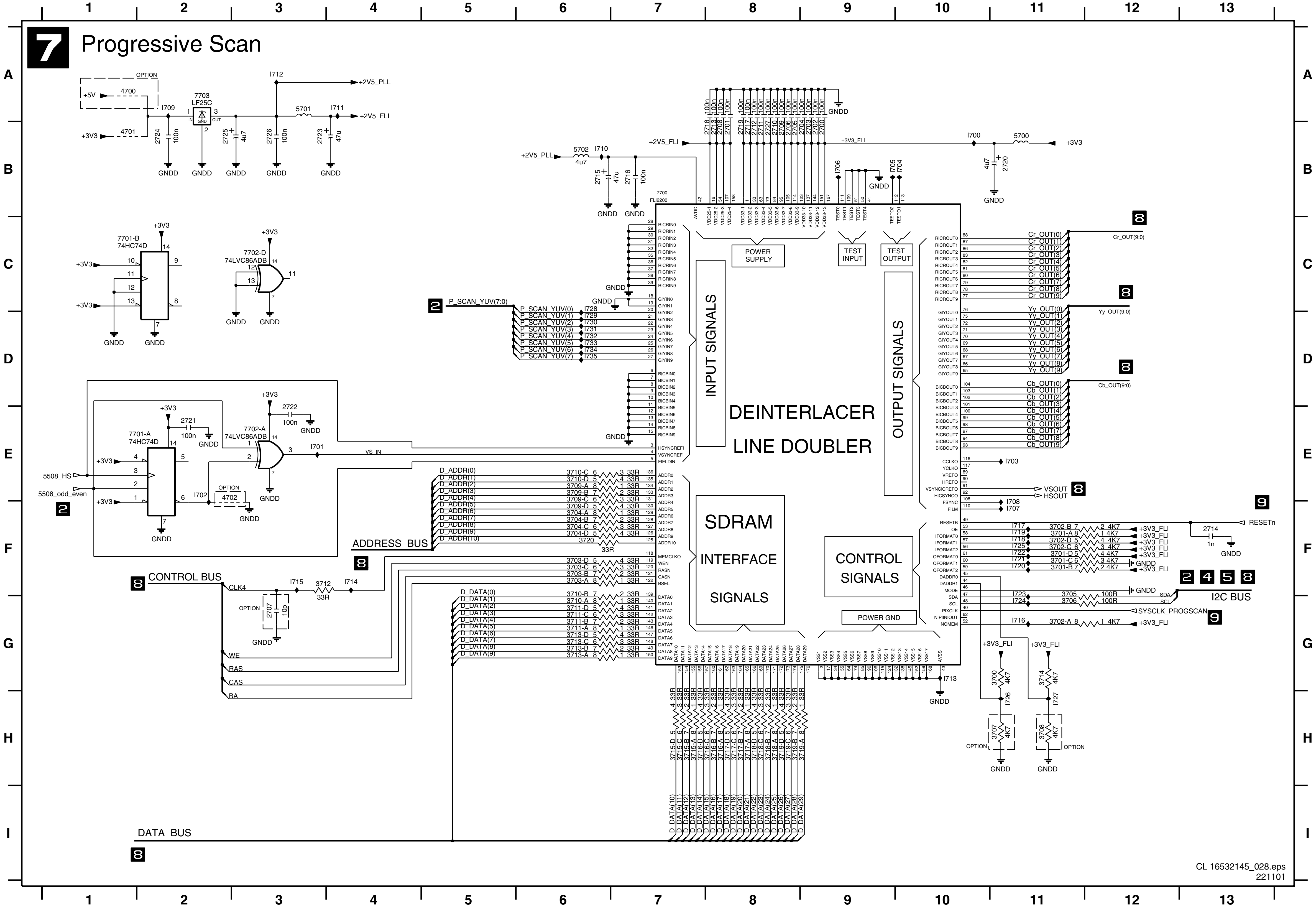
1500	H3
2500	C4
2501	D2
2502	D2
2503	E2
2504	E2
2505	E2
2506	E2
2507	E2
2508	E2
2509	E2
2510	H3
2511	H4
2512	F11
2513	B3
2514	A5
2515	C3
2516	B5
2517	A4
2518	B3
2519	B3
2520	B4
2521	C7
2522	B7
2523	C7
2524	B7
2525	C7
2526	B7
2527	A6
2528	C7
2529	B7
2530	C5
2531	A6
2532	C8
2533	B7
2534	A6
2535	C7
2536	B7
2537	B7
2538	A6
2539	A6
2540	B7
2541	B8
2542	C4
2543	A6
2544	C11
2545	G2
2565	C1
3500	C7
3501	C7
3502	C3
3503	C1
3504	A1
3505	E8
3506	H7
3507	F3
3508	G5
3509	G3
3513	C2
3515	H3
4500	C2
4501	C7
5500	A4
5501	A3
5502	A4
5503	B3
5504	E11
5505	B8
5506	A8
5507	A6
5508	C4
5509	G2
6500	B1
7500	C3
7501-A	F11
7501-B	B2
7501-C	H7
7501-D	H6
7502-A	C10
7502-B	D11
7503	H2
7504	B1

Digital Board: Analog Board Cons. Video In / Output


6
Analog Board Cons.
Video In / Output
1 2 3 4 5 6 7 8 9 10 11 12 13 14
A B C D E F G H I
VIP ANALOG VIDEO INPUT
AUDIO ENCODER
DATA STREAM BUS
AUDIO OUT
MUTEN
VIDEO_OUT
DV_IN_DATA(0:7)
DIVIO
1603
84816
UART2
UART1
ANALOG BOARD INTERFACE AUDIO IN/OUT
ANALOG BOARD INTERFACE VIDEO IN/OUT
ANALOG BOARD
INTERFACE CONTROL
1600
FMN
1601
1602
7202-C
74HCT125D
VDD_125
7600 BC847B
7601 BC847B
7602 BC847B
7603 BC847B
7604 BC847B
7605 BC847B
7606 BC847B
+5V_Buffer
-5V_Buffer
GNDD
CVBS_OUT_B_VIP
CVBS_OUT
Y_OUT
C_OUT
B_OUT
G_OUT
R_OUT
CVBS_OUT_B
Y_OUT_B
C_OUT_B
B_OUT_B
G_OUT_B
R_OUT_B
(V_IN,U_IN,Y_IN,C_IN,CVBS_Y_IN)
(R_OUT_B,G_OUT_B,B_OUT_B,C_OUT_B,CVBS_OUT_B,Y_OUT_B)
IRESET_DIG
IOn
ANA_WE
BE_FAN
VIP_FB
DV_IN_CLK
DV_IN_HS
DV_IN_VS
AE_BCLK
AE_WCLK
AE_DATAI
RESETn_DVIO
LOAD_DVN
VSM_UART2_RX
VSM_UART2_CTSn
OPTION
CL 16532145_027.eps
221101

1600	H14
1601	D14
1602	C14
1603	E2
2600	E6
2601	E5
2602	E5
2603	C12
2604	C13
2605	E10
2606	E9
2607	E9
2608	A6
2609	A6
2610	G6
2611	G5
2612	G5
2613	A9
2614	B9
2615	F10
2616	G9
2617	G9
2618	A9
2619	C9
2620	H6
2621	I5
2622	I5
2623	C12
2624	C12
2625	H10
2626	I9
2627	I9
2628	C6
2629	A6
2630	A2
2631	C12
2632	A2
2633	B9
2634	B2
2635	C9
2636	H9
3600	D13
3601	E5
3602	E6
3603	F6
3604	B12
3605	A10
3606	E8
3607	E9
3608	F10
3609	A9
3610	C10
3611	G5
3612	G6
3613	H6
3614	C9
3615	B3
3616	G8
3617	G9
3618	G10
3619	B2
3620	F1
3621	I5
3622	I6
3623	A12
3624	I6
3625	A12
3626	I8
3627	I9
3628	I10
3629	A6
3630	C6
3631	B10
3632	B6
3633	C6
3634	B9
3635	B12
3636	B2
3637	B12
3638	B3
4600	G3
4601	G1
4602	G3
5600	E5
5601	G9
5602	I5
5603	G5
5604	I9
5605	E9
5606	A2
5607	H9
7202-C	D12
7600	E6
7601	G10
7602	B3
7603	G6
7604	I10
7605	I6
7606	E10

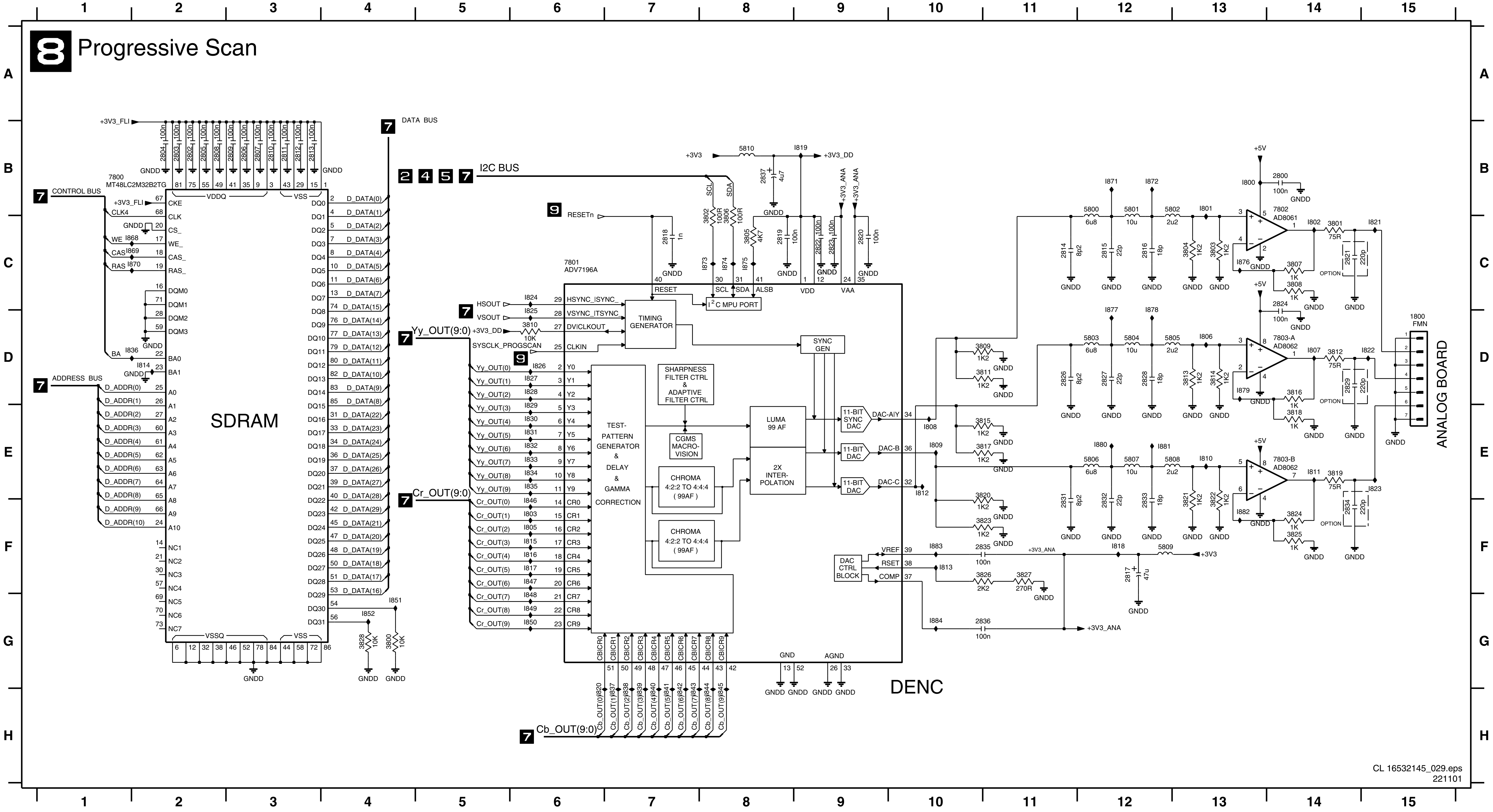
Digital Board: Progressive Scan


7
Progressive Scan
OPTION
+5V
4700
+3V3
4701
I709
7703
LF25C
IN
GND
OUT
I712
+2V5_PLL
5701
I711
+2V5_FLI
2724
100n
2725
4u7
2726
100n
2723
47u
GNDD
5702
4u7
I710
2715
47u
2716
100n
7700
FLI2200
I700
5700
+3V3_FLI
2720
4u7
I706
I705
I704
7701-B
74HC74D
7702-D
74LVC86ADB
7701-A
74HC74D
7702-A
74LVC86ADB
2721
100n
2722
100n
5508_HS
5508_odd_even
I701
VS_IN
I702
4702
P_SCAN_YUV(7:0)
I728
I729
I730
I731
I732
I733
I734
I735
POWER SUPPLY
TEST INPUT
TEST OUTPUT
INPUT SIGNALS
OUTPUT SIGNALS
DEINTERLACER
LINE DOUBLER
SDRAM
INTERFACE
SIGNALS
CONTROL
SIGNALS
POWER GND
Cr_OUT(9:0)
Yy_OUT(9:0)
Cb_OUT(9:0)
I703
VSOUT
HSOUT
I708
I707
RESETn
2714
1n
I717
I719
I718
I725
I722
I721
I720
+3V3_FLI
I2C BUS
SDA
SCL
I723
I724
3705
3706
100R
SYSCLK_PROGSCAN
I716
3702-A
1 4K7
3700
4K7
3714
4K7
I726
I727
3707
4K7
3708
4K7
I713
ADDRESS BUS
D_ADDR(0)
D_ADDR(10)
3720
33R
CONTROL BUS
CLK4
I715
3712
33R
I714
2707
10p
WE
RAS
CAS
BA
D_DATA(0)
D_DATA(9)
D_DATA(10)
D_DATA(29)
DATA BUS
2
8
9
2 4 5 8
CL 16532145_028.eps
221101

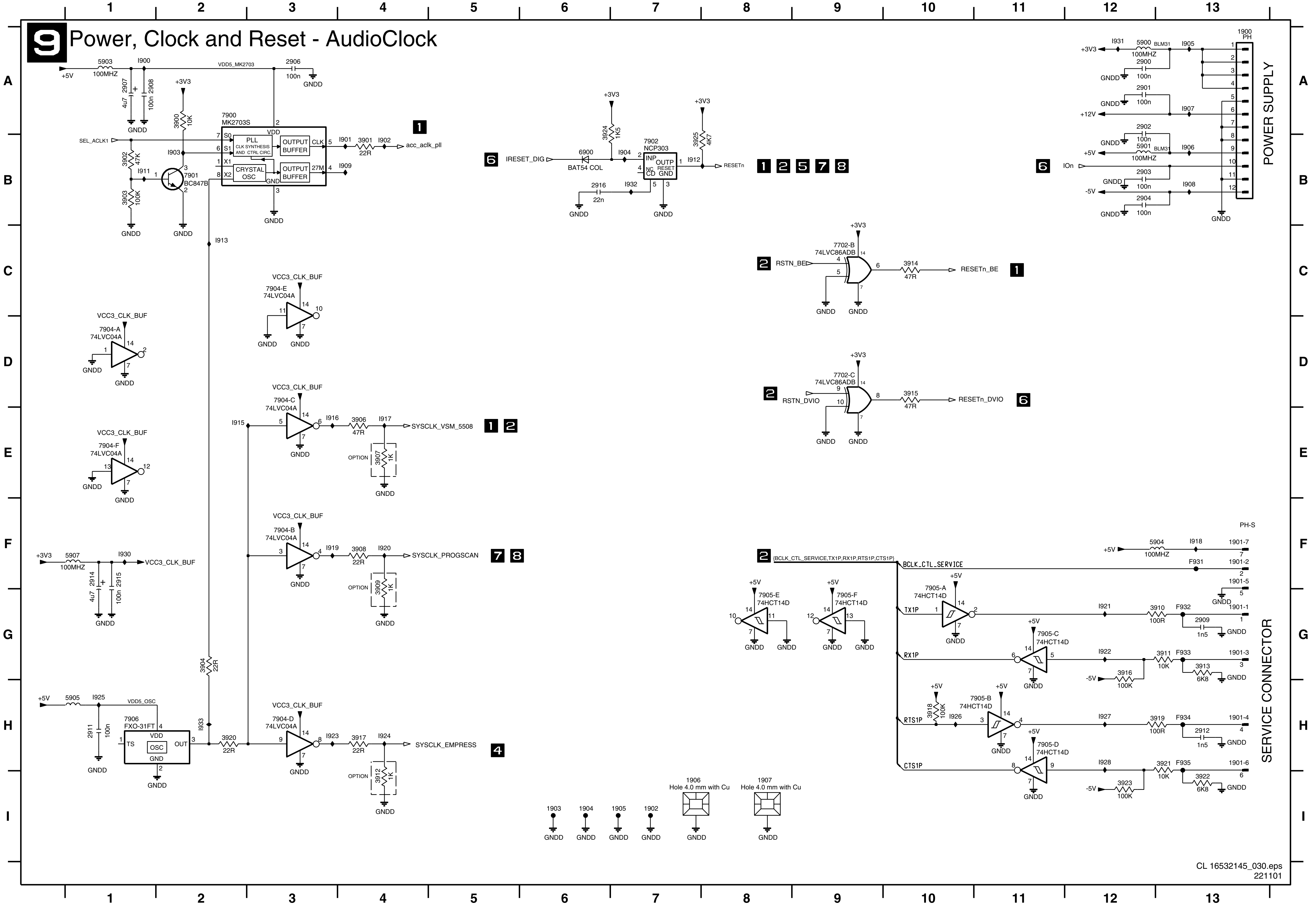
2700	B9
2701	B8
2702	B9
2703	B9
2704	B9
2705	B8
2706	B8
2707	G3
2708	B8
2709	B8
2710	B8
2711	B8
2712	B8
2713	B8
2714	F13
2715	B6
2716	B7
2717	B8
2718	B8
2719	B8
2720	B11
2721	E2
2722	E3
2723	B3
2724	B2
2725	B2
2726	B3
2727	B8
3700	G11
3701-A	F11
3701-B	F11
3701-C	F11
3701-D	F11
3702-A	G11
3702-B	F11
3702-C	F11
3702-D	F11
3703-A	F6
3703-B	F6
3703-C	F6
3703-D	F6
3704-A	F6
3704-B	F6
3704-C	F6
3704-D	F6
3705	G11
3706	G11
3707	H11
3708	H11
3709-A	E6
3709-B	E6
3709-C	F6
3709-D	F6
3710-A	G6
3710-B	G6
3710-C	E6
3710-D	E6
3711-A	G6
3711-B	G6
3711-C	G6
3711-D	G6
3712	F3
3713-A	G6
3713-B	G6
3713-C	G6
3713-D	G6
3714	G11
3715-A	H7
3715-B	H7
3715-C	H7
3715-D	H7
3716-A	H8
3716-B	H8
3716-C	H8
3716-D	H7
3717-A	H8
3717-B	H8
3717-C	H8
3717-D	H8
3718-A	H8
3718-B	H8
3718-C	H8
3718-D	H8
3719-A	H9
3719-B	H8
3719-C	H8
3719-D	H8
3720	F6
4700	A1
4701	B1
4702	E2
5700	B11
5701	A3
5702	B6
7700	B7
7701-A	E1
7701-B	C1
7702-A	E3
7702-D	C3
7703	A2

Digital Board: Progressive Scan

1800	D15	2806	B3	2812	B3	2818	C7	2824	C14	2832	E12	3800	G4	3806	B8	3812	D14	3818	E14	3824	F14	5801	B12	5807	E12	7802	B14
2800	B14	2807	B3	2813	B3	2819	C8	2826	D11	2833	E12	3801	C14	3807	C14	3813	D13	3819	E14	3825	F14	5802	B12	5808	E12	7803-A	D14
2802	B2	2808	B2	2814	C11	2820	C9	2827	D12	2834	F14	3802	B8	3808	C14	3814	D13	3820	E10	3826	F11	5803	D12	5809	F12	7803-B	E14
2803	B2	2809	B3	2815	C12	2821	C14	2828	D12	2835	F10	3803	C13	3809	D10	3815	E10	3821	E13	3827	F11	5804	D12	5810	B8		
2804	B2	2810	B3	2816	C12	2822	C9	2829	D14	2836	G10	3804	C13	3810	D6	3816	D14	3822	E13	3828	G4	5805	D12	7800	B1		
2805	B2	2811	B3	2817	F12	2823	C9	2831	E11	2837	B8	3805	C8	3811	D11	3817	E11	3823	F11	5800	B12	5806	E12	7801	C6		

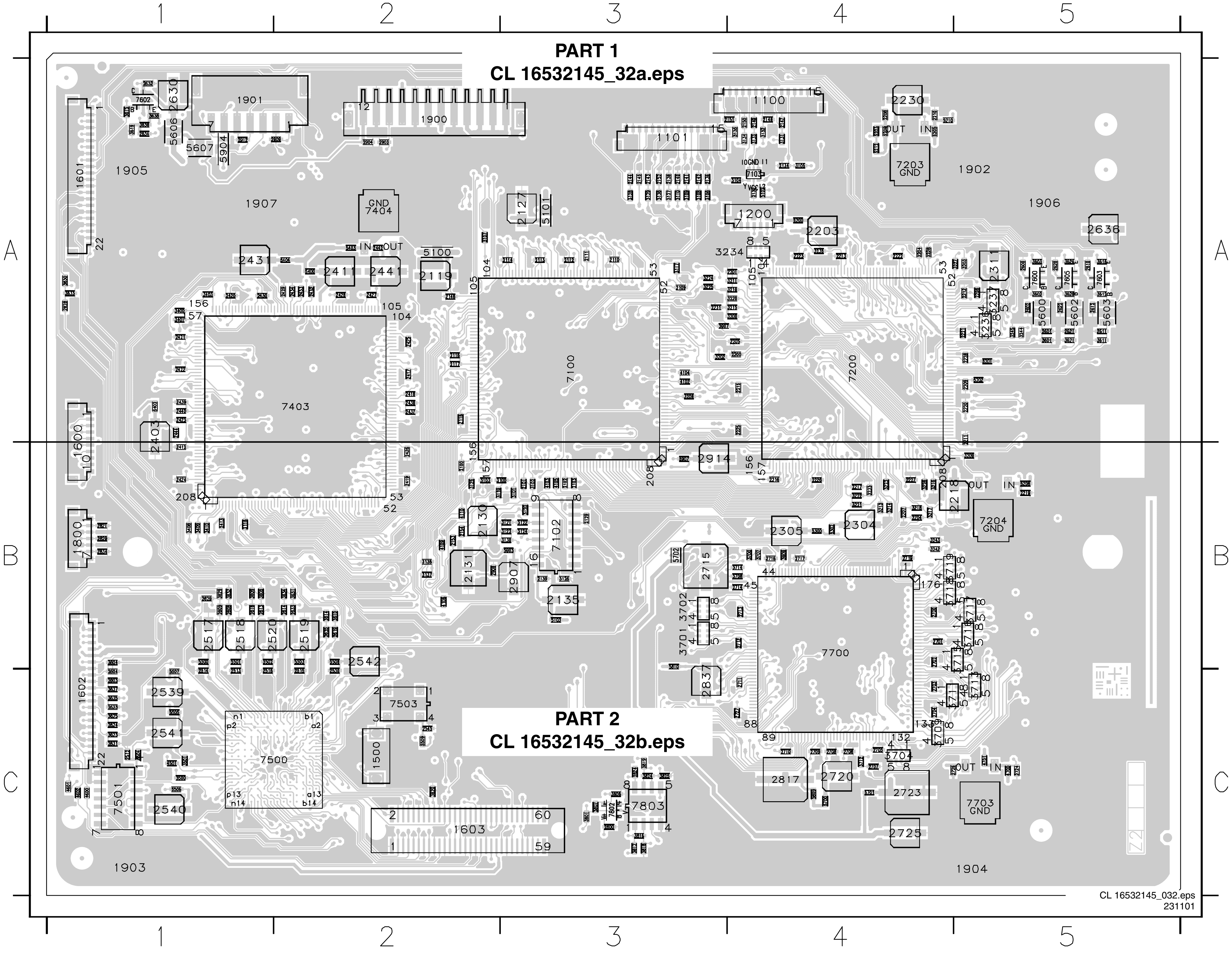

8 Progressive Scan
SDRAM
7800 MT48LC2M32B2TG
DENC
7801 ADV7196A
CONTROL BUS
ADDRESS BUS
DATA BUS
I2C BUS
+3V3_FLI
RESETn
HSOUT
VSOUT
SYSCLK_PROGSCAN
Yy_OUT(9:0)
Cr_OUT(9:0)
Cb_OUT(9:0)
TIMING GENERATOR
I2C MPU PORT
SYNC GEN
SHARPNESS FILTER CTRL & ADAPTIVE FILTER CTRL
CGMS MACRO-VISION
TEST-PATTERN GENERATOR & DELAY & GAMMA CORRECTION
LUMA 99 AF
CHROMA 4:2:2 TO 4:4:4 (99AF)
2X INTER-POLATION
11-BIT SYNC DAC
11-BIT DAC
DAC CTRL BLOCK
DAC-A/Y
DAC-B
DAC-C
VREF
RSET
COMP
7802 AD8061
7803-A AD8062
7803-B AD8062
+5V
+3V3
+3V3_DD
+3V3_ANA
GNDD
OPTION
1800 FMN
ANALOG BOARD
A B C D E F G H
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
CL 16532145_029.eps
221101

Digital Board: Power, Clock, and Reset Audio Clock


9
Power, Clock and Reset - AudioClock
+5V
5903
100MHZ
I900
VDD5_MK2703
2906
100n
GNDD
2907
4u7
2908
100n
+3V3
3900
10K
7900
MK2703S
SEL_ACLK1
3902
47K
I903
PLL
CLK SYNTHESIS AND CTRL CIRC
OUTPUT BUFFER
CRYSTAL OSC
7901
BC847B
I911
3903
100K
I901
3901
22R
I902
acc_aclk_pll
I909
I913
+3V3
3924
1K5
3925
4K7
7902
NCP303
IRESET_DIG
6900
BAT54 COL
I904
I912
RESETn
2916
22n
I932
1 2 5 7 8
6
7702-B
74LVC86ADB
RSTN_BE
3914
47R
RESETn_BE
7702-C
74LVC86ADB
RSTN_DVIO
3915
47R
RESETn_DVIO
VCC3_CLK_BUF
7904-E
74LVC04A
7904-A
74LVC04A
7904-C
74LVC04A
I915
I916
3906
47R
I917
SYSCLK_VSM_5508
OPTION
3907
1K
7904-F
74LVC04A
7904-B
74LVC04A
I919
3908
22R
I920
SYSCLK_PROGSCAN
3909
1K
+3V3
5907
100MHZ
I930
VCC3_CLK_BUF
2914
4u7
2915
100n
3904
22R
I933
+5V
5905
I925
VDD5_OSC
7906
FXO-31FT
OSC
2911
100n
3920
22R
7904-D
74LVC04A
I923
3917
22R
I924
SYSCLK_EMPRESS
3912
1K
4
1900
PH
+3V3
I931
5900
100MHZ
BLM31
I905
2900
100n
2901
100n
+12V
I907
2902
100n
5901
100MHZ
I906
2903
100n
IOn
-5V
I908
2904
100n
POWER SUPPLY
PH-S
5904
100MHZ
I918
1901-7
F931
1901-2
1901-5
(BCLK_CTL_SERVICE,TX1P,RX1P,RTS1P,CTS1P)
BCLK_CTL_SERVICE
7905-A
74HCT14D
TX1P
I921
3910
100R
F932
2909
1n5
1901-1
7905-C
74HCT14D
RX1P
I922
3911
10K
F933
1901-3
3916
100K
3913
6K8
7905-B
74HCT14D
RTS1P
3918
100K
I926
I927
3919
100R
F934
2912
1n5
1901-4
7905-D
74HCT14D
CTS1P
I928
3921
10K
F935
1901-6
3923
100K
3922
6K8
7905-E
74HCT14D
7905-F
74HCT14D
SERVICE CONNECTOR
1906
Hole 4.0 mm with Cu
1907
Hole 4.0 mm with Cu
1903
1904
1905
1902
CL 16532145_030.eps
221101
1 2 3 4 5 6 7 8 9 10 11 12 13
A B C D E F G H I

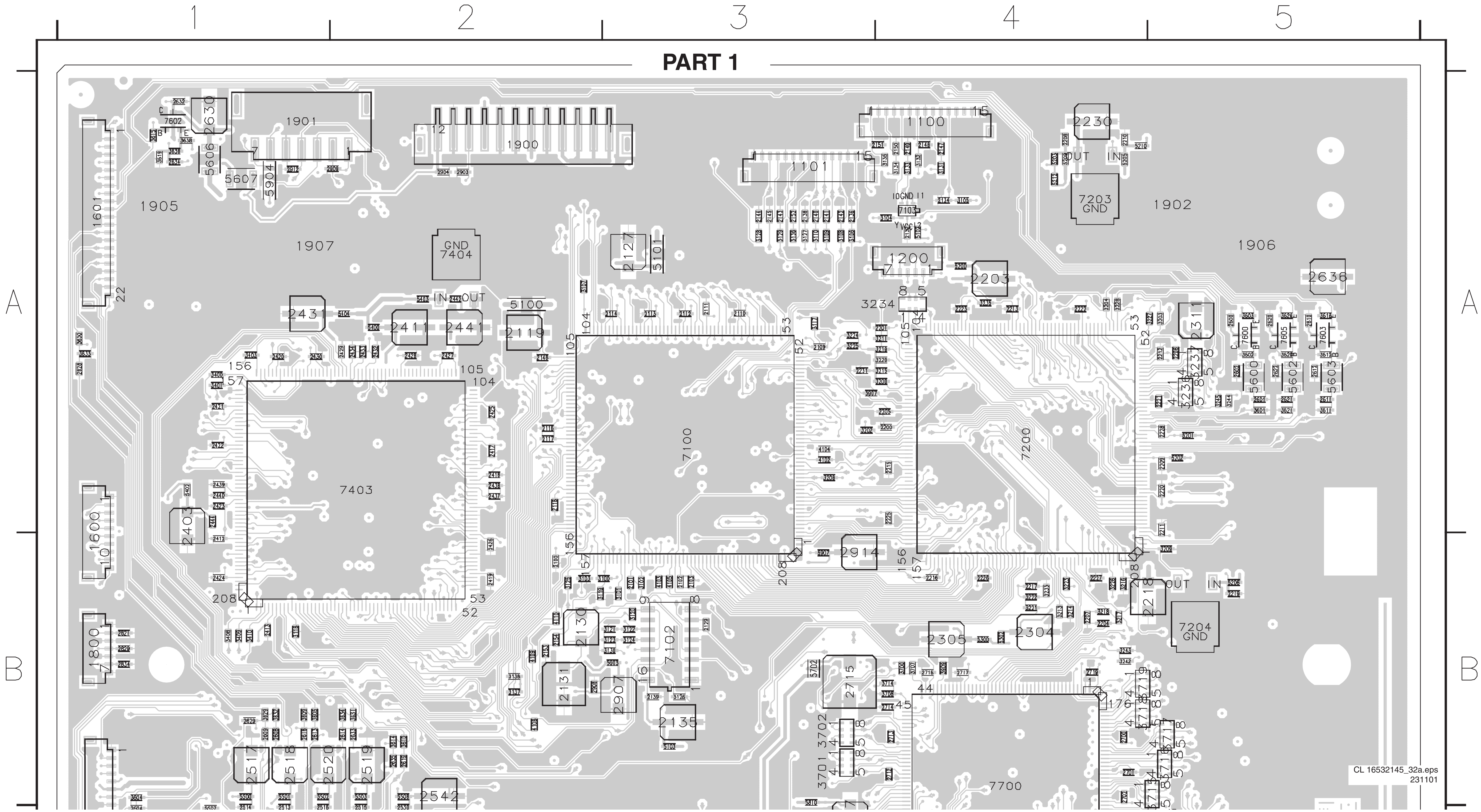
1900	A13
1901-1	G13
1901-2	F13
1901-3	G13
1901-4	H13
1901-5	F13
1901-6	H13
1901-7	F13
1902	I7
1903	I6
1904	I6
1905	I7
1906	I7
1907	I8
2900	A12
2901	A12
2902	A12
2903	B12
2904	B12
2906	A3
2907	A1
2908	A1
2909	G13
2911	H1
2912	H13
2914	F1
2915	F1
2916	B6
3900	A2
3901	B4
3902	B1
3903	B1
3904	G2
3906	E4
3907	E4
3908	F4
3909	F4
3910	G13
3911	G13
3912	I4
3913	G13
3914	C10
3915	D10
3916	G12
3917	H4
3918	H10
3919	H13
3920	H2
3921	H13
3922	I13
3923	I12
3924	A6
3925	B7
5900	A12
5901	B12
5903	A1
5904	F13
5905	H1
5907	F1
6900	B6
7702-B	C9
7702-C	D9
7900	A2
7901	B2
7902	B7
7904-A	D1
7904-B	F3
7904-C	D3
7904-D	H3
7904-E	C3
7904-F	E1
7905-A	G10
7905-B	H10
7905-C	G11
7905-D	H11
7905-E	G8
7905-F	G9
7906	H1
F931	F13
F932	G13
F933	G13
F934	H13
F935	H13

Layout Digital Board (Overview Top View)



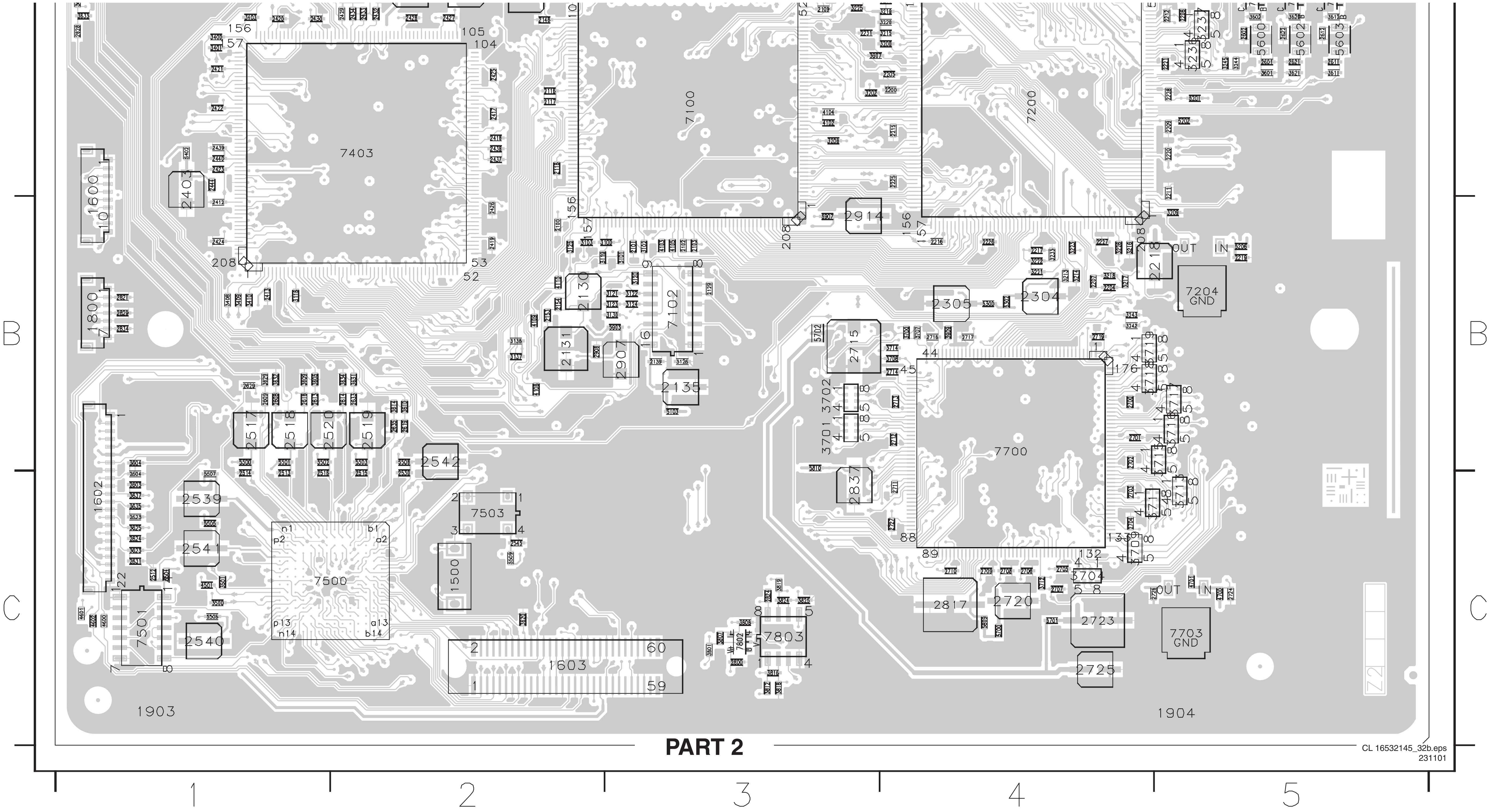
1100	A4	2311	A5	2707	C4	3221	B4	3909	B4
1101	A3	2403	A1	2708	C4	3222	B4	4102	A3
1200	A4	2411	A2	2709	C4	3223	B4	4103	B3
1500	C2	2412	B1	2710	C4	3224	A3	4104	A3
1600	A1	2413	B1	2711	C4	3225	A3	4105	B3
1601	A1	2417	A2	2712	B4	3226	B4	4108	B2
1602	C1	2418	A2	2713	B4	3227	A5	4109	B2
1603	C2	2419	B2	2714	B4	3228	A4	4110	B2
1800	B1	2420	A1	2715	B3	3233	B4	4501	C1
1900	A2	2421	A1	2716	B4	3234	A4	4600	C1
1901	A1	2422	A1	2717	B4	3235	A4	4601	C1
2100	B2	2423	A1	2719	B4	3236	A5	4602	C1
2101	B3	2424	B1	2720	C4	3237	A5	4700	C5
2102	B3	2425	A2	2723	C4	3242	B4	4701	C5
2103	B3	2426	B2	2724	C5	3243	B4	5100	A2
2109	A3	2427	A2	2725	C4	3244	A5	5101	A3
2110	A3	2428	A2	2726	C4	3245	A5	5102	A4
2111	A3	2429	A2	2727	C4	3400	A1	5103	B3
2112	A3	2430	A1	2800	C3	3401	A1	5200	A4
2113	A3	2431	A1	2817	C4	3403	A1	5201	A5
2114	A3	2432	A2	2821	B1	3408	B1	5202	A5
2116	A2	2433	A2	2824	C3	3409	B1	5203	A4
2117	A2	2434	A2	2829	B1	3410	B1	5205	A4
2118	A2	2437	A2	2834	B1	3500	C1	5206	B5
2119	A2	2438	A2	2837	C3	3501	C1	5209	A4
2127	A3	2439	A1	2903	A2	3601	A5	5210	A4
2129	B3	2440	A1	2904	A2	3602	A5	5212	A4
2130	B2	2441	A2	2907	B3	3603	A5	5300	B4
2131	B2	2442	A2	2908	B2	3604	B1	5302	B4
2132	A4	2444	A1	2909	A2	3605	B1	5400	A2
2134	A4	2512	C1	2912	A1	3609	B1	5402	A1
2135	B3	2513	C1	2914	B3	3610	B2	5403	A2
2136	A3	2514	C1	3100	B3	3611	A5	5404	A2
2138	A3	2515	C2	3101	B3	3612	A5	5500	B1
2139	B3	2516	C1	3102	B3	3613	A5	5501	B1
2140	A3	2517	B1	3103	B2	3614	B2	5502	B1
2141	A3	2518	B1	3104	A4	3615	A1	5503	B2
2142	A3	2519	B2	3105	A4	3619	A1	5504	C1
2143	A3	2520	B1	3106	A3	3620	C2	5505	C1
2144	A3	2530	C2	3107	A2	3621	A5	5506	C1
2145	A3	2539	C1	3108	A3	3622	A5	5507	C1
2146	A2	2540	C1	3109	A3	3623	C1	5508	B2
2147	A4	2541	C1	3110	A3	3624	A5	5509	C2
2148	A4	2542	B2	3117	A3	3625	C1	5600	A5
2149	A4	2545	C2	3118	B1	3629	B1	5602	A5
2150	A4	2600	A5	3119	B2	3630	A1	5603	A5
2151	A4	2601	A5	3120	B3	3631	B2	5606	A1
2152	A3	2602	A5	3121	B3	3632	B1	5607	A1
2153	B2	2603	C1	3122	B3	3633	A1	5700	C4
2154	B2	2604	C1	3123	B3	3634	B2	5701	C4
2200	A4	2608	B1	3124	B3	3635	C1	5702	B3
2201	A4	2609	B1	3125	B2	3636	A1	5809	C4
2203	A4	2610	A5	3126	B3	3637	C1	5810	B3
2204	B4	2611	A5	3127	A3	3638	A1	5903	B3
2205	A4	2612	A5	3128	A3	3700	B4	5904	A1
2206	A5	2613	B1	3129	A3	3701	B3	5907	B3
2207	B4	2614	B2	3130	B3	3702	B3	7100	A3
2208	A4	2618	B1	3131	A4	3704	C4	7102	B3
2209	A5	2619	B2	3132	A4	3707	B4	7103	A4
2210	A4	2620	A5	3133	A4	3708	B4	7200	A4
2211	A5	2621	A5	3134	A4	3709	C4	7203	A4
2212	A5	2622	A5	3135	A4	3711	C4	7204	B5
2213	A4	2623	C1	3136	A3	3712	C4	7403	A2
2215	A4	2624	C1	3137	B2	3713	C5	7404	A2
2216	B4	2628	A1	3138	B2	3714	B4	7500	C2
2217	B4	2629	B1	3200	A4	3715	B5	7501	C1
2218	B5	2630	A1	3202	A3	3716	B5	7503	C2
2219	B5	2631	C1	3203	A5	3717	B5	7600	A5
2220	A5	2632	A1	3204	A4	3718	B4	7602	A1
2221	A5	2633	B2	3208	A3	3719	B4	7603	A5
2222	A4	2634	A1	3209	B5	3801	C3	7605	A5
2223	A4	2635	B2	3211	A4	3807	C3	7700	B4
2225	A4	2636	A5	3213	B4	3808	C3	7703	C5
2226	B4	2700	B4	3214	B4	3812	C3	7802	C3
2227	B4	2701	B4	3215	A4	3816	C3	7803	C3
2228	A5	2702	B4	3216	B4	3818	C3		
2230	A4	2703	C4	3217	B4	3819	C3		
2231	A3	2704	C4	3218	B4	3824	C3		
2304	B4	2705	C4	3219	A4	3825	C3		
2305	B4	2706	C4	3220	A4	3907	A3		

Layout Digital Board (Part 1 Top View)


1
2
3
4
5
A
B
PART 1
1901
1900
1100
1101
2230
7203
GND
1902
1905
1907
1906
1601
7404
GND
2127
5101
1200
2203
2636
2431
2411
2441
5100
2119
3234
2311
7403
7100
7200
1600
2403
2914
2218
7204
GND
1800
2130
7102
2131
2907
2135
2305
2304
2715
7700
2517
2518
2520
2519
2542
5606
5607
5904
2630
7602
7600
7605
7603
5600
5602
5603
3237
3236
3701
3702
3718
3719
3717
3714
IN
OUT
12
15
1
22
156
57
105
104
53
52
208
176
45
44

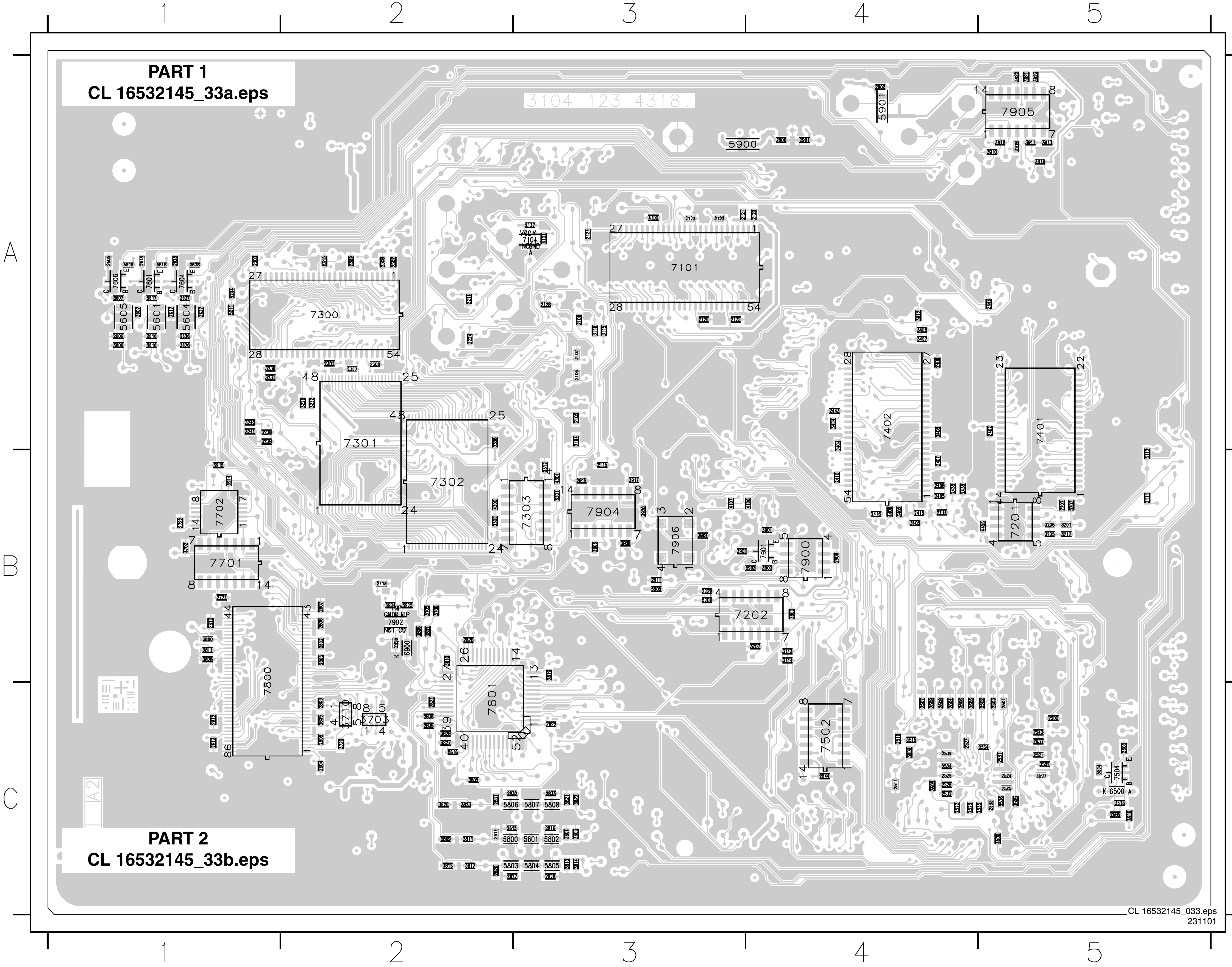
CL 16532145_32a.eps
231101

Layout Digital Board (Part 2 Top View)


7403
7100
7200
7102
7700
7500
7501
7503
7803
1600
1800
1602
1603
1500
2403
2130
2131
2907
2135
2914
2218
7204 GND
2305
2304
2715
2837
2517
2518
2520
2519
2542
2539
2541
2540
2817
2720
2723
2725
7703 GND
1903
1904
PART 2
B
C
1
2
3
4
5
OUT
IN

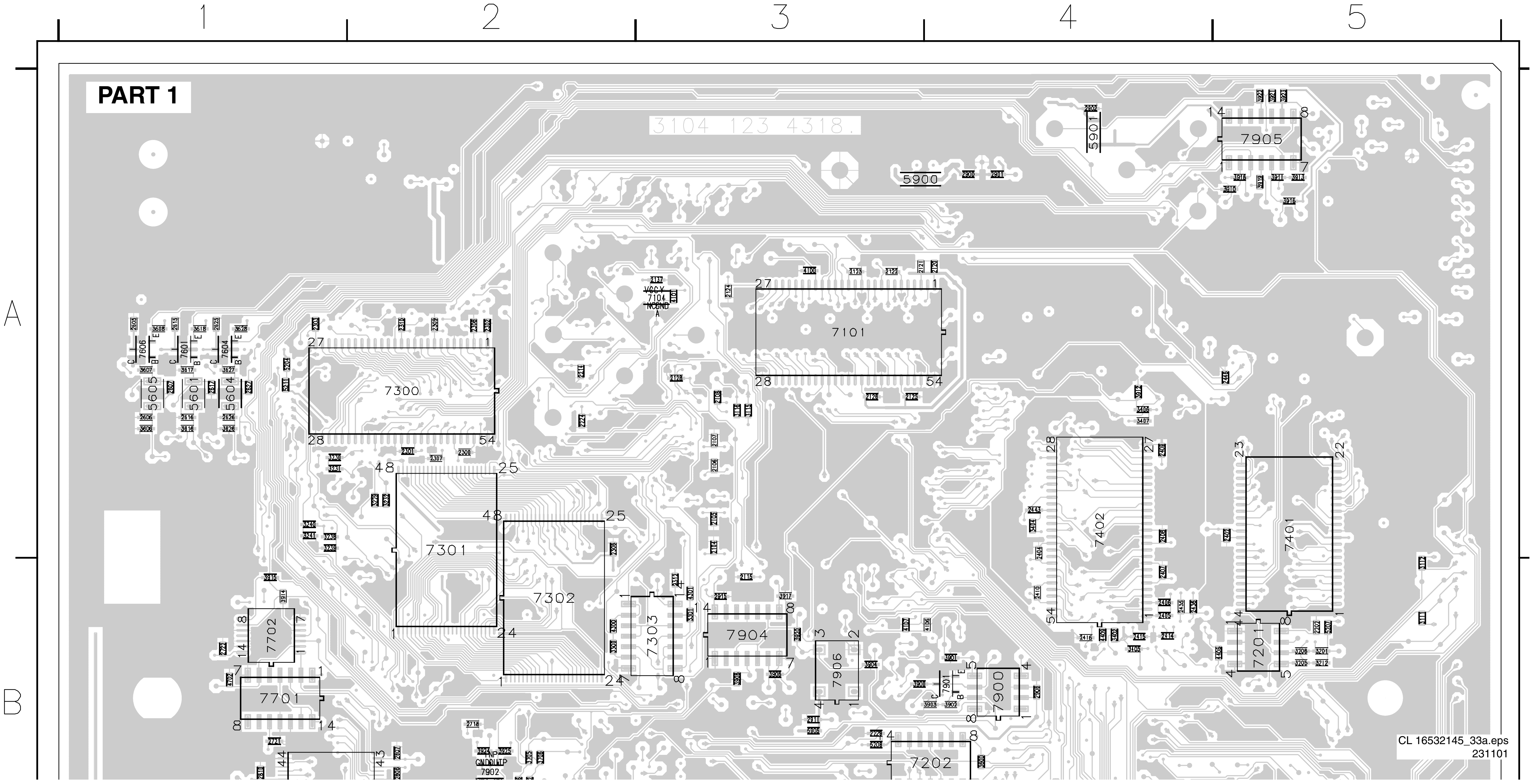
CL 16532145_32b.eps
231101

Layout Digital Board (Overview Bottom View)

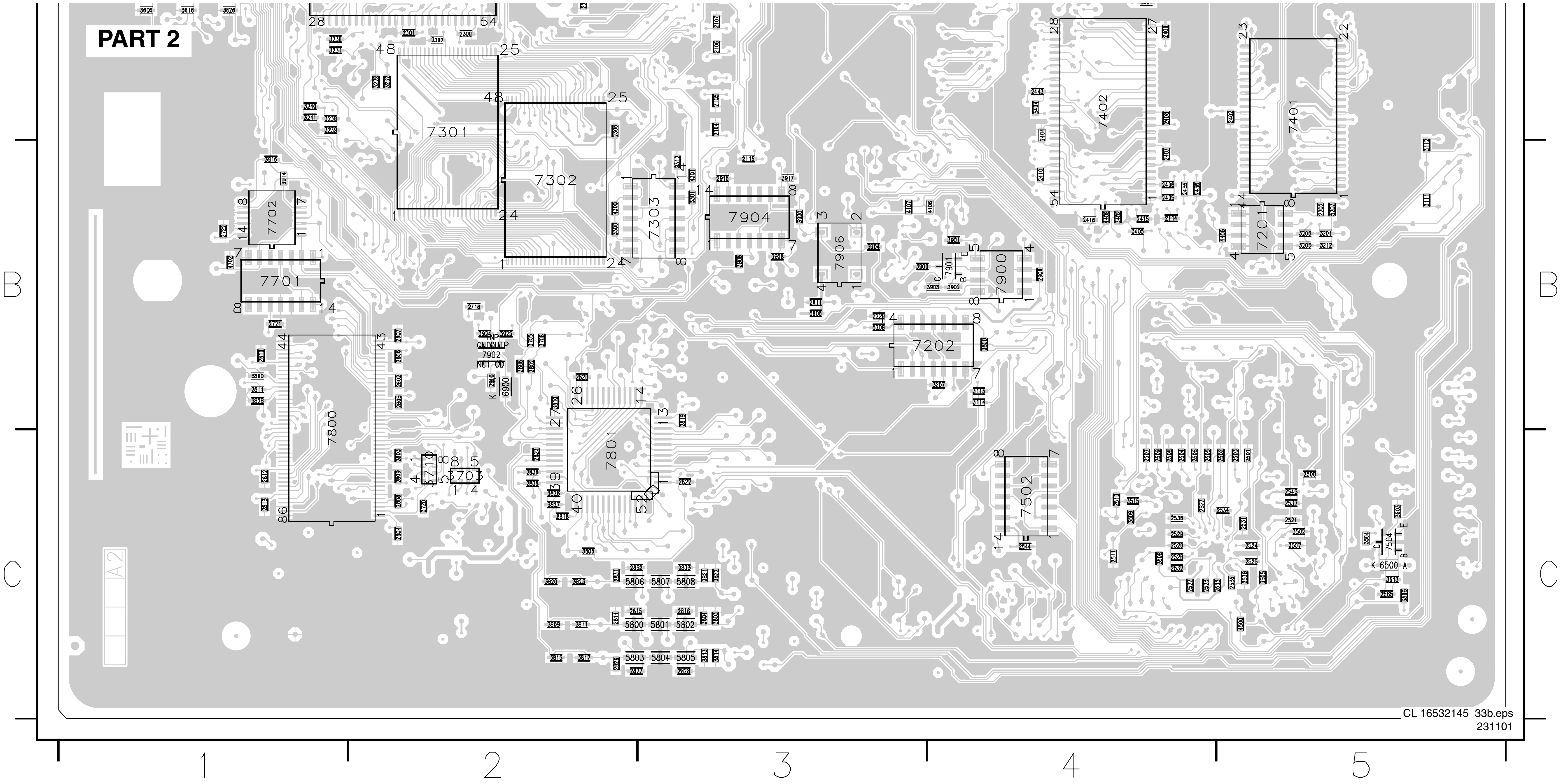

1
2
3
4
5
A
B
C
PART 1
CL 16532145_33a.eps
PART 2
CL 16532145_33b.eps
3104 123 4318.
7101
7300
7301
7302
7303
7402
7401
7201
7904
7905
7906
7900
7901
7202
7502
7702
7701
7800
7801
7902
5900
5901
5601
5604
5605
5703
5710
6500
6900
5800
5801
5802
5803
5804
5805
5806
5807
5808
A2
CL 16532145_033.eps
231101

2104	A3
2105	A3
2106	A3
2107	A3
2108	A3
2115	B3
2120	A4
2121	A3
2122	A3
2123	A3
2124	A3
2125	A3
2126	A3
2128	A3
2137	A3
2202	B5
2214	A2
2224	A2
2229	B3
2300	A2
2301	A2
2302	A2
2303	A1
2306	A2
2307	A2
2308	A2
2309	A2
2310	A2
2312	B3
2402	A5
2404	A4
2405	B4
2406	B4
2407	B4
2408	A4
2409	A4
2410	B4
2414	B4
2415	B4
2416	B4
2435	B4
2436	B4
2443	A4
2446	A5
2500	C5
2501	C5
2502	C5
2503	C5
2504	C4
2505	C4
2506	C4
2507	C4
2508	C4
2509	C4
2510	C4
2511	C4
2521	C5
2522	C4
2523	C4
2524	C5
2525	C5
2526	C4
2527	C4
2528	C4
2529	C4
2531	C5
2532	C4
2533	C5
2534	C5
2535	C5
2536	C5
2537	C5
2538	C4
2543	C5
2544	C4
2565	C5
2605	A1
2606	A1
2607	A1
2615	A1
2616	A1
2617	A1
2625	A1
2626	A1
2627	A1
2718	B2
2721	B1
2722	B1
2802	B2
2803	C2
2804	C2
2805	B2
2806	B2
2807	B2
2808	C2
2809	C2
2810	B1
2811	B1
2812	C1
2813	C1
2814	C2
2815	C2
2816	C3
2818	C2
2819	B3
2820	B2
2822	C3
2823	C2
2826	C2
2827	C2
2828	C3
2831	C2
2832	C2
2833	C3
2835	C2
2836	C2
2900	A4
2901	A4
2902	A4
2906	B4
2911	B3
2915	B3
2916	B2
3111	B5
3112	B5
3113	B4
3114	B4
3115	A3
3116	A3
3201	B5
3205	B5
3206	B5
3207	B4
3212	B5
3229	A2
3230	A1
3231	A1
3232	A2
3238	A1
3239	A1
3240	A1
3241	A1
3300	B2
3301	B3
3402	B4
3404	A4
3405	B4
3406	A4
3407	A4
3502	C5
3503	C5
3504	C5
3505	C5
3506	C5
3507	C5
3508	C4
3509	C4
3513	C5
3515	C4
3600	B4
3606	A1
3607	A1
3608	A1
3616	A1
3617	A1
3618	A1
3626	A1
3627	A1
3628	A1
3703	C2
3705	B2
3706	B2
3710	C2
3720	C2
3800	B1
3802	B2
3803	C3
3804	C3
3805	C2
3806	B2
3809	C2
3810	B2
3811	C2
3813	C3
3814	C3
3815	C2
3817	C2
3820	C2
3821	C3
3822	C3
3823	C2
3826	C2
3827	C2
3828	B1
3900	B3
3901	B4
3902	B4
3903	B4
3904	B3
3906	B3
3908	B3
3910	A5
3911	A5
3912	A4
3913	A5
3914	B1
3915	B1
3916	A5
3917	B3
3918	A5
3919	A5
3920	B3
3921	A5
3922	A5
3923	A5
3924	B2
3925	B2
4100	A3
4101	A3
4106	B4
4107	B3
4300	B2
4301	B3
4406	B5
4409	B4
4500	C5
4702	B1
5204	A1
5207	B5
5208	B3
5211	A1
5601	A1
5604	A1
5605	A1
5800	C2
5801	C3
5802	C3
5803	C2
5804	C3
5805	C3
5806	C2
5807	C3
5808	C3
5900	A3
5901	A4
5905	B3
6500	C5
6900	B2
7101	A3
7104	A3
7201	B5
7202	B4
7300	A2
7301	A2
7302	B2
7303	B3
7401	A5
7402	A4
7502	C4
7504	C5
7601	A1
7604	A1
7606	A1
7701	B1
7702	B1
7800	B1
7801	C2
7900	B4
7901	B4
7902	B2
7904	B3
7905	A5
7906	B3

Layout Digital Board (Part 1 Bottom View)

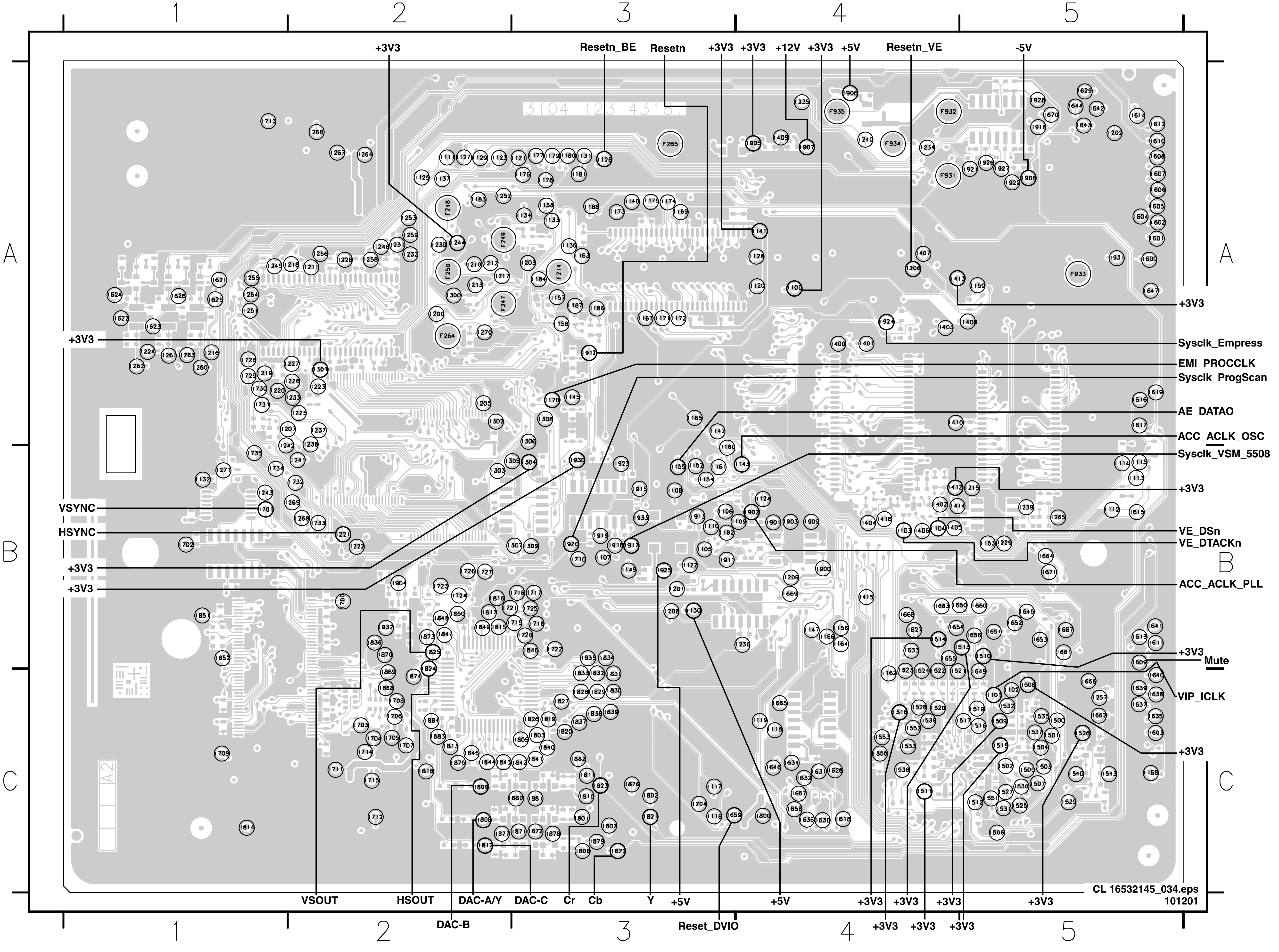

1
2
3
4
5
A
B
PART 1
3104 123 4318.
7300
7301
7302
7303
7101
7104
7402
7401
7201
7202
7701
7702
7900
7901
7902
7904
7905
7906
7601
7604
7606
5605
5601
5604
5900
5901
CL 16532145_33a.eps
231101

Layout Digital Board (Part 2 Bottom View)


PART 2
7301
7302
7303
7904
7906
7900
7901
7402
7401
7201
7202
7702
7701
7800
7801
7710
7703
7902
6900
7502
7504
6500
5806
5807
5808
5800
5801
5802
5803
5804
5805
A2
B
C
1
2
3
4
5

CL 16532145_33b.eps
231101

Layout Digital Board (Testlands Bottom View)


1
2
3
4
5
A
B
C
3104 123 4318.
+3V3
Resetn_BE
Resetn
+3V3
+3V3
+12V
+3V3
+5V
Resetn_VE
-5V
+3V3
Sysclk_Empress
EMI_PROCCLK
Sysclk_ProgScan
AE_DATAO
ACC_ACLK_OSC
Sysclk_VSM_5508
+3V3
VE_DSn
VE_DTACKn
ACC_ACLK_PLL
+3V3
Mute
VIP_ICLK
+3V3
+3V3
VSYNC
HSYNC
+3V3
+3V3
VSOUT
HSOUT
DAC-A/Y
DAC-C
Cr
Cb
Y
+5V
+5V
+3V3
+3V3
+3V3
+3V3
DAC-B
Reset_DVIO
+3V3
+3V3
+3V3
CL 16532145_034.eps
101201

Layout Digital Board (Mapping Testlands)

F214	A3	I175	A3	I300	A2	I610	A5	I720	B3	I880	C3
F247	A2	I176	A3	I301	A2	I611	B5	I721	B2	I881	C3
F248	A2	I177	A3	I302	A2	I612	A5	I722	B3	I882	C3
F249	A2	I178	A3	I303	B2	I613	B5	I723	B2	I883	C2
F250	A2	I179	A3	I304	B3	I614	A5	I724	B2	I884	C2
F264	A2	I180	A3	I305	B3	I615	B5	I725	B3	I900	B4
F265	A3	I181	A3	I306	A3	I616	A5	I726	B2	I901	B4
F931	A4	I182	B3	I307	B3	I617	A5	I727	B2	I902	B4
F932	A4	I183	A2	I308	A3	I618	C4	I728	A1	I903	B4
F933	A5	I184	A3	I309	B3	I619	A5	I729	A1	I904	B2
F934	A4	I186	A3	I400	A4	I621	A1	I730	A1	I905	A4
F935	A4	I187	A3	I401	A4	I622	A1	I731	A1	I906	A4
I100	A4	I188	A3	I402	B4	I623	A1	I732	B2	I907	A4
I101	C5	I200	A2	I403	A4	I624	A1	I733	B2	I908	A5
I102	C5	I201	B3	I404	B4	I625	A1	I734	B1	I909	B4
I103	B4	I202	A5	I405	B4	I626	A1	I735	B1	I911	B3
I104	B4	I203	A3	I406	B4	I627	B4	I800	C4	I912	A3
I105	B3	I204	C3	I407	A4	I628	C4	I801	C3	I913	B3
I106	B3	I205	A2	I408	A5	I629	A5	I802	C3	I915	B3
I107	B3	I206	A4	I409	A4	I630	C4	I803	C3	I916	B3
I108	B3	I207	A2	I410	A4	I631	C4	I805	C3	I917	B3
I109	B4	I208	B3	I412	B4	I632	C4	I806	C3	I918	A5
I110	B3	I209	B4	I413	A4	I633	B4	I807	C3	I919	B3
I111	A2	I210	A2	I414	B4	I634	C4	I808	C2	I920	B3
I112	B5	I211	A2	I415	B4	I635	C5	I809	C2	I921	A5
I113	B5	I212	A2	I416	B4	I636	C4	I810	C3	I922	A5
I114	B5	I213	A2	I500	C5	I637	C5	I811	C3	I923	B3
I115	B5	I215	B5	I501	C5	I638	C5	I812	C2	I924	A4
I116	C3	I216	A1	I502	C5	I639	C5	I813	C2	I925	B3
I117	C3	I217	A2	I503	C5	I640	C5	I814	C1	I926	A5
I118	C4	I218	A2	I504	C5	I641	B5	I815	B2	I927	A5
I119	C4	I219	A1	I505	C5	I642	A5	I816	B2	I928	A5
I120	A4	I220	A1	I506	C5	I643	A5	I817	B2	I930	B3
I121	A3	I221	B2	I507	C5	I644	A5	I818	C2	I931	A5
I122	B3	I222	B2	I508	C5	I645	B5	I819	C3	I932	B2
I123	A2	I223	A2	I509	C5	I646	C4	I820	C3	I933	B3
I124	B4	I224	A1	I510	B5	I647	A5	I821	C3		
I125	A2	I225	A2	I511	C4	I649	C5	I822	C3		
I126	A3	I226	A2	I512	C5	I650	B4	I823	C3		
I127	A2	I227	A2	I513	B5	I651	B5	I824	B2		
I128	A4	I228	A2	I514	B4	I652	B5	I825	B2		
I129	A2	I229	B5	I515	C5	I653	B5	I826	C3		
I130	B3	I230	A2	I516	C5	I654	B4	I827	C3		
I131	A3	I231	A2	I517	C5	I655	B4	I828	C3		
I132	B1	I232	A2	I518	C4	I656	B5	I829	C3		
I133	A3	I233	A2	I519	C5	I657	C4	I830	C3		
I134	A3	I234	A4	I520	C4	I658	C4	I831	C3		
I136	A3	I235	A4	I521	C4	I659	C3	I832	C3		
I137	A2	I236	B4	I522	C4	I660	B5	I833	C3		
I138	A3	I237	A2	I523	C4	I661	B5	I834	B3		
I140	A3	I238	A2	I524	C4	I662	C5	I835	B3		
I141	A4	I239	B5	I525	C5	I663	B4	I836	B2		
I142	A3	I240	A4	I526	C5	I664	B5	I837	C3		
I143	B4	I241	B2	I527	C5	I665	C4	I838	C3		
I145	A3	I242	B1	I528	C4	I666	C5	I839	C3		
I147	B4	I243	B1	I529	C5	I667	B5	I840	C3		
I149	B3	I244	A2	I530	C5	I668	B4	I841	C3		
I152	B3	I245	A1	I531	C5	I669	B4	I842	C3		
I153	B5	I246	A2	I532	C5	I670	A5	I843	C2		
I154	B3	I251	A1	I533	C4	I671	B5	I844	C2		
I155	B3	I252	A2	I535	C5	I700	B2	I845	C2		
I156	A3	I253	A2	I536	C4	I701	B1	I846	B3		
I157	A3	I254	A1	I537	C5	I702	B1	I847	B2		
I158	B4	I255	A1	I538	C4	I703	C2	I848	B2		
I159	A5	I256	A2	I540	C5	I704	C2	I849	B2		
I160	B3	I257	C5	I543	C5	I705	C2	I850	B2		
I161	B3	I258	A2	I551	C5	I706	C2	I851	B1		
I162	C4	I259	A2	I552	C4	I707	C2	I852	B1		
I163	A3	I260	A1	I553	C4	I708	C2	I868	C2		
I164	B4	I261	A1	I555	C4	I709	C1	I869	C2		
I165	A3	I262	A1	I600	A5	I710	B3	I870	B2		
I166	B4	I263	A1	I601	A5	I711	C2	I871	C3		
I167	A3	I264	A2	I602	A5	I712	C2	I872	C3		
I168	C5	I265	B5	I603	C5	I713	A1	I873	B2		
I169	A3	I266	A2	I604	A5	I714	C2	I874	C2		
I170	A3	I267	A2	I605	A5	I715	C2	I875	C2		
I171	A3	I268	B2	I606	A5	I716	B3	I876	C3		
I172	A3	I269	B2	I607	A5	I717	B3	I877	C2		
I173	A3	I270	A2	I608	A5	I718	B3	I878	C3		
I174	A3	I271	B1	I609	B5	I719	B3	I879	C3		

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101201

Personal Notes:

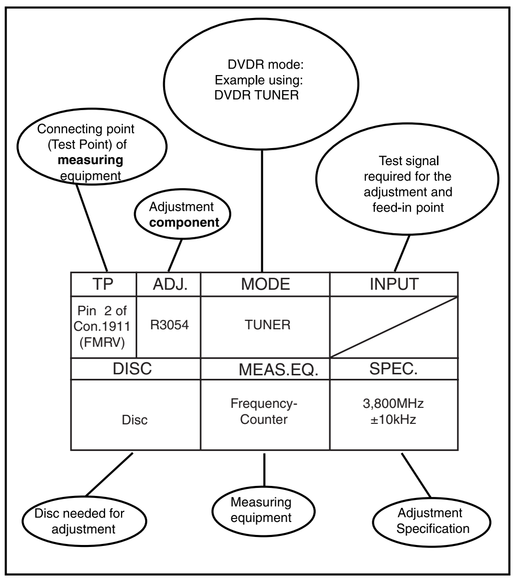
8. Alignments

8.1 Alignment Instructions Analogue Board

Test equipment:

1. Dual-trace oscilloscope
   Voltage range : 0.001 ~ 50 V/div
   Frequency : DC ~ 50 MHz
   Probe : 10:1, 1:1
2. DVM (Digital voltmeter)
3. Frequency counter
4. Sinus generator
   Sinus : 0 ~ 50 MHz
5. Test pattern generator

How to read the adjustment procedures:


DVDR mode:
Example using:
DVDR TUNER
Connecting point (Test Point) of **measuring** equipment
Adjustment **component**
Test signal required for the adjustment and feed-in point
TP
ADJ.
MODE
INPUT
Pin 2 of Con.1911 (FMRV)
R3054
TUNER
DISC
MEAS.EQ.
SPEC.
Disc
Frequency-Counter
3,800MHz ±10kHz
Disc needed for adjustment
Measuring equipment
Adjustment Specification

Front End (FV)

Service tasks after replacement of IC 7710, coil L5710 and L5711:

1 AFC Adjustment:

Purpose: Correct adjustment of demodulator AFC - circuit
Symptom, if incorrectly set:
Bad or disturbed TV channel reception.

PAL - AFC adjustment [5711]:

TP	ADJ.	MODE	INPUT
IC 7710 Pin 17 (F708)	L5711	TUNER	38,9MHz 500mV$_{pp}$ at Tuner 1705, Pin 11 (F710, IF-out)
DISC		MEAS.EQ.	SPEC.
		DC Voltmeter Frequ. Generator	2,5V ±0,1V

Storage in NVRAM via command mode interface of DSW:
After adjustment, the AFC reference value has to be stored in the NVRAM.
This reference value is 256 * measured voltage/Ucc. Ucc is 5.0V.
Store the reference value via command 732 , followed by the ref. value.
Example: DD:> 732 128

2 HF - AGC adjustment [3724]:

Service tasks after replacement of IC 7710:

Purpose: Set amplifier control.

Symptom, if incorrectly set:
Picture jitter if input level is too low and picture distortion if input level is too high.

TP	ADJ.	MODE	INPUT
Tuner 1705 Pin 11 (F710, IF-out)	R3707	Set tuned to channel 25 503.25 MHz	5mV(74dBµV) on aerial input PAL white picture, audio IF on, no modulation
DISC		MEAS.EQ.	SPEC.
		Oscilloscope Video Pattern Generator	500mV$_{pp}$ +/-0.5dB (use a 10:1 probe)

3 Attenuating the 40.4 MHz [5710]: (SECAM only)

Service tasks after replacement of coil 5710:

Purpose: To attenuate the band I carrier rests.

Symptom, if incorrectly set:
Bad picture quality when the filter attenuates the picture carrier (38.9MHz).

TP	ADJ.	MODE	INPUT
OFW 1701 Pin 1 (F709)	L5710	TUNER	40.4 MHz, 200mV$_{rms}$ at Tuner 1705, Pin 11 (F710, IF-out)
DISC		MEAS.EQ.	SPEC.
		Oscilloscope, Sinus Generator, Counter	adjust minimum amplitude

If the adjustment is correct the signal at pin 1 of OFW [1701] must be smaller than the input signal amplitude by at least 6 dB.

Figure 8-1

8.2 Reprogramming Procedure of NVM on the Microprocessor Sub PCB

The NVM, item 7808, on the Microprocessor Sub board contains the following factory settings:

1. Clock correction factor
2. AFC reference value
3. Slash version

The settings 1,2 and 3 are stored in the NVM during the production of the analogue board.
The slash version is stored at the end of the production line of the set.
In case of failure, the NVM must be replaced by an empty device. By way of commands via the Diagnostic Software or via ComPair, the factory settings must be restored in the NVM.

8.2.1 Clock Correction Adjustment

To guarantee an exact function of the real time clock, an adjustment of the clock frequency is possibe. The adjustment value is stored in the NVM.
Procedure:

- put the set in service command mode
- execute command 722 to initiate that a signal with 32768 Hz is available on pin 3 of connector 1988
  DD:>722
- measure the frequency f_{meas} of the Clock Crystal with an accuracy of ± 0.1 Hz.
- Calculate the parameter to be entered: $32768/f_{meas} * 10^6$
- Normally the parameter must be between 999902 and 1000097. If the parameter and therefore the frequency of the crystal is outside this range, the crystal must be replaced.
- Execute command 721 with the parameter as input
  example:
  DD:>721 1000023

8.2.2 AFC Reference Voltage Tuner

This function stores the reference voltage for the tuner in the NVM. Before this value can be stored, the AFC adjustment, described in the adjustment instructions of the analogue board, must be carried out.
Procedure:

- Adjust AFC circuit
- Calculate the reference value
- Execute command 732 and use the calculated reference value as parameter
  example:
  DD:>732 128

8.2.3 Slash Version

The slash version is stored with command 715 followed by the slash version as parameter.
The slash versions used in DVDR880 and DVDR890 are the following:

- DVDR880/00X: 63
- DVDR880/02X: 63
- DVDR880/05X: 64
- DVDR890/00X: 61
- DVDR890/02X: 61
- DVDR890/05X: 62
- DVDR890/69X: 81
- DVDR890/17X: 61

Example:
DD:>715 63

Reset of Slash Version
Use command 729 to reset the analogue board to the default setting.
Procedure:

- Put the set in DSW command mode
- Execute command 729 with the following parameters:
  DD:> 729 w 0xA0 3 0x07 0xD0 0x00
- Leave the DSW command mode and start up the set in application mode
  No background is visible on the TV screen. The analogue board is ready to accept the appropriate slash version

8.3 Rework Procedure IEEE Unique Number

8.3.1 Scope:

The procedure describes how to upgrade sets with a unique number after repair. This unique number is stored in the NVRAM (item 7201) of the digital board at the end of the production line.
This procedure is only valid or necessary when:

- The digital board is replaced
- NVRAM on the digital board is replaced
- NVRAM is cleared

In all other cases the repaired set retains its unique number.
The procedure defines several means to re-assure the unique number depending on the possibilities of repair or the state the faulty set is in.

8.3.2 Handling:

State of original (defective) board:

1. The digital board starts up in Diagnostics Mode: follow procedure A to retrieve the valid unique number
2. The digital board does NOT start up in Diagnostics Mode: follow procedure B.

8.3.3 Procedure A

1. Connect defective digital board to PC via serial cable (3122 785 90017)
2. start up hyper terminal or any other serial terminal via the correct settings (DSW command mode interface)
3. read out existing unique number via nucleus 403
   example:
   ```
   DD:> 403
   40300: DV Unique ID = 00D7A1FC6C
   Test OK @
   ```
4. note read out
5. program new digital board via nucleus 410
   example:
   ```
   DD:> 410 00D7A1FC6C
   41000:
   Test OK @
   ```

The set has now the original unique number

8.3.4 Procedure B

1. Note the serial number of the set
   example:
   VN050136130156
   - VN = production centre (VN....Szekesfehervar). According to UAW-500: V=22 and N=14
   - 05 = change code (this is not used for this calculation)
   - 01 = YEAR
   - 36 = Production WEEK
   - 130156 = Lot and SERIAL number
2. Calculate the unique number: this number always exists out of 10 hexadecimal numbers.
3. First 5 numbers:
   First we calculate a decimal number according to the formula below:
   35828*YEAR* + **676*** *WEEK* + **26***V + N + **8788**
   The figures are fixed, *YEAR* + *WEEK* + *factory code (V + N) are variable*
   Example:
   35828*01*+**676***36*+**26***22+14+**8788** = 69538 (decimal)
   Then we translate the decimal number to a hexadecimal number.
   example:
   69538 (decimal) = 10FA2 (hex)
4. Last 5 numbers:
   The last 5 numbers exist out of the Lot and SERIAL number.
   We have to translate the decimal number to the next 5 hexadecimal numbers:
   Example:
   130156 (decimal) = 1FC6C (hex)
5. Program new digital board via nucleus 410
   Therefore we use the 10 hexadecimal numbers we calculated above:
   example:
   DD:> 410 10D7A1FC6C
   41000:
   Test OK @

The set has now its original unique number

9. Circuit-, IC Descriptions and List of Abbreviations

9.1 Display Board

9.1.1 Microcontroller

The core element of the Display Control unit is the microcontroller TMP87CH74AF [7110]. The TMP87CH74AF is an 8 bit microcontroller fitted with 32kB ROM and 1kB RAM. It requires 5V supply and is responsible for the following functions:

- Interface to Central Controller-µP
- Evaluation of the keyboard matrix
- Decoding the remote control commands from the infra-red receiver
- Activation and control of the local display
- Heater voltage generation

The 8 MHz resonator (Pos. 1111) generates the system clock. The reset is generated by the CC-µP via “POR_DC”-signal where the transistor [7106] is used as a level-shifter from 3V3 to 5V.

9.1.2 Interface to the Central Control µP

The communication to the main microcontroller (CC) on the µP-Sub-PCB is done via I^{2}C-Interface, where the TMP87CH74AF acts in slave-mode.
An additional wire (“INT”-line) is used to signal the Central controller that data are ready, e.g. when a key has been pressed.

9.1.3 Evaluation of the Keyboard Matrix

There are 10 different keys on the display board. A resistor network is used to generate a specific direct voltage value, depending on the pressed key. Via the resistors 3168 and 3169 on the analog/digital (A/D) ports (7110 pin 37 and 38) the evaluation is done.

9.1.4 IR Receiver and Signal Evaluation

The IR receiver [7150] contains a selectively controlled amplifier as well as a photo-diode. The photo-diode changes the received infra red transmission (approx. 940nm) to electrical pulses, which are then amplified and demodulated. On the output of the IR receiver [7150], a pulse sequence with TTL-level, which corresponds to the envelope curve of the received IR remote control command, can be measured. This pulse sequence is fed into the controller for further processing via port TC1 [7110, pin20].

9.1.5 Vacuum Fluorescence Display

The VFD “10-BT-242GNK” [POS 7100] is fully controlled by the microcontroller. The µC also includes the driving stages. Only two additional drivers [POS 7101 and 7102] are necessary for the grids 8 and 10 because of their large size.

9.1.6 VFD Heater Voltage Generator

The circuit around POS [7103, 7104 and 7105] is used to generate a proper AC-Voltage for the filament of the VFD. For this the microcontroller generates an appropriate rectangular signal with 50% duty-cycle and a frequency of 30 kHz at pin 19. Pos. [5193] and [2102] are acting as a resonance-circuit. Via Zener-Diode (POS[6100]) and resistors [3100, 3103 and 3104] the two heater-pins of the VFD (“FIL1” and “FIL2”) are clamped so that the grids and segments can be fully switched off.

9.1.7 REC-LED

The REC-LED is a red LED, located on a small PCB together with the REC-Switch and controlled via pin 3 of the microcontroller. The POS [7180] is used as a driver for the led.

9.2 Microcontroller Sub Board (UPC12 SUB PCB)

9.2.1 General

This small PCB is directly soldered in on top of the Analogue-Board.
It is used with no diversity in all three different basic versions (Europe, NAFTA and APAC-Pal). Only the software being loaded into the external Flash-memory is not the same.

9.2.2 Microcontroller

The main part of the Sub-PCB is the central controller (CC) µP [7804] TMP91CW12AF, which is a 16-bit CPU with 128kBROM and 4kB RAM.
It works with a 3V3 supply and a system clock of 24,576MHz [1801].
The 3V3-supply is made out of the “5VSTBY” by the circuit around [7816].
After connecting the set to the mains (power-up) the IC [7806] generates a reset pulse. This signal (“IPOR”) is directly fed to first priority interrupt input (pin 63) for power fail detection and also to the Reset-Input of the CC (Pin30) via [7802], which is necessary to generate a reset only during power-up. In case of power fail pin 30 of the CC must be kept high (3V3).
The internal memory of the CC is too small for all necessary demands. Therefore an external Flash-ROM [7805] with 1MByte in size and a RAM [7803] with 128kByte are necessary. Both parts are connected to the µP via a parallel address-/data-bus. The lower eight bus-lines (AD0 to AD7) are multiplexed by [7801] and the “ALE”-signal of the CC.
For updating of the software the external Flash-ROM can be reprogrammed by the µP. During this process [7807] is switched on by the “WE”-signal.
When no mains is connected, the CC is supplied via Gold-Cap [2816] during the power backup period. The diode [6802] prevents unwanted current consumption of other components.
The internal ROM of the µP holds the program code for the Real-Time-Clock. Only the microprocessor is supplied by the backup cell, not the external memories and the µP operates in a low frequency mode with the clock crystal [1805] only (32.768 kHz). To adjust the clock the frequency can be measured at pin 87 of the µP in a special test-mode.

9.2.3 Control-Interfaces

The CC is communicating with the digital board via a serial connection, which operates at a speed of 19,4 kbit/s (“D_DATA”-, “A_DATA”, “D_RDY”- and “A_RDY”-signal on [1986]). By generating a high level on pin 16 of the CC the digital PCB can be reset (inverter [7817] in between).
Most of the other parts are controlled by the µP via I^{2}C-bus (“SDA”- and “SCL”-signal). The FETs [7821] and [7822] are used for adaptation of the 3V3-level on CC-side to the components supplied with 5V.
The CC can also reset the display-board-µP by pulling pin 39 to high.
The transistor [7819] acts as a level shifter for the “INT”-signal.
In the European sets a bi-directional interface is established between the recording unit and the TV device at pin 10 of the Scart (“P50”-line/Easy Link). The processing is done via pin 14 (output) and pin 38 (input) of the CC and the circuit around [7813], [7814] and [7815].

9.2.4 EEPROM

The EEPROM M24C16 [7808] is an electrical erasable and programmable, non-volatile memory. The EEPROM stores data specific to the device, such as the AFC-reference value of the Europe IF-part, the clock-correction-factor, etc. It is accessed by the µP via the I^2C-bus.

9.2.5 Sync Separator

TTo detect whether a video signal is available or not a separate IC [7825] is used to extract the sync information out of the video signal that is also routed to the digital board for recording.
While on the input a low-pass-filter ([2823] and [3869]) limits the bandwidth an additional filter (circuit
around [7818]) on the output avoids distortions. Afterwards the sync-signal is routed to pin11 of the CC.

9.2.6 Fan Control

To avoid unwanted temperatures inside the set (especially the Laser on the OPU of the drive is very sensitive) a fan is located on top of the basic engine. The speed control is dependent on the ambient temp. A NTC resistor [3172] located on the display board measures the temperature. An operational amplifier [7902-B] generates a proper voltage, which is then fed to the engine ("BE_FAN"-line). Below 28°C ambient temp. the fan-voltage is approx. 5V and is increased to 10V when the ambient temperature goes up to approx. 35°C. The second part of the Op-Amp. [7902-A] prevents damage of any temperature-sensitive part in case the NTC or the wire in between is damaged. It acts as a comparator and pulls the "BE_FAN"-signal to 10V. As the fan has to be stopped in case the tray of the drive is open this voltage is "killed" by the CC ("FAN_OFF"-signal). The double-diode [6903] acts for both Op.-Amp.-circuits.

9.2.7 Power Supply

The 5SW and 8SW supply are switched off in case of standby from the P via the ISTBY-line. This is possible for power-save. The ISTBY-line must be low in case of STBY. There is also a „power fail" circuit on the PS-schematic which is necessary to mute AUDIO when IPFAIL is low.

9.3 Analog Board Europe

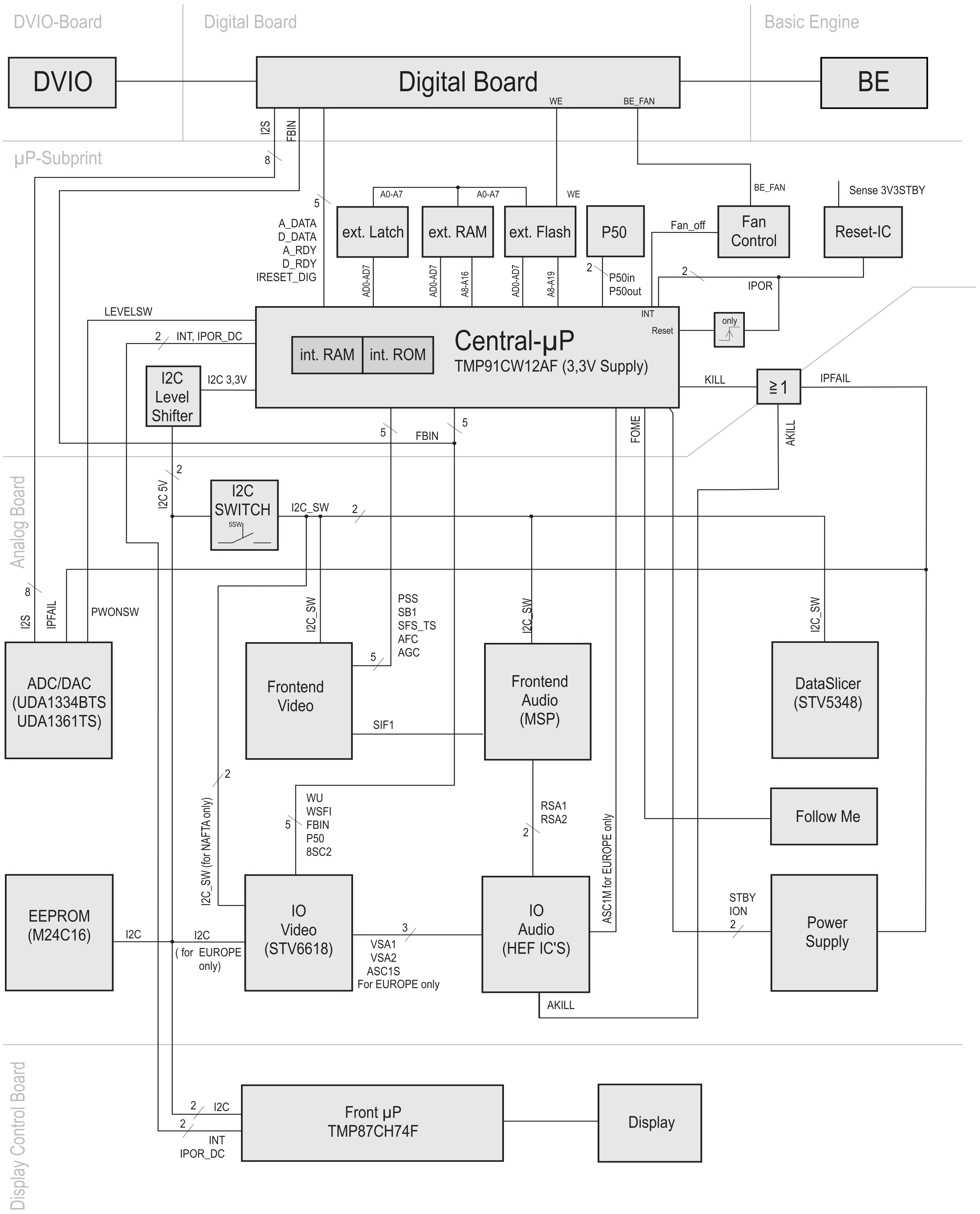
9.3.1 General

This PCB consists out of the following parts:
- Power-Supply-Unit
- Frontend (Audio & Video)
- Input/Output-switching
- Audio ADC- & DAC-processing
- VPS/PDC- and Text-Data slicer
- Analog Follow-Me Circuit

All functional groups are either controlled via I^2C-bus or via separate signal lines by the Central-Controller on the µP-Sub-Board. This sub board is directly soldered in onto the analog PCB. During Stand-By mode of the set, several parts are not supplied (Tuner, MSP, …). The microprocessor is running and maintains the clock of the set.

To avoid bus blockades the I^2C-bus ("SCLSW" & "SDASW") to/from these units is decoupled via transistors [7419], [7420] from the general bus ("SCL" & "SDA").

Blockdiagram Control Lines and Bus Systems


DVIO-Board
Digital Board
Basic Engine
DVIO
Digital Board
BE
WE
BE_FAN
I2S
FBIN
µP-Subprint
8
5
A0-A7
A0-A7
WE
BE_FAN
Sense 3V3STBY
A_DATA
D_DATA
A_RDY
D_RDY
IRESET_DIG
ext. Latch
ext. RAM
ext. Flash
P50
Fan_off
Fan Control
Reset-IC
AD0-AD7
AD0-AD7
A8-A16
AD0-AD7
A8-A19
2
P50in
P50out
2
IPOR
LEVELSW
INT
Reset
only
2
INT, IPOR_DC
int. RAM
int. ROM
Central-µP
TMP91CW12AF (3,3V Supply)
I2C Level Shifter
I2C 3,3V
KILL
≥1
IPFAIL
5
5
FBIN
FOME
AKILL
Analog Board
2
I2C 5V
I2C SWITCH
5SW
I2C_SW
2
8
I2S
IPFAIL
PWONSW
I2C_SW
PSS
SB1
SFS_TS
AFC
AGC
5
I2C_SW
I2C_SW
ADC/DAC (UDA1334BTS UDA1361TS)
Frontend Video
Frontend Audio (MSP)
DataSlicer (STV5348)
SIF1
2
WU
WSFI
FBIN
P50
8SC2
5
RSA1
RSA2
2
Follow Me
I2C_SW (for NAFTA only)
ASC1M for EUROPE only
STBY
ION
2
EEPROM (M24C16)
I2C
I2C
(for EUROPE only)
IO Video (STV6618)
3
VSA1
VSA2
ASC1S
For EUROPE only
IO Audio (HEF IC'S)
AKILL
Power Supply
Display Control Board
2
I2C
2
INT
IPOR_DC
Front µP TMP87CH74F
Display

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9.3.2 Power Supply Unit

Functional Principle:
This power supply works in the way of a flyback converter. In the mains input part [1931 to 2309], the mains voltage is rectified and buffered in the capacitor [2309]. From this direct voltage at [2309] energy is transferred into the transformer [5300, pins 7-5] during the conductive phase of the switching transistor [7307] and is stored there as magnetic energy. This energy is passed to the secondary outputs of the power supply in the blocking phase of the switching transistor [7307]. With the switch-on time of the switching transistor [7307], the energy transferred in every cycle is regulated in such a way that the output voltages remain constant regardless of changes in the load or mains voltage. The power transistor is driven by the integrated circuit [7313].

Mains input part:
The mains input part extends from the mains socket [1931] to the capacitor [2309]. The diodes [6301, 6302, 6305 and 6306] rectify the AC supply voltage, which is then buffered by the capacitor [2309]. The common mode coil [5302] and capacitor [2302] work as a filter to block interference arising in the power supply from the mains. Components [1302], [3306] protect the power supply against short-term over voltages in the mains, e.g. caused by indirect lightning.

Start-up with Mains-on:
After connecting the power cord to the mains, the capacitor [2325] is loaded via a current source between pin 8 and pin 1 in the IC [7313]. Once the voltage on [2325] and therefore the supply voltage V_{cc} of the IC [7313] has reached approx. 11V, the IC starts up and provides pulses at its output pin 5. These pulses are used to drive the gate of the power transistor [7307]. The frequency of these pulses is depending on load and mains voltage. The current consumption of the IC is approx. 5 mA at V_{cc} in normal mode.
If V_{cc} drops to below approx. 9V (e.g. with power limitation) or if V_{ac} exceeds approximately 16V (e.g. interruption of the control loop), the output of the IC [7313, pin 5] is blocked and a new start-up cycle begins. (See also “Overload, Power Limitation, Burst Mode“ section)

Normal operation:
With increasing load on one or more of the power supply outputs, the switch-on time for the power transistor [7307] increases, and thus also the peak value of the delta-shaped current through this power transistor. The equivalent voltage of this current profile is passed from resistors [3321] and [3352] via [3365] to pin 5 of the IC [7313]. If the voltage on pin 2 reaches approx. 0.4V in one switching cycle, the conductive phase of the switching transistor is ended immediately. The check is done in each individual switching cycle. This process ensures that no more than approx. 50W can be taken out from the mains (= **power limitation**).
If the power supply reaches the power limit, the output voltages and the supply voltage V_{cc} on pin 1 of the IC [7313] will be reduced following further loading. If V_{cc} is less than approx. 9V at any point during this process, the output of the IC [7313, pin 6] is blocked. All output voltages and V_{cc} decrease and a new start-up cycle begins. If the overload status or short-circuit remains, the power limitation will be activated immediately and the voltages will again decrease, followed by another start-up cycle (**Burst Mode**). The amount of power taken up from the mains in burst mode is low.

Overload, power limitation, burst mode
With the power supply in normal mode, the periodic sequences in the circuit are divided primarily into the conductive and blocking phase of the switching transistor [7307]. During the **conductive phase** of the switching transistor [7307], current flows from the rectified mains voltage at capacitor [2309] through the primary coil of the transformer [5300, pins 7-5], the transistor [7307] and resistors [3321, 3352] to ground. The positive voltage on pin 7 of the transformer [5300] can be assumed as constant for a switching cycle. The current in the primary coil of the transformer [5300] increases linearly. A magnetic field representing a certain value of the primary current is formed inside the transformer. In this phase, the voltages on the secondary coils are polarized such that the diodes [6300, 6303, 6307, 6308, 6310, 6313, 6317 and 6319] block. From the controller [7315] a current is supplied into the CTRL input on the IC [pin 3, 7313] via optocoupler [7314]. Once the switch on time of the switching transistor [7307] - that corresponds to the current supplied into the CTRL input - has been reached, the switching transistor [7307] is switched off.
When the switching transistor has been switched off, the **blocking phase** begins. No more energy will be transferred into the transformer. The inductivity of the transformer will still attempt to keep the current flowing at a constant level (U=L*di/dt). Switching off transistor [7307] interrupts the primary current circuit. The polarity of the voltages on the transformer is reversed, which means that the diodes [6300, 6303, 6307, 6308, 6310, 6313, 6317 and 6319] become conductive and current flows into the capacitors [2305, 2312, 2319, 2322, 2326 and 2328] and the load. This current is also ramp-shaped (di/dt negative, therefore decreasing).
The **feedback control** for the switched-mode power supply is done by changing the conductive phase of the switching transistor so that either more or less energy is transferred from the rectified mains voltage at [2309] into the transformer. The regulation information is provided by voltage reference [7315]. This element compares the 5V-output voltage via voltage divider [3332, 3333, 3334] with an internal 2.5V reference voltage. The output voltage of [7315] passes via an optocoupler [7314] for insulation of primary and secondary parts as a current value into pin 3 on the IC [7313]. The switch-on time of the transistor [7307] is inversely proportional to the value of this current.

Standby modes:
In the ‘AV-Standby‘ operating mode of the set, the ’ION‘ control line is primarily used to switch off all output voltages for Basic Engine and Digital Board (supplies 3V3, 5V, 12V, 5N and 4V6 at Connectors 1932 and 1933) of the power supply. This reduces the amount of power taken from the mains. In Low Power Standby mode additionally the ‘STBY’ control line is used to switch off output voltages 5SW and 8SW. This reduces power consumption to less than 3W. The power supply will continue operating in Standby mode with a switching frequency of approx. 25 kHz.

9.3.3 Frontend

This unit is designed to support two basic versions, which are distinguished by a different assembly variant only (one for multistandard and the second for Pal-I only) and comprises the following parts:
- Tuner UV1316K [1705]
- IF amplifier & video demodulator IC TDA 9818/9817 [7710]
- Sound processor MSP3415G [7600]

Tuner and IF selection
The Tuner [1705] converts the RF-signal coming from the antenna input to an IF-signal. The tuner is fully controlled via I²C-bus of the CC-µP. [1705] is also equipped with a “passive-loop-through” between antenna-in and –out to save power in stand-by of the set, when the complete part is not supplied. The IF frequency of the video carrier is 38.9 MHz for all systems except SECAM L' (34,0 MHz).
A quasi-split audio system is used. Separate surface-wave filters (SAW) are required. [1701], [1703] for video, [1702] for audio. [1701] is switched into the signal path for DK/I-SECAM L/L' reception, if the signal “SFS_TS” is “high”. In this case the switches [7704], [7705] are open and the diode [6703] is conducting. [1703] is switched into the signal path for BG reception (“SFS_TS” is “low”). Then the switch [7712] is open and the diode [6704] is conducting. For DK/I-SECAM L/L' recep-

tion, an additional circuit for suppressing the audio carrier of the adjacent channel is used. This circuitry is adjusted by coil [5710] for maximum suppression at 40.4MHz.

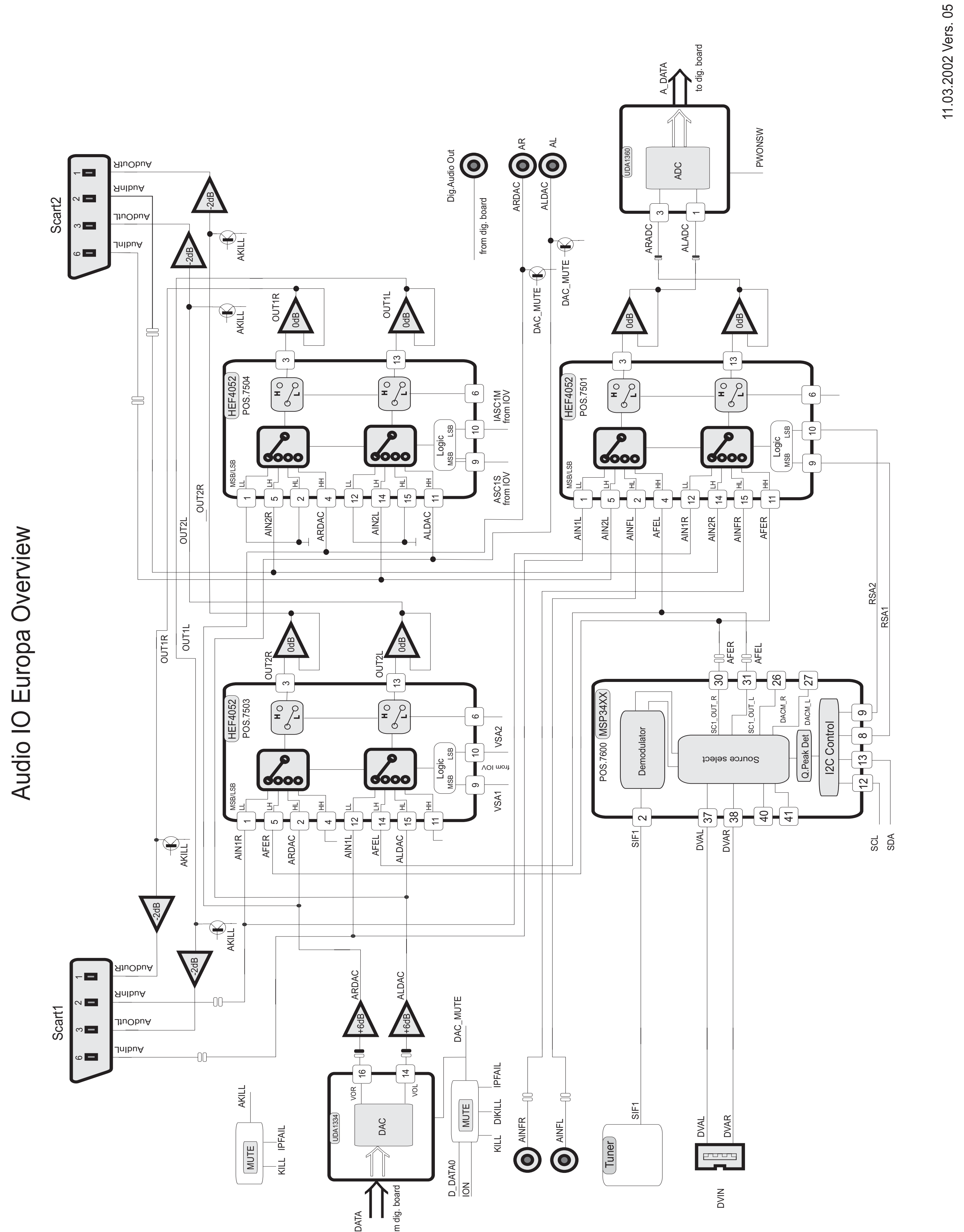
IF demodulator

The signal from the tuner and IF-selection circuit is processed by the demodulator IC TDA 9818/9817 [7710]. The signal "PSS" to pin 3 switches between demodulation of positive (SECAM only) or negative modulated video carriers. A QSS-audio-IF signal SIF1 is generated for demodulation in the sound processor [7600]. The audio-IF carrier is selected in the audio SAW filter [1702]. This filter is switched for SECAM L'. If the signal "SB1" is "high", the switch [7714] is closed and the diode [6705] is not conducting. For all other standards the diode [6705] is conducting and the switch [7714] is open. The output signal of this SAW filter is firstly processed in the TDA 9818. Audio carriers are converted from the tuner IF level to the audio IF position and further processed in the audio demodulator [7600]. The AFC coil [5711] on the TDA 9818/9817 is adjusted so that when a frequency of 38.90 MHz is supplied to the IF output of the tuner, the AFC voltage on pin 17 of [7710] is 2.5V. The setting of the picture carrier frequency for SECAM L in the TDA 9818 is achieved by connecting pin 7 of the IC via a resistor [3710] to ground. The switch [7701] and the signal "SB1" do this. The HF-AGC is set using the potentiometer [3724] so that, with a sufficiently large antenna input signal (74 $dB_{\mu V}$), the voltage at the IF output of the tuner [1705] pin 11 is 500 mV_{pp}. This setting must be carried out when the audio carrier is switched off. The demodulated video signal appears on pin 16 of [7710]. The AGC voltage at pin 4 is used to determine the antenna signal strength after a buffer [7717] with the signal "AGC" and an analog input port of the CC-µP. The trap [1704] reduces the sound carrier remainders in the video for BG standards. The trap [1706] works in the same way for the Pal-I standard only. For all other standards the switch [7713] is closed via [7706] and "SFS_TS"-line set "high" to bypass this trap. In these cases the selectivity of the SAW filter [1701] is sufficient. The coil [5713] for non-BG standards realizes a frequency response correction. This correction is not desired for SECAM L' and therefore short-circuited by [7716] (signal SB1 is "high" and [7702] has on-status). The demodulated video signal "VFV" is available after the buffer and limiting stage for noise peaks [7711]. The FM-PLL demodulator function of TDA 9818 is not necessary and therefore deactivated by the resistor [3739].

Audio demodulator

The sound demodulation is done by the MSP3415 [7600], which is also fully controlled via I²C-bus by the CC-µP (determination of bandwidth, amplitude, standard, …).The audio signals are available at pin 30 and pin 31 of [7600] and fed as "AFER"- & "AFEL"-line to the audio-I/O for further processing.

9.3.4 Audio routing


Audio IO Europa Overview
11.03.2002 Vers. 05
Scart2
Scart1
AudOutR
AudInR
AudOutL
AudInL
-2dB
AKILL
0dB
OUT1R
OUT1L
OUT2R
OUT2L
HEF4052
POS.7504
POS.7503
POS.7501
Logic
MSB
LSB
IASC1M from IOV
ASC1S from IOV
VSA2
VSA1
from IOV
AIN2R
ARDAC
AIN2L
ALDAC
AIN1R
AFER
AIN1L
AFEL
AINFL
AINFR
Dig.Audio Out
from dig. board
AR
AL
DAC_MUTE
UDA1360
ADC
ARADC
ALADC
A_DATA
to dig. board
PWONSW
RSA2
RSA1
POS.7600
MSP34XX
Demodulator
Source select
Q.Peak Det
I2C Control
SC1_OUT_R
SC1_OUT_L
DACM_R
DACM_L
SIF1
DVAL
DVAR
SCL
SDA
UDA1334
DAC
VOR
VOL
+6dB
D_DATA
MUTE
KILL
IPFAIL
DIKILL
D_DATA0
ION
Tuner
DVIN

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The processing of audio is always done in stereo (e.g. separate left- and right-channel) and the complete switching is realized by using HEF4052, which is a dual four-to-one multiplexer. In principle there are three independent selectors:

a) Scart 1-Output-Path:

Pos [7504] is used to select either Scart 2-Input (“AIN2L”/”AIN2R”) or the signal directly from the audio DAC [7001] (“ALDAC”/”ARDAC”) as the output source for Scart 1 (“AOUT1L”/”AOUT1R”).

The control is done by means of the lines “ASC1S” coming from [7408] (IC [7408] acts as a port expander for the CC-µP) and “IASC1M”, which is directly coming from the CC. Pos [7412] is used for level adaptation (3V3 to 5V) in between.

b) Scart 2-Output-Path:

Pos [7503] selects between Scart 1-Input (“AIN1L”/”AIN1R”), signals from the internal frontend (“AFEL”/”AFER”) via MSP [7600] or audio directly from the DAC [7001] (“ALDAC”/”ARDAC”). The outputs of this switch are routed to Scart 2 (“AOUT2L”/AOUT2R”). This switch is controlled via “VSA1”- and “VSA2”-line. These lines come from [7408] that is acting as a port expander for the CC-µP.

c) Record-Path:

Pos [7501] selects either signals from Scart 1 (“AIN1L”/”AIN1R”) or Scart 2 (“AIN2L”/”AIN2R”) or Cinch-Front (“AINFL”/”AINFR”) or the MSP [7600] (“AFEL”/”AFER”) and routes to the audio ADC [7005] (“ALADC”/”ARADC”) for record purposes. The switch is controlled via “RSA1”- and “RSA2”-signals. These signals come from the MSP [7600], which acts as a port expander of the CC-µP. As there can also exist a fifth input in case of DV-In is present the corresponding analog audio signals from the DVIO-board are firstly routed via extra cable and connector [1960] to the MSP. The MSP acts as a preselector between audio from internal frontend or the DV-Input.

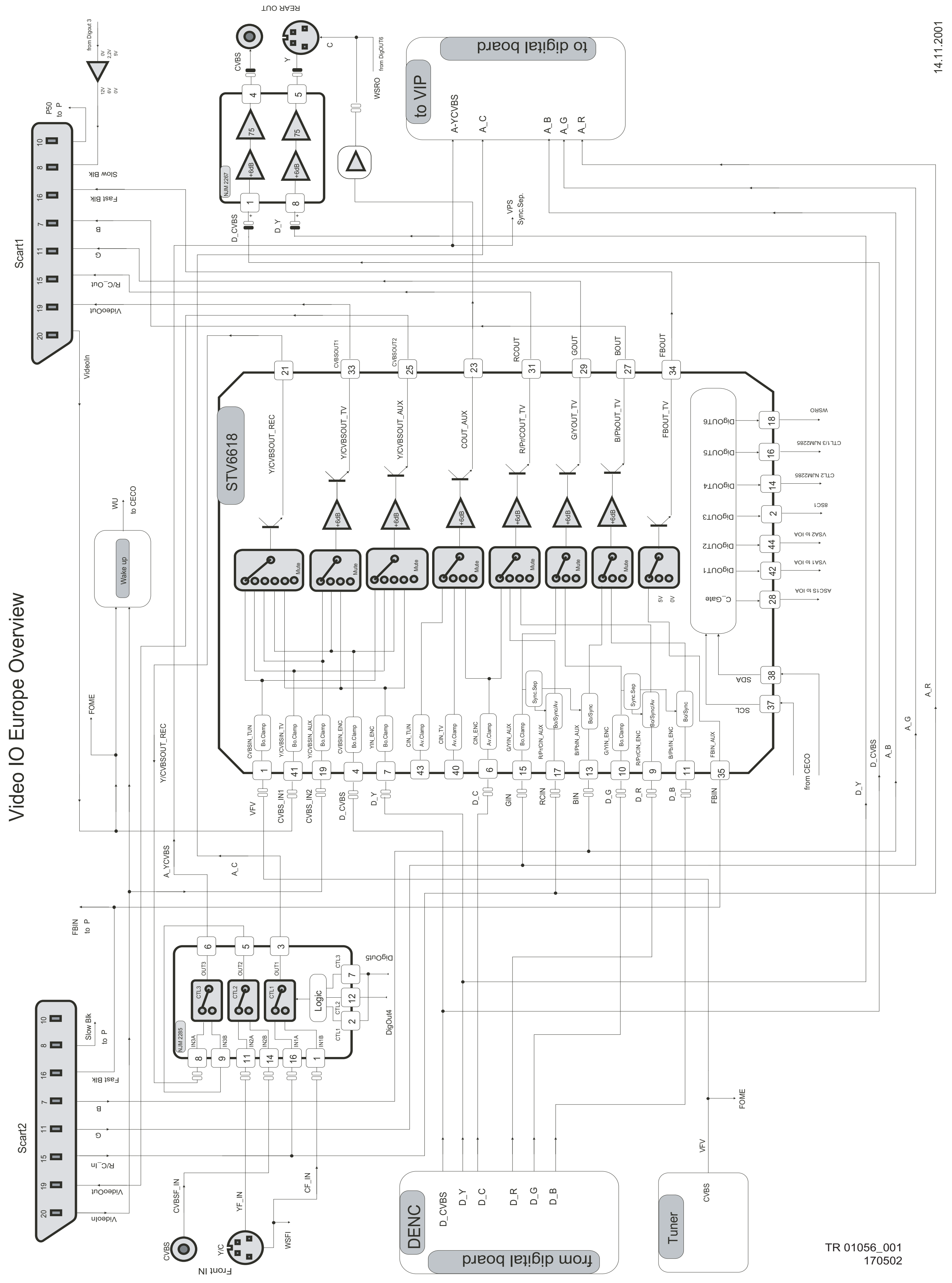
Each of these three selectors ([7501], [7503] & [7504]) has a separate Op-Amp on the output for level-adaptation-, performance- and line-driving-reasons. [7505-A & -B] for record, [7502-C & -D] for Scart 1-Output and [7502-A & -B] respectively for Scart 2. Every audio output line on the two Scart connectors can be “killed” (muted) by a extra transistors ([7506], [7508], [7509] &[7511]), which can be activated by the “AKILL”-line. This signal is generated by the circuit around [7404]/[7421] and is a combination of the “KILL”- from the CC-µP and the “IPFAIL” of the power-supply-unit.

Additionally to analog audio the set is also equipped with a digital output via cinch plug [1951]. The signal is generated on the dig. board and routed via audio interface cable and connector [1900] to the Ana-PCB. Here the “DAOUT”-line first passes a 6-fold inverter [7580] being used as a driver and for performance reasons (noise reduction, jitter, …). Afterwards a transformer [5580] is necessary to achieve the correct level and also to have a floating output with isolated ground before the signal is fed via [3580] to cinch plug [1951]. The capacitor [2580] performs an AC-coupling between connector- and set-ground.

9.3.5 Audio ADC/DAC

The conversion of analog audio signals from the record-selector [7501] in the I/O (“ALADC”- & “ARADC”) is done via UDA1361TS [7005]. This IC can process input signals up to $2V_{rms}$ by using external resistors [3039], [3041] in series to the input pins. As the level from the DVIO-Board is only $1V_{rms}$ a 6dB step can be performed by setting pin 7 of [7005] to 3,3V via [7006] and the “PWONSW”-line controlled by the CC-µP to use the whole dynamic range of the ADC. All required clock signals are generated on the dig. board and only the audio data (“A_DAT”-line) are routed from Ana- to Dig.-PCB for further processing.
The transformation of dig. audio back into the analog domain is done by UDA1334BTS [7001]. All necessary clock signals are coming from the dig. board and dig. audio data (“D_DATA0”-line) are converted into analog signals, which are available at pin 14 and pin 16 of [7001]. Afterwards an Op-Amp. [7002] (line driver & level adaptation) and a low-pass-filter to increase signal performance (noise, distortions,…). is passed. Then both signals (“ALDAC” & “ARDAC”) are directly routed to the rear cinch output and also used in the audio-I/O for further processing. The DAC has also a mute possibility, which can be activated by setting pin 8 to 3,3V via [7003]. This mute is controlled either by the dig. board (“D_IKLL”-line) or the “IPFAIL”-signal from power-supply-unit.
In addition to that the DAC [7001] and the cinch outputs can be killed (muted) in case of “digital silence” by the circuit around [7008],[7009] and [7010], when no audio data are available (e.g. “D_DATA0”-line zero).
This function can be also activated via the “ION”-line (set to high during any stand-by mode). To avoid signal distortions (clipping) the mute transistors for cinch rear out [7415], [7416] are decoupled via [7011].

9.3.6 Video-routing


Video IO Europe Overview
Scart1
Scart2
P50 to P
Slow Blk
Fast Blk
B
G
R/C_Out
VideoOut
VideoIn
R/C_In
Slow Blk to P
FBIN to P
from Digout 3
REAR OUT
CVBS
Y
C
WSRO
from DigOUT6
NJM 2267
+6dB
75
D_CVBS
D_Y
to VIP
to digital board
A-YCVBS
A_C
A_B
A_G
A_R
VPS
Sync.Sep.
WU
to CECO
Wake up
FOME
Y/CVBSOUT_REC
STV6618
Y/CVBSOUT_REC
Y/CVBSOUT_TV
Y/CVBSOUT_AUX
COUT_AUX
R/Pr/COUT_TV
G/YOUT_TV
B/PbOUT_TV
FBOUT_TV
CVBSOUT1
CVBSOUT2
RCOUT
GOUT
BOUT
FBOUT
Mute
DigOUT6
DigOUT5
DigOUT4
DigOUT3
DigOUT2
DigOUT1
C_Gate
WSRO
CTL1/3 NJM2285
CTL2 NJM2285
8SC1
VSA2 to IOA
VSA1 to IOA
ASC1S to IOA
SDA
SCL
from CECO
CVBSIN_TUN
Y/CVBSIN_TV
Y/CVBSIN_AUX
CVBSIN_ENC
YIN_ENC
CIN_TUN
CIN_TV
CIN_ENC
G/YIN_AUX
R/PrCIN_AUX
B/PbIN_AUX
G/YIN_ENC
R/PrCIN_ENC
B/PbIN_ENC
FBIN_AUX
Bo.Clamp
Av.Clamp
Sync.Sep
Bo/Sync/Av
Bo/Sync
VFV
CVBS_IN1
CVBS_IN2
D_CVBS
D_Y
D_C
GIN
RCIN
BIN
D_G
D_R
D_B
FBIN
A_YCVBS
A_C
NJM 2285
OUT1
OUT2
OUT3
CTL1
CTL2
CTL3
Logic
DigOut5
DigOut4
IN1A
IN1B
IN2A
IN2B
IN3A
IN3B
CVBSF_IN
YF_IN
CF_IN
WSFI
Front IN
Y/C
DENC
from digital board
Tuner
CVBS
FOME
VFV

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The complete Video-I/O-switching is basically realized by the matrix switch STV6618 [7408], which is controlled via I²C-bus by the CC. All used outputs excluding pin 21 (Y/CVBS-REC) have a 6 dB-amplification and a 75 Ohms driver-stage inside. This IC includes also several digital outputs, which are used for switching purposes on the analog board. The record selector inside the switch selects between the CVBS from frontend ("VFV"), the input from Scart 1 ("YCVBSIN1") or the signal from Scart 2 ("YCVBSIN2"). Afterwards the signal passes another switch [7411] in which a selection between signals from the front or the preselected ones are done. The output signals of [7411] are fed as "A_YCVBS"- and "A_C"-line to the digital board for further processing.

To reduce the number of external presets there exists only one preset for CVBS- and Y/C-front. The set automatically detects between the two inputs depending on the presence of a video signal (sync separator-circuit on mP-sub-board) where Y/C has higher priority.

The R/G/B-inputs and the Fast-Blanking-line from Scart 2 are directly routed to the digital PCB. These signals are also available on the corresponding input-pins of the STV6618 to enable a loop-through in AV-Standby. In this mode the set has to behave like a cable between the two Scart-connectors. AV-Standby is activated either by a "high" level on pin 8 of Scart 2 ("active device is present") or by the "WU"-line (wake up). This signal is generated out of the circuit around [7401], [7402] & [7403] and will become "high" if there is a signal on pin 20 of Scart 1- or Scart 2. The detection of the input level on pin 8 of Scart 2 ("8SC2") is done via an analog input of the CC-µP (less than 2V means inactive; 4,5V to 7V determines a source with 16:9 picture-ratio and greater than 9,5V is an active 4:3 source).

All signals from the digital board ("D_R", "D_G", "D_B", D_C", "D_Y" and "D_CVBS" are routed to the proper inputs of the STV6618 for amplification and driving purpose before they can be seen on the appropriate Scart outputs.

Parallel to this the "D_CVBS"- and the "D_Y"-line are passing a 6 dB-amplifier and driver-IC [7410] and are then routed to the CVBS-Cinch and Y/C-out rear. The chroma signal for this Y/C out is coming from the STV6618 - which makes the 6 dB-amplification - and a driver [7406] in between.

The detection of the picture ratio information on the Y/C-input front is made by measuring the DC-level on the Chroma signal via analog input of the CC-µP ("WSFI"-line). In case the level is higher than 3,5V the input signal is a 16:9 source. If the level is lower than 2,4V the picture ratio is 4:3.

For generation of the appropriate DC-voltage on the Y/C-out rear the "WSRO"-line is controlled via pin 18 of [7408] by the CC-µP (Pin 18 set to low means 4:3, pin 18 set to high determines 16:9).

The control of the switching voltage (Pin 8 of Scart 1) is done via 3-level-pin (nr.2) of the STV6618 [7408] and the transistors [7405], [7407] & [7409]. A "low" on pin 2 of [7408] causes around 11V on pin 8-Scart 1 (e.g. source with 4:3 picture-ratio active). Medium level (2,5V) on pin 2 of the STV6618 generates medium level (approx. 6V) on pin 8-Scart 1 (e.g. active source with 16:9) and a "high" on pin 2 of the STV6618 pushes pin 8-Scart 1 to "low" (e.g. inactive).

9.3.7 VPS/PDC- and Text-Dataslicer

For extraction of relevant information out of the video signal (time controlled recording, net-name-identification, time- & date- download) the STV5348 [7931] is used. Data transfer to/from the CC is fully done via I²C-bus and the input signal for decoding is the same as the one being routed to the digital board for recording purposes ("A_YCVBS"-line).

9.3.8 Analog Follow-Me

This circuit compares the video signal from the internal frontend ("VFV") of the recorder with that one of the connected TV-set ("CVBS1"). The TV set delivers the signal via Scart-cable. A comparator [7934] and several additional parts ([7932], [7933], …) are used to compare the two video signals. In case of both input signals are equal the output-line of this circuit ("FOME") is set to low. Detection is made via an input port of the CC-µP.

9.4 Analog board NAFTA- & APAC-Pal- version

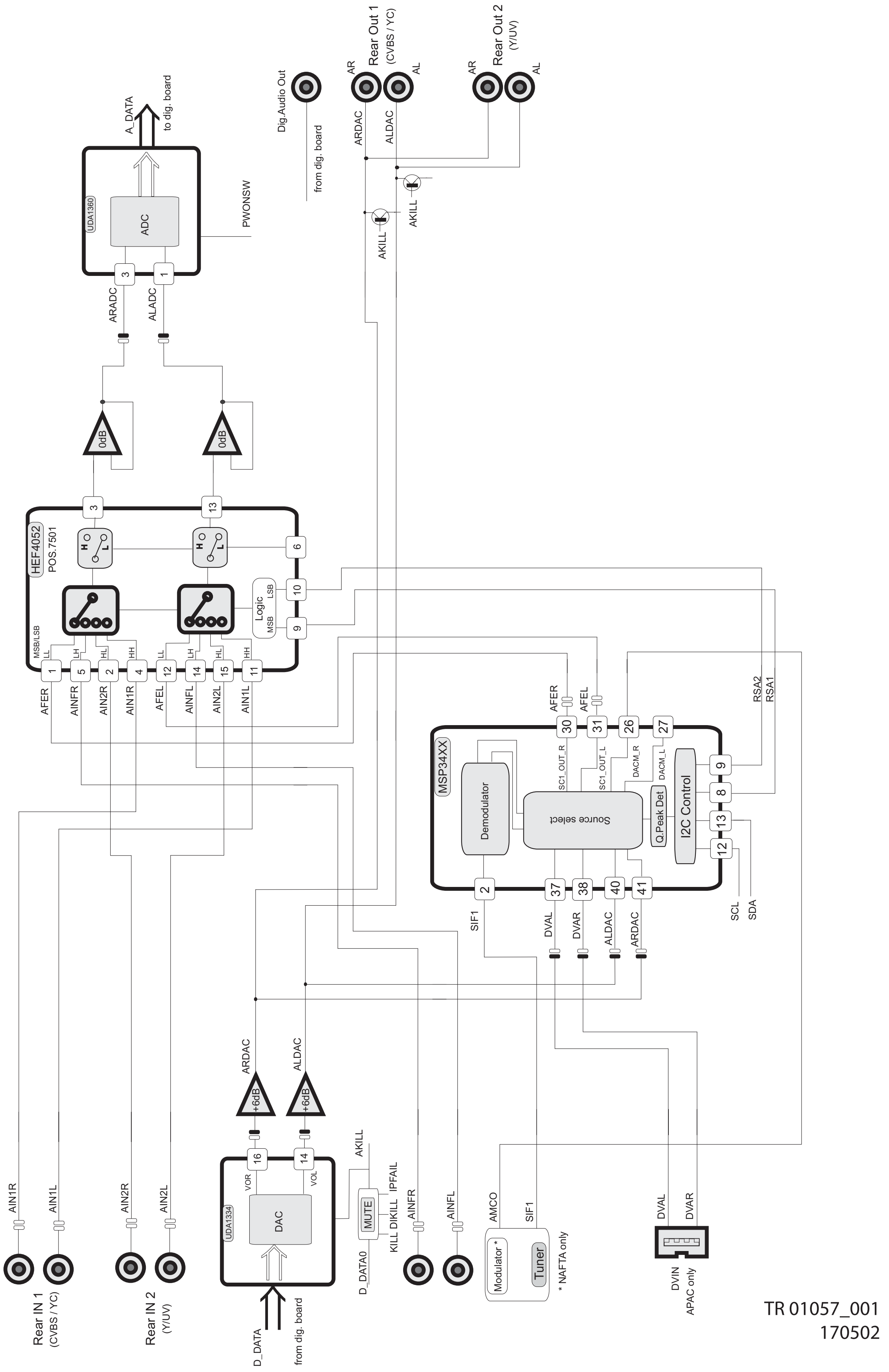
9.4.1 Frontend NAFTA

[1701] demodulates the video signal from the antenna input. Tuner and IF-demodulator are in one unit. Also a modulator is included in that part. The audio- and video-signal to the modulator are the ones from the selected input or the playback path of the set ("AMCO"- and "D_CVBS"-line). The control of the tuner is fully done via I²C-bus by the CC-µP. Via the "MSW"-signal and [7701] the modulator is switched on and off. In opposite to this the antenna loop-through is opened or closed. In the APAC-Pal version POS [1700] is used with the difference that it demodulates only PAL- instead of NTSC-signals and has also no modulator. The "CSW_SSW" line switches the modulator between CH3 or CH4 in the NTSC-version.
To achieve optimal tuning the "AFC"-signal is detected by the CC via an analog input; [3701], [3702] and [3703] are used for level adaptation (5V to 3V3). Pos [7700] is a driver for the video signal.
The sound demodulation is realized by the MSP34x5 [7600], which is also fully controlled via I²C-bus by the CC-µP (determination of bandwidth, amplitude, standard, …). The audio signals are available at pin 30 and pin 31 of [7600] and fed as "AFER"- & "AFEL"-line to the audio-I/O for further processing. As this PCB is used for different regions (NAFTA and APAC) either MSP3425 or MSP3415 are assembled.

9.4.2 Audio routintg

Audio IO NAFTA / APAC Overview

12.03.2002 Vers. 05


HEF4052
POS.7501
MSB/LSB
LL
LH
HL
HH
Logic
MSB
LSB
1
5
2
4
12
14
15
11
3
13
6
10
9
AFER
AINFR
AIN2R
AIN1R
AFEL
AINFL
AIN2L
AIN1L
0dB
0dB
ARADC
ALADC
UDA1360
ADC
PWONSW
A_DATA
to dig. board
Dig.Audio Out
from dig. board
Rear Out 1
(CVBS / YC)
Rear Out 2
(Y/UV)
AR
AL
ARDAC
ALDAC
AKILL
MSP34XX
Demodulator
Source select
Q.Peak Det
I2C Control
SC1_OUT_R
SC1_OUT_L
DACM_R
DACM_L
30
31
26
27
2
37
38
40
41
9
8
13
12
RSA2
RSA1
SCL
SDA
SIF1
DVAL
DVAR
ALDAC
ARDAC
Rear IN 1
(CVBS / YC)
Rear IN 2
(Y/UV)
AIN1R
AIN1L
AIN2R
AIN2L
UDA1334
DAC
VOR
VOL
16
14
+6dB
+6dB
ARDAC
ALDAC
D_DATA
from dig. board
MUTE
KILL DIKILL
IPFAIL
AKILL
D_DATA0
AINFR
AINFL
AMCO
SIF1
Modulator *
Tuner
* NAFTA only
DVAL
DVAR
DVIN
APAC only

TR 01057_001
170502

The sound processing is always done in stereo (that means separate left- and right-channel). The complete selection of the audio signal for recording is done by a HEF4052 [7501], which is a dual four-to-one multiplexer. The Op-Amp on the output [7504] is necessary for performance reasons and acts also as a driver. The selected signals “ARADC” and “ALADC” are directly fed to the Audio-ADC. The input lines for the selector [7501] are coming either from MSP [7600] (“AFEL”/”AFER”) or cinch rear in 1 (“AIN1L”/”AIN1R”) or cinch rear in 2 (“AIN2L”/”AIN2R”) or the cinch in front (“AINFL”/AINFR”). The [7501] is controlled via “RSA1”- and “RSA2”-signals coming from the MSP [7600]. The MSP acts as a port expander of the CC-µP.

As there can exist also a fifth input in case of DV-In is present the corresponding analog audio signals from the DVIO-board are firstly routed via extra cable and connector [1960] to the MSP, which acts as a preselector between audio from internal frontend or the DV-Input.

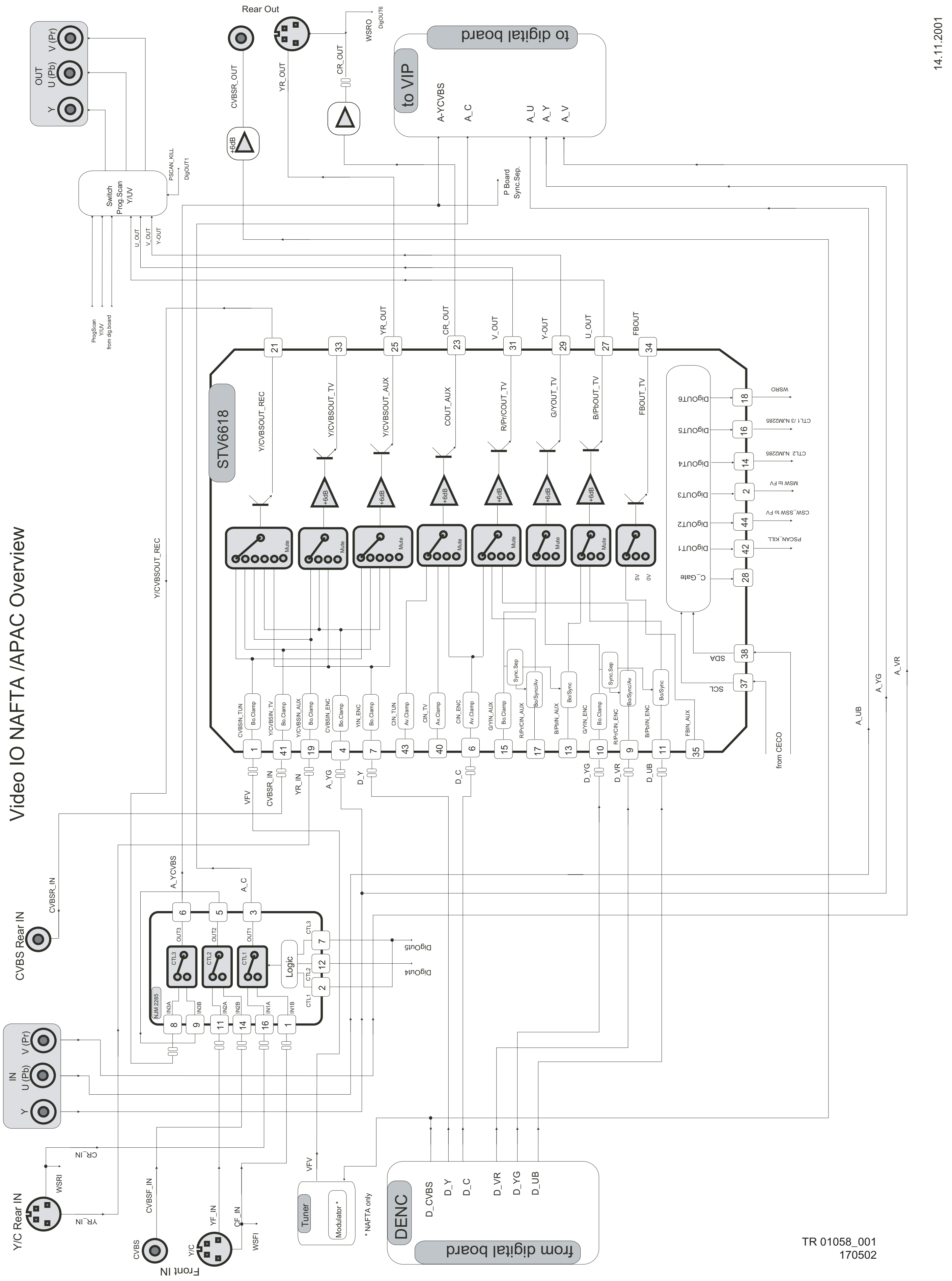
The signals from the audio DAC part (“ARDAC”/”ALDAC”) are directly routed to both cinch rear outputs, which are connected in parallel. To avoid plops and any other audible noise on the output there is a mute-stage implemented [7509], [7511] for each channel. The activation is done via “AKILL”-line, which is a combination of the “KILL” from CC-µP, “DAC_Mute” from DAC-part and “IPFAIL” of the power-supply-unit. The circuit around [6430], [6431], [7430] and [7404] generates this signal.

Additionally to analog audio the set is also equipped with a digital output via cinch plug [1951]. The signal is generated on the dig. board and routed via audio interface cable and connector [1900] to the Ana-PCB. Here the “DAOUT”-line first passes a 6-fold inverter [7580] being used as a driver and for performance reasons (noise reduction, jitter, …). Afterwards a transformer [5580] is necessary to achieve the correct level and also to have a ground isolated (floating) output before the signal is fed via [3580] to cinch plug [1951]. The capacitors POS [2580], [2582] & [2583] perform on the one side an AC-coupling between connector- and set-ground. On the other side they are necessary to keep radiation at a minimum for EMC reasons.

9.4.3 Audio ADC/DAC

The conversion of analog audio signals from the record-selector [7501] in the I/O (“ALADC”- & “ARADC”) is done via UDA1361TS [7005]. This IC can process input signals up to $2V_{rms}$ by using an external resistor [3039], [3041] in series to the input pins. As the level from the DVIO-Board is only $1V_{rms}$ a 6dB step can be performed by setting pin 7 of [7005] to 3,3V via [7006] and “PWONSW”-line controlled by the CC-µP to use the whole dynamic range of the ADC. All required clock signals are generated on the dig. board and only the audio data (“A_DAT”-line) are routed from Ana- to Dig.-PCB for further processing.
The transformation of dig. audio back to the analog domain is done by UDA1334BTS [7001]. All necessary clock signals are coming from the dig. board and dig. audio data (“D_DATA0”-line) are converted into analog signals, which are available at pin 14 and pin 16 of [7001]. Afterwards an Op-Amp. [7002] (line driver & level adaptation) and a low-pass-filter to increase signal performance (noise, distortions,…). are passed. Then both signals (“ALDAC” & “ARDAC”) are directly routed to the rear cinch output. The DAC has also a mute possibility, which can be activated by setting pin 8 to 3,3V via [7003]. This mute is controlled either by the dig. board (“D_IKLL”-line) or the “IPFAIL”-signal from power-supply-unit.
In addition to that the DAC [7001] and the cinch outputs can be killed (muted) in case of “digital silence” by the circuit around [7008],[7009] and [7010], when no audio data are available (e.g. “D_DATA0”-line zero)

9.4.4 Video-routing


Video IO NAFTA /APAC Overview

14.11.2001

TR 01058_001
170502
OUT
Y
U (Pb)
V (Pr)
Rear Out
CVBSR_OUT
YR_OUT
CR_OUT
WSRO
DigOUT6
+6dB
to digital board
to VIP
A-YCVBS
A_C
A_U
A_Y
A_V
Switch
Prog.Scan
Y/UV
PSCAN_KILL
DigOUT1
U_OUT
V_OUT
Y-OUT
ProgScan
Y/UV
from dig.board
P Board
Sync.Sep.
STV6618
Y/CVBSOUT_REC
Y/CVBSOUT_TV
Y/CVBSOUT_AUX
COUT_AUX
R/Pr/COUT_TV
G/YOUT_TV
B/PbOUT_TV
FBOUT_TV
FBOUT
V_OUT
Y-OUT
U_OUT
Mute
DigOUT6
DigOUT5
DigOUT4
DigOUT3
DigOUT2
DigOUT1
C_Gate
5V
0V
WSRO
CTL1 /3 NJM2285
CTL2 NJM2285
MSW to FV
CSW_SSW to FV
PSCAN_KILL
SDA
SCL
from CECO
CVBSIN_TUN
Y/CVBSIN_TV
Y/CVBSIN_AUX
CVBSIN_ENC
Y/IN_ENC
CIN_TUN
CIN_TV
CIN_ENC
G/YIN_AUX
R/Pr/CIN_AUX
B/PbIN_AUX
G/YIN_ENC
R/Pr/CIN_ENC
B/PbIN_ENC
FBIN_AUX
Bo.Clamp
Av.Clamp
Sync.Sep
Bo/Sync/Av
Bo/Sync
VFV
CVBSR_IN
YR_IN
A_YG
D_Y
D_C
D_YG
D_VR
D_UB
A_UB
A_YG
A_VR
CVBS Rear IN
CVBSR_IN
A_YCVBS
A_C
NJM2285
CTL1
CTL2
CTL3
OUT1
OUT2
OUT3
IN1A
IN1B
IN2A
IN2B
IN3A
IN3B
Logic
DigOut5
DigOut4
IN
Y
U (Pb)
V (Pr)
Y/C Rear IN
WSRI
CR_IN
YR_IN
CVBSF_IN
YF_IN
CF_IN
WSFI
CVBS
Y/C
Front IN
VFV
Tuner
Modulator *
* NAFTA only
DENC
D_CVBS
D_Y
D_C
D_VR
D_YG
D_UB
from digital board

The complete Video-I/O-switching is basically realized by the matrix switch STV6618 [7408], which is controlled via I²C-bus by the CC. All used outputs excluding pin 21 (Y/CVBS-REC) have a 6dB-amplification and a 75 Ohms-driver-stage inside. This IC also includes several digital outputs, which are used for switching purposes on the analog board. The record selector inside the switch selects between the CVBS from frontend, the CVBS from Cinch-Rear or Y from the S-Video-input rear. Afterwards the signal passes another switch [7411] in which a selection between signals from the front or the preselected ones is done. The output signals of [7411] are fed as "A_YCVBS"- and "A_C"-line to the digital board for further processing.

To reduce the number of external presets there is only one station for CVBS or Y/C (front and rear). The set automatically detects between the two inputs depending on the presence of a video signal (sync separator-circuit on mP-sub-board) where Y/C has higher priority.

The Y/U/V-inputs are directly routed to the digital PCB. Only the Y-line has to be present additionally on pin 4 of [7408] for video recognition.

The signals "D_C" and "D_Y" are fed through [7408] (6dB amplification) and via [7406], [7409] used as driver to the S-Video output connector. The "D_CVBS" line is directly routed to the modulator and via the circuit around [7431] and [7432] amplified by 6dB before it is fed to the CVBS output plug.

The Y/U/V signals from the digital board are also passing [7408] for 6dB amplification and driving purpose.

To achieve optimal picture quality the set is equipped with a simple progressive scan function based on a so-called line doubler. The complete generation of the signal is done on the digital board and via a separate cable and connector [1946] the corresponding Y/U/V lines are routed to the analog PCB. As there is only one Y/U/V output available a switching between interlaced and progressive output is necessary. While the transistors [7421], [7422], [7424], [7425], [7427] and [7428] are used as driver for Y/U/V progressive, [7423], [7426] and [7429] together with [7405] are necessary for killing these signals via pin 42 of [7408] in case the interlaced is selected ("PSCAN_KILL"-line set to low). If progressive output is active the pins 27, 29 and 31 of [7408] are set to high impedance and "PSCAN_KILL" is also high (e.g. 5V).

The detection of the picture ratio information on the Y/C inputs (rear or front) is done by measuring the DC-level on the Chroma signal via an analog input of the CC-µP ("WSRI"- and "WSFI"-line). In case the level is higher than 3,5V the input signal is a 16:9 source, if the level is lower than 2,4V the picture ratio is 4:3.

For generation of the appropriate DC-voltage on the Y/C output the "WSRO"-line is controlled via pin18 of [7408] by the CC-µP (Pin 18 set to low means 4:3, pin 18 set to high determines 16:9).

During Stand-By there is also no loop-through of any input to any output performed.

9.5 Digital Board

9.5.1 Record Mode

Video Part

Analog Video input signals CVBS, YC and UV(RGB for EURO and YUV for USA) are routed via the analog board to connector 1601 and sent to IC7500 SAA7118 (Video Input Processor). Digital video input signals (DV_IN_DATA(7:0)) are sent from the DIVIO board through the connector 1603 and further also to IC7500.
IC7500 (VIP) encodes the analog video to digital video and processes the digital video to a digital video stream (CCIR656 format). This output stream (VIP_YUV[7:0]) goes to IC7403 SAA6752H (EMPRESS) and to IC7100 Versatile Stream Manager. The latter uses the data for VBI (vertical blanking interval) extraction.
IC7403 (EMPRESS) encodes the digital video stream into a MPEG2 video stream that is fed to IC7100 (VSM).

Audio Part

I2S audio are sent from the analog board to IC7403 EMPRESS via connector 1602. The EMPRESS compresses I2S audio data into an AC3 audio stream which is fed to IC7100 (VSM).

Front-End I2S

IC7100 (VSM) interfaces directly to the different hardware modules such as Basic Engine, EMPRESS IC7403, MPEG decoder IC7200 (Sti5508) and buffers the data streams that are coming from or going to these hardware modules.
In IC7100 (VSM), the video MPEG2 stream and the audio AC3 stream are multiplexed into a I2S packetized stream. The serial data are sent to the Basic Engine to be recorded.

Loop-Through

The multiplexed audio and video stream in the VSM is fed back via the parallel front-end interface to IC7200 (Sti5508). This IC decodes the MPEG stream into analog video and I2S audio. The video and audio signals are routed to the analog board via connectors 1601 and 1602. During recording, the recorded signal is present at the outputs of the analog board.

9.5.2 Playback Mode

During playback, the serial data from the Basic Engine is going directly to the Sti5505 via the serial front-end I2S interface. The Sti5508 is a MPEG & Audio/video decoder and has the following outputs:

- To the analog board:
  - analog video RGB, YC, CVBS
  - I2S audio (PCM format)
  - SPDIF audio (digital audio output)
- To the Progressive scan board:
  - digital video YC(7:0).

9.5.3 S2B Interface

The S2B interface between the VSM (IC7100) and the Servo processor MACE3 controls the Basic Engine during record and playback mode.

9.5.4 System Clock

System clocks(27MHz) of VSM, Sti5508, EMPRESS and Progressive Scan are generated by oscillator 7906

9.5.5 Audio Clock

During record mode, the audio clock ACC_ACLK_OSC is generated by IC7102 (PLL) because then, the audio clock must be sychronized with the incoming video (VIP_FID) from the VIP.
During playback mode, the audio clock ACC_ACLK_PLL is generated by the clock synthesizer IC7900 (MK2703S).
Both ACC_ACLK_OSC(also goes to the EMPRESS as ACLK_EMP) and ACC_ACLK_PLL are fed to the VSM. This IC selects the appropriate clock to the STI5508. The EMPRESS IC derives from the incoming ACLK_EMP the I2S audio encoder clocks AE_BCLK and AE_WCLK which are sent to the VSM.

9.5.6 On/Off

The digital board is not powered in standby mode. Control signal ION, coming from the analog board, will enable the PSU and power the digital board.

- ION = High: the digital board is in powered down standby mode
- ION = Low: the power supply to the digital board is enabled

9.5.7 Reset

Control signal IRESET_DIG, controlled by the microprocessor on the analog board is sent to the RESET LOGIC circuit.

- IRESET_DIG = Low in standby mode
- IRESET_DIG = High: the whole system is reset and the Digital board is waked up.

9.5.8 I2C Bus

Sti5508 is master of the I2C bus. The following IC's are controlled by the I2C bus:

- IC7201 NVRAM
- IC7403 EMPRESS
- IC7500 VIP
- IC7700 FLI2200 Video Deinterlacer Line Doubler
- IC7801 ADV7196 Video Denc

9.5.9 EMI Bus

The following IC's are connected to the External Memory Interface bus (EMI) which functions as system bus:

- IC7301 and 7302: Flash memories which contain the application and diagnostic software
- IC7100: VSM
- IC7200: MPEG AV Decoder

Block Diagram Digital Board

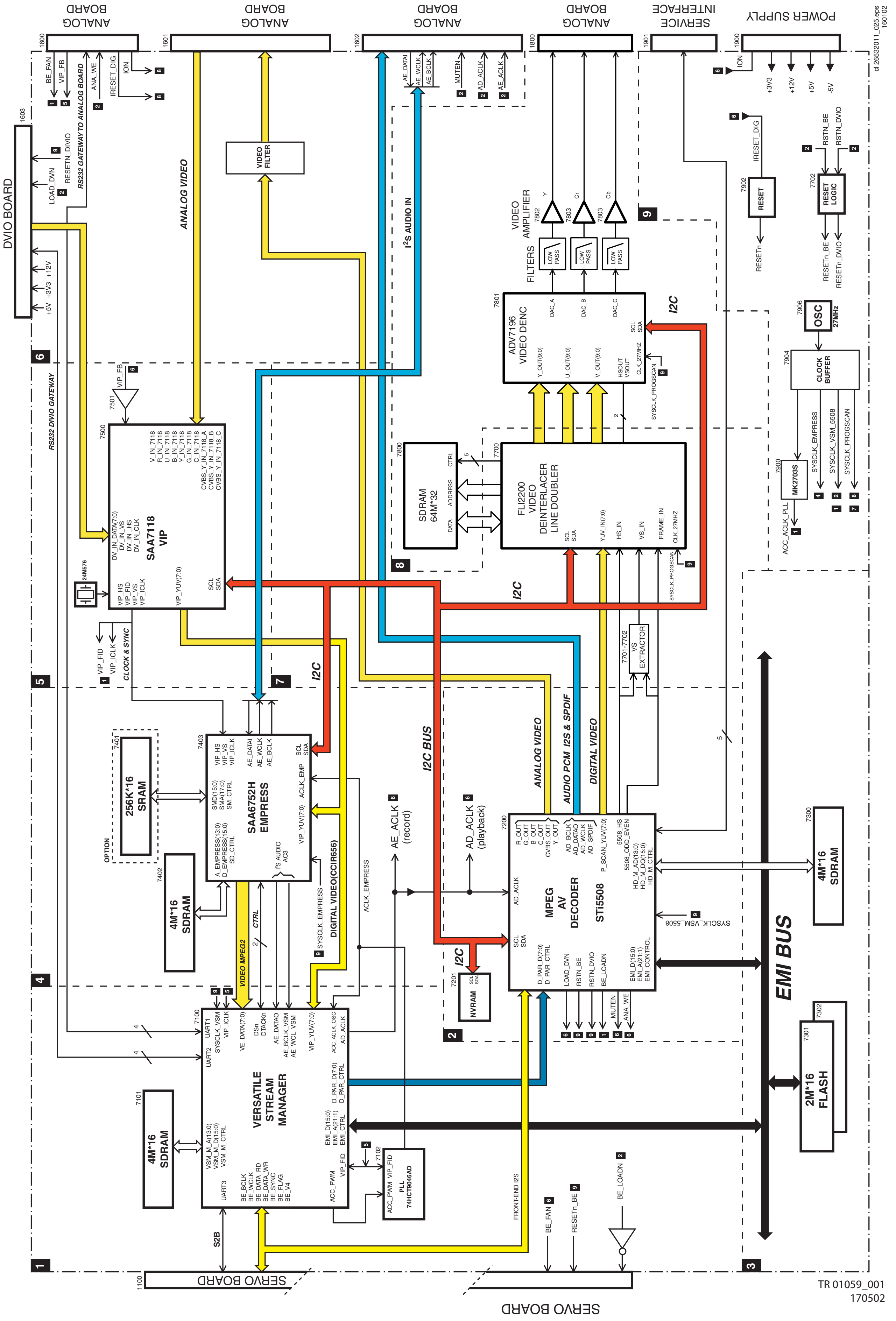
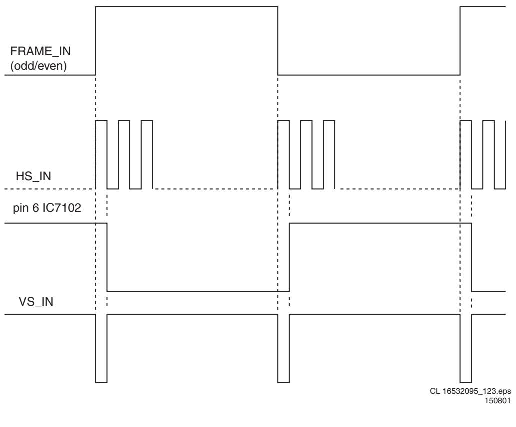

DVIO BOARD
ANALOG BOARD
ANALOG BOARD
ANALOG BOARD
ANALOG BOARD
SERVICE INTERFACE
POWER SUPPLY
SERVO BOARD
SERVO BOARD
RS232 GATEWAY TO ANALOG BOARD
RS232 DVIO GATEWAY
ANALOG VIDEO
VIDEO FILTER
I²S AUDIO IN
VIDEO AMPLIFIER
FILTERS
LOW PASS
ADV7196 VIDEO DENC
RESET
RESET LOGIC
OSC 27MHz
CLOCK BUFFER
MK2703S
SAA7118 VIP
CLOCK & SYNC
SDRAM 64M*32
FLI2200 VIDEO DEINTERLACER LINE DOUBLER
VS EXTRACTOR
I2C
I2C BUS
256K*16 SRAM
OPTION
4M*16 SDRAM
SAA6752H EMPRESS
VIDEO MPEG2
CTRL
DIGITAL VIDEO(CCIR656)
AE_ACLK (record)
AD_ACLK (playback)
ANALOG VIDEO
AUDIO PCM I2S & SPDIF
DIGITAL VIDEO
MPEG AV DECODER
STI5508
NVRAM
4M*16 SDRAM
EMI BUS
2M*16 FLASH
VERSATILE STREAM MANAGER
4M*16 SDRAM
PLL 74HCT9046AD
S2B
FRONT-END I2S
TR 01059_001
170502
cl 26532011_025.eps
160102

Figure 9-1

9.5.10 Progressive Scan

Description
The progressive scan part is integrated in the Digital Board and built around the SAGE Fli2200 de-interlacer / line doubler (7701). This I2C controlled de-interlacer uses a 64Mbit SDRAM (32bit x 2M) to perform high quality deinterlacing (meshing). The de-interlacer gets his digital YUV input data from the STi5508 (7200). The format of the digital YUV input to the SAGE is CCIR656 with separated Hsync, Vsync and odd/even signal running on 27Mhz.
Because the STi5508 doesn't have a Vsync output the odd/even output of this IC has to be translated to a Vsync signal. Some glue logic has been added to extract the vertical sync. The glue logic circuit consists of Flip-Flop IC 74HC74D (7701) and EXOR 74LVC86 (7702). The next diagram shows how the vertical sync is extracted.

Vertical Sync


FRAME_IN
(odd/even)
HS_IN
pin 6 IC7102
VS_IN

CL 16532095_123.eps
150801

Figure 9-2

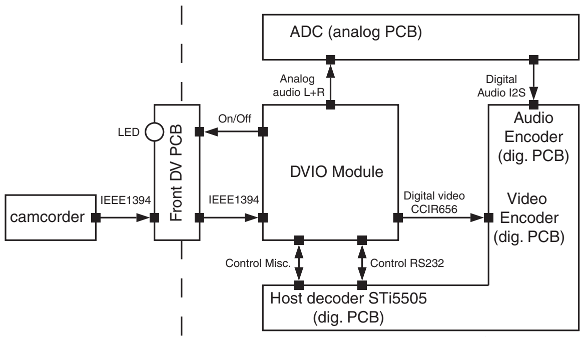
The output of the de-interlacer (4:4:4 progressive video) is fed to the Analog Devices ADV71967 MacroVision compliant DENC (7801).
The YUV current output of the DENC is fed via a low pass filter to the single supply output opamps AD8061/8062 (7802-7803). The analog video is fed via a 7 poled flex to the analog board where the YUV 2FH cinch connectors are located.

9.6 Divio Board

9.6.1 Short Description of the Module:

The DVIO Module is a decoder for DV streams. The module is intended for the Philips DVDR1000/002 en DVDR1000/172 DVD+RW recorders. Input is a stream from a DV-camcorder IEEE1394. Outputs are CCIR656 Video and Analog audio (L+R). A serial control interface is present.
The following picture shows the location of the DVIO Module inside the DVDR set.

Description DIVIO Module


ADC (analog PCB)
Analog
audio L+R
Digital
Audio I2S
LED
On/Off
Front DV PCB
DVIO Module
Audio
Encoder
(dig. PCB)
camcorder
IEEE1394
IEEE1394
Digital video
CCIR656
Video
Encoder
(dig. PCB)
Control Misc.
Control RS232
Host decoder STi5505
(dig. PCB)

CL 16532095_118.eps
150801

Figure 9-3

9.6.2 Block Diagram

Block Diagram DVIO

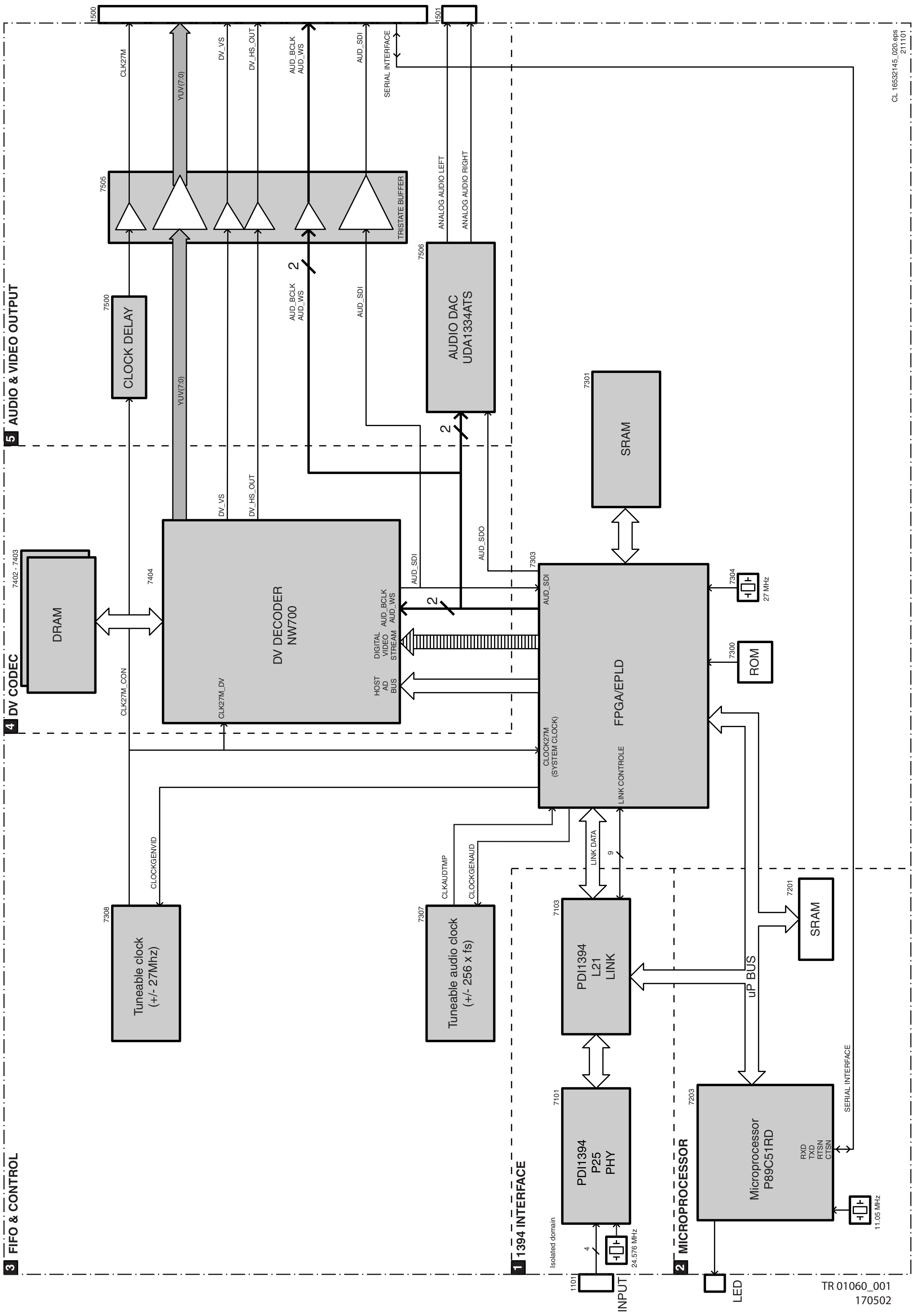

5 AUDIO & VIDEO OUTPUT
4 DV CODEC
3 FIFO & CONTROL
1 1394 INTERFACE
2 MICROPROCESSOR
1500
1501
CLK27M
YUV(7:0)
DV_VS
DV_HS_OUT
AUD_BCLK
AUD_WS
AUD_SDI
SERIAL INTERFACE
7505
TRISTATE BUFFER
ANALOG AUDIO LEFT
ANALOG AUDIO RIGHT
7500
CLOCK DELAY
7506
AUDIO DAC
UDA1334ATS
2
7301
SRAM
7402 - 7403
DRAM
7404
DV DECODER
NW700
HOST AD BUS
DIGITAL VIDEO STREAM
CLK27M_CON
CLK27M_DV
AUD_SDO
7303
FPGA/EPLD
CLOCK27M (SYSTEM CLOCK)
LINK CONTROLE
LINK DATA
9
7304
27 MHz
7300
ROM
7201
SRAM
uP BUS
7308
Tuneable clock (+/- 27Mhz)
CLOCKGENVID
7307
Tuneable audio clock (+/- 256 x fs)
CLKAUDTMP
CLOCKGENAUD
7103
PDI1394 L21 LINK
7101
PDI1394 P25 PHY
Isolated domain
4
24.576 MHz
1101
INPUT
7203
Microprocessor P89C51RD
RXD
TXD
RTSN
CTSN
11.05 MHz
LED
CL 16532145_020.eps 211101
TR 01060_001 170502

Figure 9-4

9.6.3 Functional Description

The DVIO module consists of the following blocks (see blockdiagram):

1. IEEE1394 Interface
   - PDI1394P25(7101)
   - PDI1394L40(7103)
2. Micro-controller
   - 89C51RD2(7203)
   - 32kb SRAM(7201)
3. FIFO and Control
   - FPGA/EPLD(7303)
   - SRAM(7301)
   - Clock generation(7307, 7308)
     – Independently tuneable audio and video clock, implemented with FPGA and PLL
4. DV-Decoder
   - NW700(7404)
   - EDO DRAM(7402, 7403)
5. Audio & Video output
   - Audio DAC UDA1334ATS(7602)
   - Clock delay(7500)
   - Tristate buffer(7505)

IEEE1394 Interface

The 1394 interface consists of a PDI1394P25 physical layer and a PDI1394L40 link layer.
It has the following features:

- S200 operation (200 megabit per second)
- One i.Link port (4 pin)
- AV link port

Micro-Controller

The 89C51RD2 processor has a 8051 cpu with the following extra features:

- 64 kilobyte of flash memory as program memory
- 1 kilobyte of internal data memory
- watchdog timer
- PCA outputs
- Power control modes
- Speed allowed up to 33 MHz but used at 11.0592 MHz
- On board ISP(In Circuit Programming) functionality

ISP

By use of In Circuit Programming, it is possible to update the software of the DVIO board that is in the 89C51RD2. ISP can be made active by resetting the processor and keeping the ISPN pin low during reset. During ISP, the ISPN signal on the board has to be kept low. A programming voltage of 5V is always present at the Vpp pin. When the ISP mode is active, the new program can be sent to the microprocessor through the serial port.

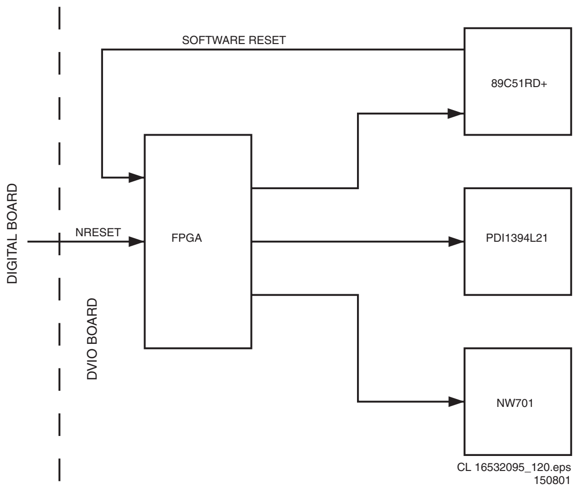
Fifo and Control

In decode mode, an isochronous AV-stream is flowing through the IEEE1394 Interface into the FPGA. The FPGA stores the data in a FIFO buffer (ping-pong buffer type, i.e. 2 buffers that can hold one whole frame each).

Reset

The FPGA controls the reset signals on the board. This has the advantage that it is possible to reset the board both from software and hardware.

Reset



CL 16532095_120.eps
150801

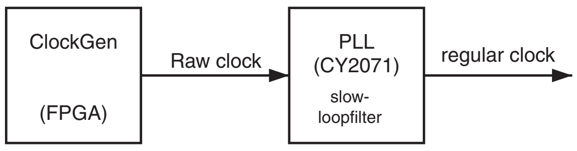
Figure 9-5

The board reset NRESET will reset the whole board, and the software reset can reset everything except the microprocessor itself. Power-on reset is implemented by adding pull-ups and pull-downs to the reset inputs of the devices. Since the FPGA will tri-state all the pins during configuration, reset is active during configuration time. After configuration of the FPGA, the reset signals are driven inactive. The NRESET signal is used to reset the DVIO board. After reset, the tri-state buffers to connector 1500 are disabled.

Clock Circuit

There are 2 clocks to consider in the system, this is the video clock and the audio clock. These two clocks do not have a relation, so these clocks must be considered independently. The video clock is approximately 27 MHz. When data is flowing from an external source that is supposed to have the same frequency, it does not have exactly the same clock. Because of this, buffers may under-run of over-run. Since the clock can not be directly recovered from the 1394 interface, there has to be another solution. This solution is a tuneable clock that is adjusted to the required frequency to process at the rate of the incoming data.
The hardware implementation of such a tuneable clock is as follows:

Clock Circuit



CL 16532095_121.eps
150801

Figure 9-6

The same can be applied for the audio clock. For this clock, a frequency of 8.192 MHz, 11.2896 MHz or 12.228 MHz is required. This depends on the sample-rate frequency(32kHZ, 44.1kHZ or 48kHZ)of the audio signal.

DV Decoder

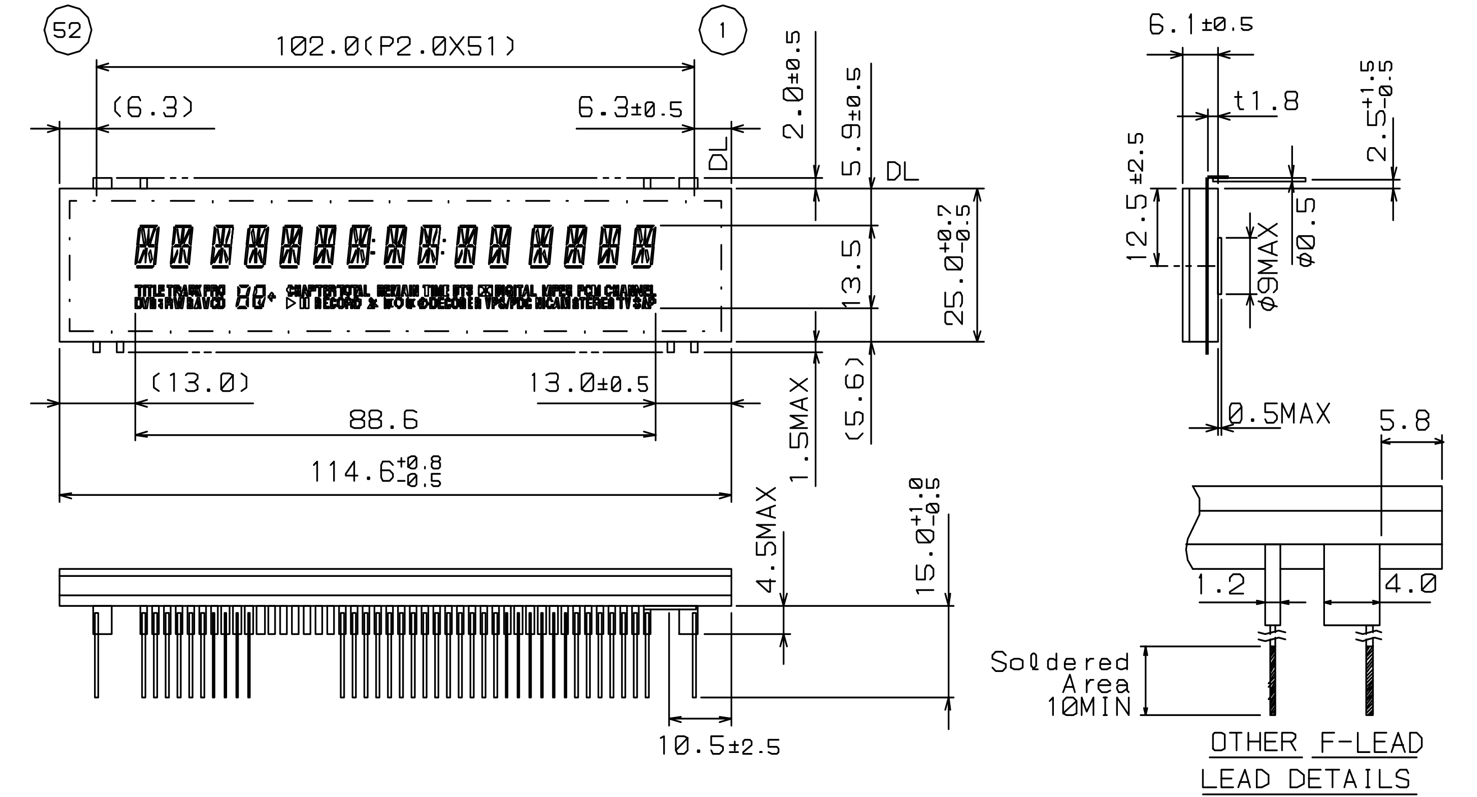
The AV-data will go from the FIFO to the NW700. The NW700 decodes the stream into video data in 656 format and audio data in I2S format.
The microprocessor has the ability to read the status registers of the NW700 through the FPGA. By reading these registers, extra data from the DV stream, that is not decoded into audio or video, can be sent to the digital board using pin TXD of the serial interface. This data includes time stamp and some more.

Audio & Video Output

The audio I2S data are sent to audio DAC UDA1334. Analog audio left and right signals are connected to the analog board.
The tristate buffer enables the digital video stream to the Video Input Processor on the digital board when the DV source is selected.
The clock delay synchronizes the AV clock with the AV data at the output.

9.7 IC's Display Panel

9.7.1 IC7100


52
1
102.0(P2.0X51)
(6.3)
6.3±0.5
2.0±0.5
5.9±0.5
DL
DL
13.5
25.0+0.7 -0.5
(5.6)
1.5MAX
(13.0)
13.0±0.5
88.6
114.6+0.8 -0.5
4.5MAX
15.0+1.0 -0.5
10.5±2.5
6.1±0.5
t1.8
2.5+1.5 -0.5
12.5 ±2.5
φ9MAX
φ0.5
0.5MAX
5.8
1.2
4.0
Soldered
Area
10MIN
OTHER F-LEAD
LEAD DETAILS

PIN CONNECTION

PIN NO.	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27
CONNECTION	F2	NX	NP	NP	10G	9G	8G	7G	6G	5G	4G	3G	2G	1G	NX	NX	NX	NX	NX	NX	NX	P15	P16	P17	P18	P19

PIN NO.	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
CONNECTION	P20	P21	P22	P23	P24	P25	P26	P27	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	NP	NP	NX	F1

NOTE
1) F1,F2 --- Filament
2) NP ------- No pin
3) NX ------- No extend pin
4) DL ------- Datum Line
5) 1G~10G --- Grid
6) Field of vision is a minimum of 26° from the lower side.

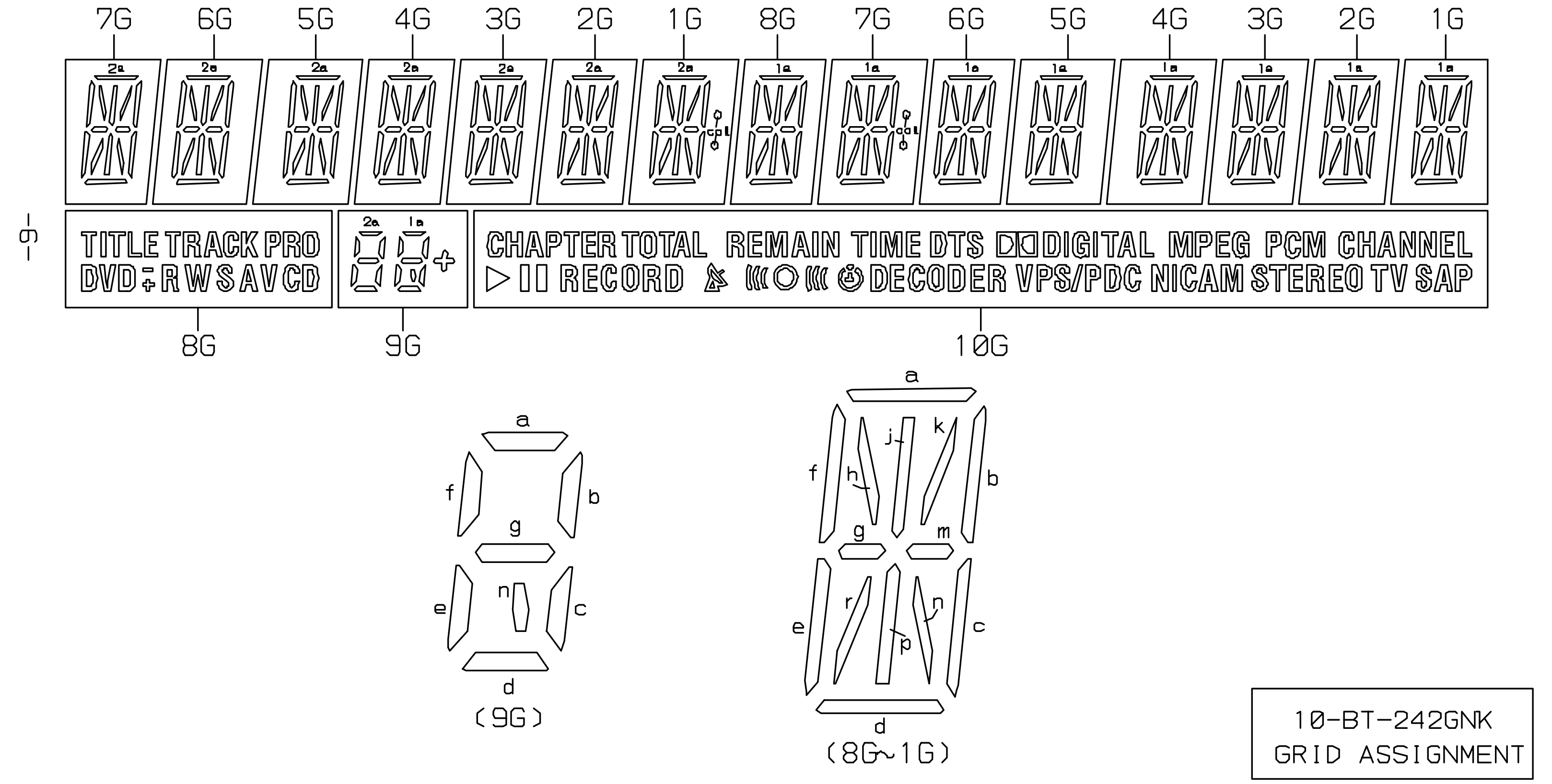
(unit in mm)

10-BT-242GNK
OUTER DIMENSION

-4-

2.8

GRID ASSIGNMENT


7G
6G
5G
4G
3G
2G
1G
8G
7G
6G
5G
4G
3G
2G
1G
2a
1a
col
TITLE TRACK PRO
DVD+-R W S A V CD
CHAPTER TOTAL REMAIN TIME DTS DIGITAL MPEG PCM CHANNEL
RECORD DECODER VPS/PDC NICAM STEREO TV SAP
8G
9G
10G
-6-
a
b
c
d
e
f
g
n
(9G)
a
b
c
d
e
f
g
h
j
k
m
n
p
r
(8G~1G)
10-BT-242GNK
GRID ASSIGNMENT

ANODE CONNECTION

	1G	2G	3G	4G	5G	6G	7G	8G	9G	10G
P1	1a	1a	1a	1a	1a	1a	1a	1a	1a	PCM
P2	1j,1p	1j,1p	1j,1p	1j,1p	1j,1p	1j,1p	1j,1p	1j,1p	1f	MPEG
P3	1h	1h	1h	1h	1h	1h	1h	1h	1b	DD DIGITAL
P4	1k	1k	1k	1k	1k	1k	1k	1k	1g	DTS
P5	1b	1b	1b	1b	1b	1b	1b	1b	1c	TIME
P6	1f	1f	1f	1f	1f	1f	1f	1f	1e	REMAIN
P7	1m	1m	1m	1m	1m	1m	1m	1m	1n	TOTAL
P8	1g	1g	1g	1g	1g	1g	1g	1g	1d	CHAPTER
P9	1c	1c	1c	1c	1c	1c	1c	1c	✚	SAP
P10	1e	1e	1e	1e	1e	1e	1e	1e	–	TV
P11	1r	1r	1r	1r	1r	1r	1r	1r	–	STEREO
P12	1n	1n	1n	1n	1n	1n	1n	1n	–	NICAM
P13	1d	1d	1d	1d	1d	1d	1d	1d	–	VPS/PDC
P14	coℓ	–	–	–	–	–	coℓ	–	–	CHANNEL
P15	2a	2a	2a	2a	2a	2a	2a	CD	–	DECODER
P16	2j,2p	2j,2p	2j,2p	2j,2p	2j,2p	2j,2p	2j,2p	V	–	⏻
P17	2h	2h	2h	2h	2h	2h	2h	A	–	((((Right)
P18	2k	2k	2k	2k	2k	2k	2k	S	–	○
P19	2b	2b	2b	2b	2b	2b	2b	W	–	((((Left)
P20	2f	2f	2f	2f	2f	2f	2f	R	–	📡
P21	2m	2m	2m	2m	2m	2m	2m	✚	2d	RECORD
P22	2g	2g	2g	2g	2g	2g	2g	▭	2e	▯▯
P23	2c	2c	2c	2c	2c	2c	2c	DVD	2c	▷
P24	2e	2e	2e	2e	2e	2e	2e	TITLE	2g	–
P25	2r	2r	2r	2r	2r	2r	2r	TRACK	2b	–
P26	2n	2n	2n	2n	2n	2n	2n	PRO	2f	–
P27	2d	2d	2d	2d	2d	2d	2d	–	2a	–

10-BT-242GNK
ANODE CONNECTION

9.8 IC's Analog Board

9.8.1 IC1705

VHF/UHF splitter-tuner UV1316K MK3

FEATURES

- Member of UV1300 MK3 family of small-sized UHF/VHF tuners
- Integrated passive splitter
- Systems CCIR: B/G, H, L, L', I and I'; OIRT: D/K
- Digitally-controlled (PLL) tuning via I^{2}C-bus
- Fast 400kHz I^{2}C bus protocol compatible with 3.3V and 5V micro controllers
- Off-air, S-cable and hyperband channels
- World standardized mechanical dimensions and pinning. Horizontal mounting is optionally available.

DESCRIPTION

The UV1316K MK3 splitter - tuner belongs to the UV1300 MK3 family of tuners, which are designed to meet a wide range of TV applications. It is a full band tuner suitable for CCIR systems B/G, H, L, L', I and I'. The low IF output impedance is designed for direct drive of a wide variety of SAW filters with sufficient suppression of triple transient. In addition, it is equipped with 2 two standard items, one a 5 level Analog Digital Converter and the other an internal wide band AGC with I^{2}C selectable TOP.

This tuner complies with the requirements of radiation, signal handling capability and immunity conforming to:

- CISPR 13 (1990) incl. amendment 1 (1992) and amendment 2 (1993) and CISPR 20
- European standards CENELEC EN55013, EN55020

MARKING

The following items of information are printed on a sticker that is on the top cover of the tuner:

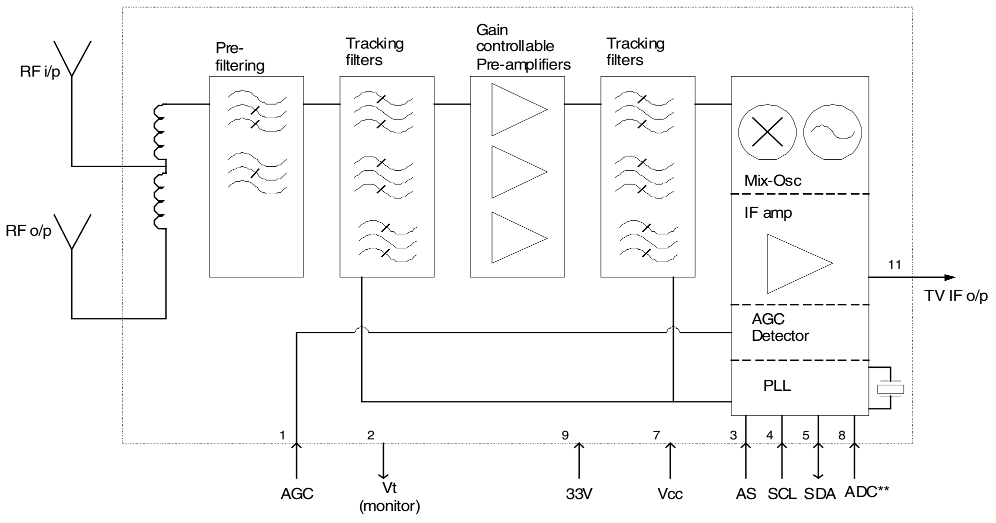
- Type number
- Code number
- Origin letter of factory
- Change code
- Year and week code

ORDERING INFORMATION

TYPE	DESCRIPTION	ORDER NUMBERS
UV1316K/A I G -3	Asymmetrical IF output; IEC connector	3139 147 17001

VHF/UHF splitter-tuner UV1316K MK3

BLOCK DIAGRAM


RF i/p
RF o/p
Pre-filtering
Tracking filters
Gain controllable Pre-amplifiers
Tracking filters
Mix-Osc
IF amp
AGC Detector
PLL
11
TV IF o/p
1
2
9
7
3
4
5
8
AGC
Vt (monitor)
33V
Vcc
AS
SCL
SDA
ADC**

** ADC option not available in NTSC versions

PINNING

SYMBOL	PIN	DESCRIPTION
AGC	1	Gain Control Voltage
TU	2	Tuning voltage
AS	3	I^{2}C-Bus Address Select
SCL	4	I^{2}C-Bus Serial Clock
SDA	5	I^{2}C-Bus Serial Data
n.c.	6	Not Connected
V_s	7	PLL Supply Voltage +5V
n.c./ADC	8	Not Connected / ADC Input (1)
V_{ST}	9	Fixed tuning Supply Voltage +33V
n.c	10	Do not connect
IF1	11	Asymmetrical IF Output
GND	M1,M2,M3,M4	Mounting Tags (Ground)

9.8.2 IC7408

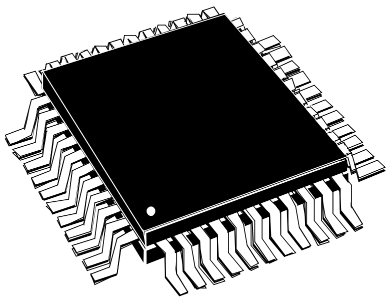
STV6618

VIDEO SWITCH MATRIX FOR DVD

TARGET SPECIFICATION

FEATURES

- I^{2}C Bus Control
- 5 Y/CVBS Inputs, 3 Y/CVBS Outputs
- 3 C Inputs, 1 C Output
- 2 RGB/YPrPb Inputs, 1 RGB/YPrPb Output
- 6 dB Gain on all 150 Buffer Outputs
- Integrated 150 Buffers
- Video Muting on all Outputs
- Bottom Clamp on all CVBS/Y, Average Clamp on C Inputs, Bottom Clamp on RGB, Sync-tip Clamp on PrPb signals
- Bandwidth: 15 MHz
- Crosstalk: 50 dB



TQFP44
(10 x 10 x 1.4 mm)
(Thin Full Plastic Quad Flat Pack)

ORDER CODE: STV6618

DESCRIPTION

The STV6618 is a highly integrated I^{2}C bus-controlled video switch matrix, optimized for use in recordable Digital Video Disk applications or DVD players. It provides video routings required for connections to two external devices (Europe 2 SCARTs), internal tuners, digital encoders and recorders.

1.2 Pin Description

Pin No.	Symbol	Description
1	Y/CVBSIN_TUN	Y/CVBS Input from Tuner
2	DIGOUT3	Digital Output Pin 3
3	GND1	Ground Supply 1 for Video Inputs
4	CVBSIN_ENC	CVBS Input from Encoder
5	DECV	Video decoupling capacitor
6	CIN_ENC	Chroma Input from Encoder
7	YIN_ENC	Y Input from Encoder
8	V_{CC}	+5 V Power Supply for Video Inputs
9	R/PR/CIN_ENC	Red or Pr or Chroma Input from Encoder
10	G/YIN_ENC	Green or Y Input from Encoder
11	B/PBIN_ENC	Blue or Pb Input from Encoder
12	GND2	Ground Supply 2 for Video Inputs
13	B/PBIN_AUX	Blue or Pb Input from Auxiliary (SCART2 or external Cinch)
14	DIGOUT4	Digital Output Pin 4
15	G/YIN_AUX	Green or Y Input from Auxiliary (SCART2 or external Cinch)
16	DIGOUT5	Digital Output Pin 5
17	R/PR/CIN_AUX	Red or Pr or Chroma input from Auxiliary (SCART2 or external Cinch)
18	DIGOUT6	Digital Output Pin 6
19	Y/CVBSIN_AUX	Y/CVBS Input from Auxiliary (SCART2 or external Cinch)
20	VCCB_REC	Video Output Recorder Buffer Supply Pin
21	Y/CVBSOUT_REC	Y/CVBS Output to Recorder
22	GNDB_REC	Ground Supply for Recorder Buffer
23	COUT_AUX	Chroma Output to Auxiliary (SCART2 or external Cinch)
24	VCCB1	Video Output Buffer Supply Pin
25	Y/CVBSOUT_AUX	Y/CVBS Output to Auxiliary (SCART2 or external Cinch)
26	GNDB	Ground Supply for Video Buffer
27	B/PBOUT_TV	Blue or Pb Output to TV (SCART1 or external Cinch)
28	C_GATE	External Transistor Command for Bidirectinnal B/C SCART I/O
29	G/YOUT_TV	Green or Y Output to TV (SCART1 or external Cinch)
30	VCCB2	Video Buffer
31	R/PR/COUT_TV	Red or Pr or Chroma Output to TV (SCART1 or external Cinch)
32	VCCB3	Video Output Buffer Supply Pin
33	Y/CVBSOUT_TV	Y/CVBS Output to TV (SCART1 or external Cinch)
34	FBOUT_TV	Fast Blanking Output to TV (SCART1)
35	FBIN_AUX	Fast Blanking Input from Auxiliary (SCART2)

Pin No.	Symbol	Description
36	VDD	+5 V Digital Power Supply
37	SCL	I²C Bus Clock
38	SDA	I²C Bus Data
39	GNDD	Digital Ground Supply
40	CIN_TV	Chroma Input from TV (SCART1 or external Cinch)
41	Y/CVBSIN_TV	Y/CVBS Input from TV (SCART1 or external Cinch)
42	DIGOUT1	Digital Output Pin 1
43	CIN_TUN	Chroma Input from Tuner
44	DIGOUT2	Digital Output Pin 2

Figure 2: STV6618 Input/Output Diagram

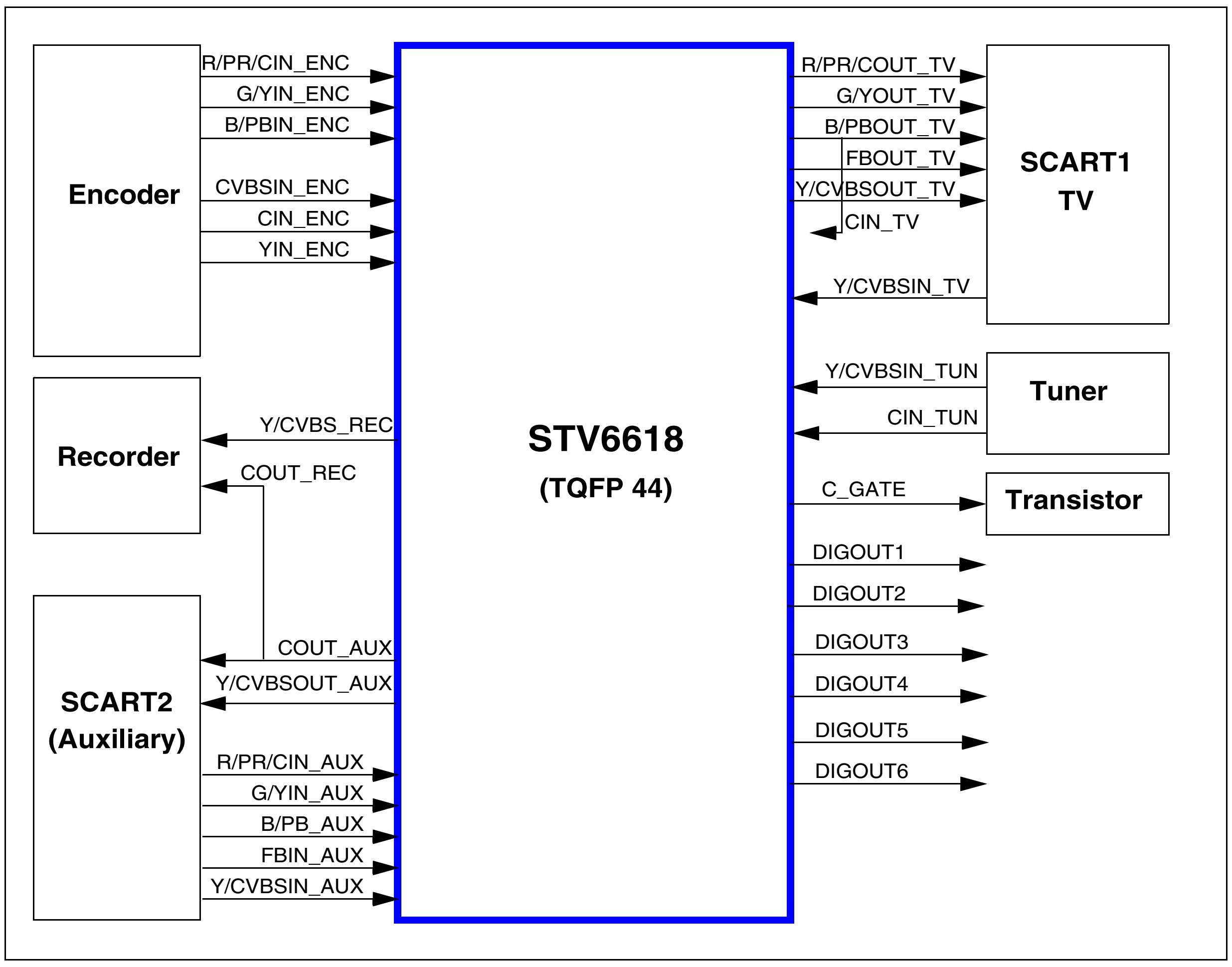
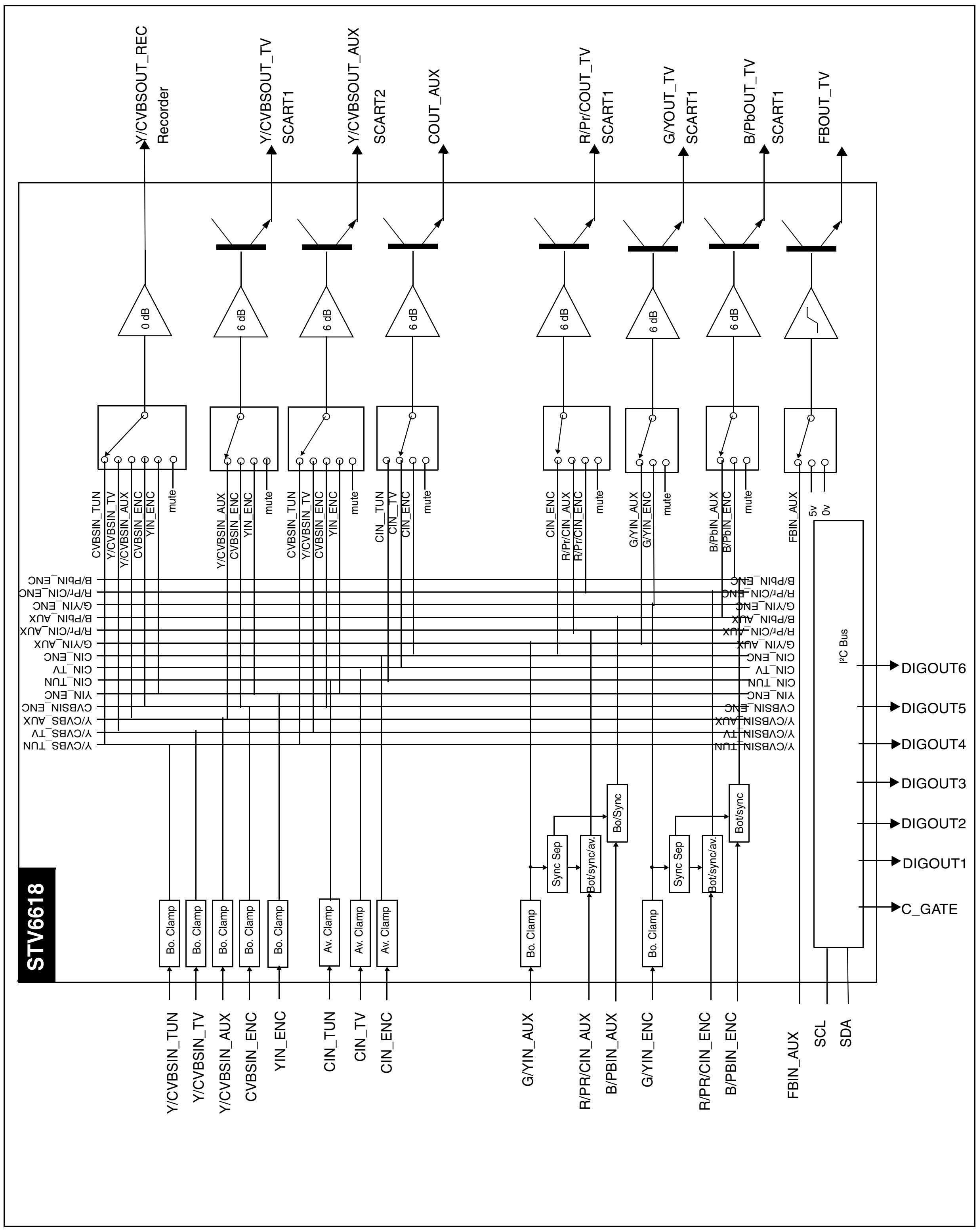

Encoder
R/PR/CIN_ENC
G/YIN_ENC
B/PBIN_ENC
CVBSIN_ENC
CIN_ENC
YIN_ENC
Recorder
Y/CVBS_REC
COUT_REC
SCART2 (Auxiliary)
COUT_AUX
Y/CVBSOUT_AUX
R/PR/CIN_AUX
G/YIN_AUX
B/PB_AUX
FBIN_AUX
Y/CVBSIN_AUX
STV6618
(TQFP 44)
R/PR/COUT_TV
G/YOUT_TV
B/PBOUT_TV
FBOUT_TV
Y/CVBSOUT_TV
CIN_TV
Y/CVBSIN_TV
SCART1 TV
Y/CVBSIN_TUN
CIN_TUN
Tuner
C_GATE
Transistor
DIGOUT1
DIGOUT2
DIGOUT3
DIGOUT4
DIGOUT5
DIGOUT6

Figure 3: STV6618 Block Diagram


STV6618
Y/CVBSOUT_REC
Recorder
Y/CVBSOUT_TV
SCART1
Y/CVBSOUT_AUX
SCART2
COUT_AUX
R/Pr/COUT_TV
SCART1
G/YOUT_TV
SCART1
B/PbOUT_TV
SCART1
FBOUT_TV
0 dB
6 dB
CVBSIN_TUN
Y/CVBSIN_TV
Y/CVBSIN_AUX
CVBSIN_ENC
YIN_ENC
mute
CIN_TUN
CIN_TV
CIN_ENC
R/Pr/CIN_AUX
R/Pr/CIN_ENC
G/YIN_AUX
G/YIN_ENC
B/PbIN_AUX
B/PbIN_ENC
FBIN_AUX
5v
0v
I²C Bus
Bo. Clamp
Av. Clamp
Sync Sep
Bot/sync/av
Bo/Sync
Bot/sync
DIGOUT6
DIGOUT5
DIGOUT4
DIGOUT3
DIGOUT2
DIGOUT1
C_GATE
Y/CVBSIN_TUN
Y/CVBSIN_TV
Y/CVBSIN_AUX
CVBSIN_ENC
YIN_ENC
CIN_TUN
CIN_TV
CIN_ENC
G/YIN_AUX
R/PR/CIN_AUX
B/PBIN_AUX
G/YIN_ENC
R/PR/CIN_ENC
B/PBIN_ENC
FBIN_AUX
SCL
SDA

IC7411

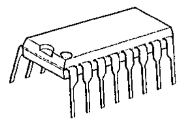
JRC **NJM2285**

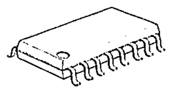
2-INPUT 3CHANNEL VIDEO SWITCH

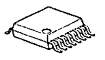
■ GENERAL DESCRIPTION

NJM2285 is a switching IC for switching over from one audio or video input signal to another. Internalizing 2 inputs, 1 output, and then each set of 3 can be operated independently. Two of them are Clamp type", and they can be operated while setting DC level fixed in position of the video signal. It is a higher efficiency video switch, featuring the operating supply voltage 5 to 12V, the frequency feature 10MHz, and then the crosstalk 75dB (at 4.43MHz).

■ PACKAGE OUTLINE


NJM2285D


NJM2285M


NJM2285V

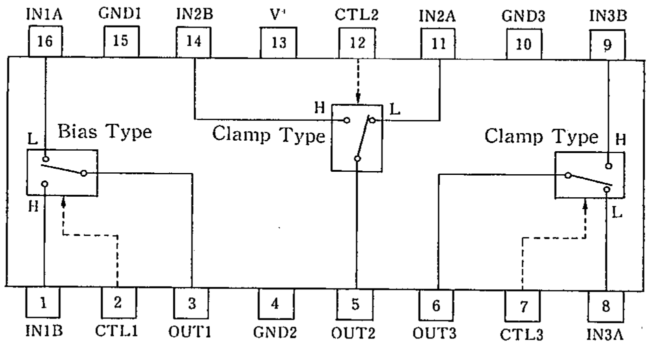
■ FEATURES

- 2 Input-1 Output
  Internalizing 3 Circuits (Two of them are Clamp type).
- Wide Operating Supply Voltage (4.75 ~ 13.0V)
- Crosstalk 75dB(at 4.43MHz)
- Wide Bandwidth Frequency Feature 10MHz(2V_{P-P} Input)
- Package Outline DIP16, DMP16, SSOP16
- Bipolar Technology

■ APPLICATIONS

- VCR, Video Camera, AV-TV, Video Disk Player.

■ BLOCK DIAGRAM


IN1A
GND1
IN2B
V+
CTL2
IN2A
GND3
IN3B
16
15
14
13
12
11
10
9
Bias Type
Clamp Type
Clamp Type
H
L
1
2
3
4
5
6
7
8
IN1B
CTL1
OUT1
GND2
OUT2
OUT3
CTL3
IN3A

NJM2285D
NJM2285M
NJM2285V

IC7313

GreenChip™II SMPS control IC TEA1507

FEATURES

Distinctive features

- Universal mains supply operation (70 to 276 V AC)
- High level of integration, giving a very low external component count.

Green features

- Valley/zero voltage switching for minimum switching losses
- Efficient quasi-resonant operation at high power levels
- Frequency reduction at low power standby for improved system efficiency (<3 W)
- Burst mode operation for very low standby levels (<1 W)
- On-chip start-up current source.

Protection features

- Safe restart mode for system fault conditions
- Continuous mode protection by means of demagnetization detection (zero switch-on current)
- Accurate and adjustable overvoltage protection
- Short winding protection
- Undervoltage protection (foldback during overload)
- Overtemperature protection
- Low and adjustable overcurrent protection trip level
- Soft (re)start
- Mains voltage-dependent operation-enabling level.

APPLICATIONS

Besides typical application areas, i.e. TV and Monitor supplies, the device can be used in all applications that demand an efficient and cost-effective solution up to 250 W.

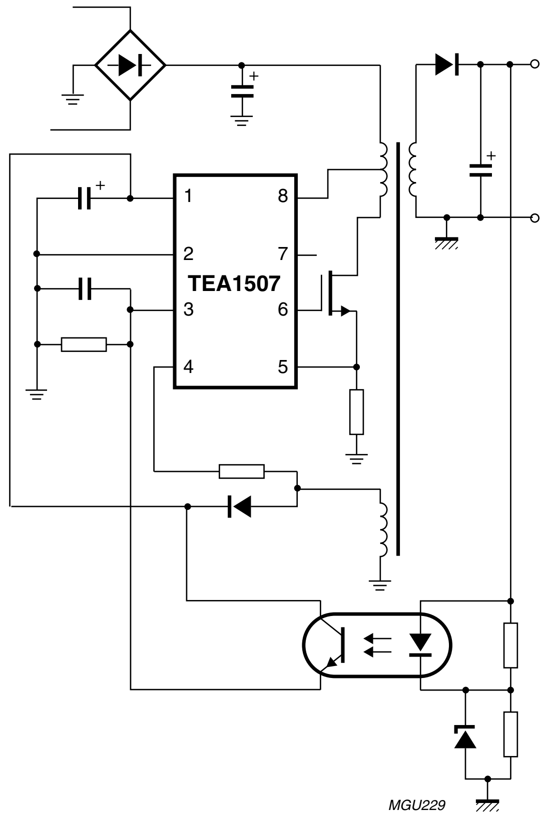


Fig.1 Typical application.

BLOCK DIAGRAM

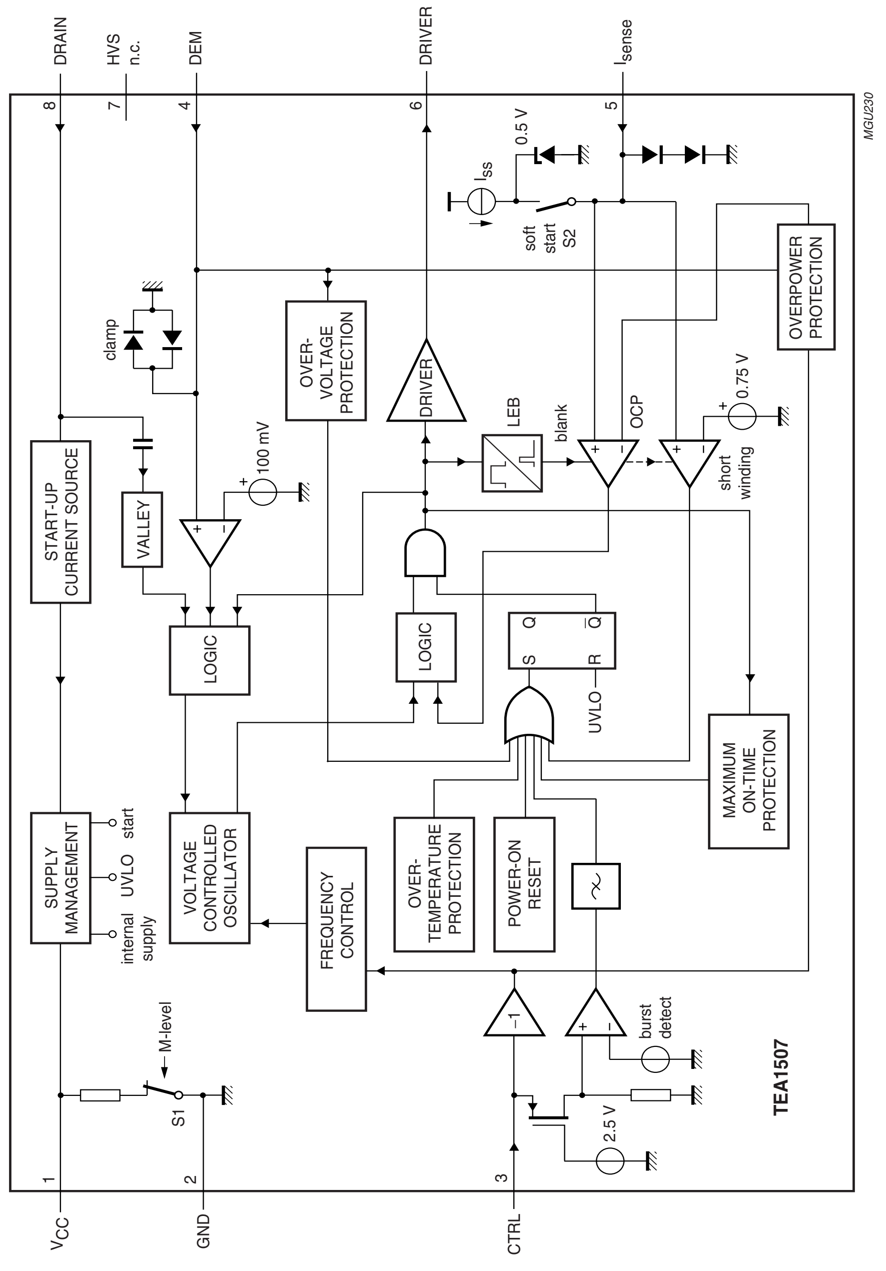

DRAIN
HVS
n.c.
DEM
DRIVER
I_{sense}
8
7
4
6
5
MGU230
0.5 V
I_{ss}
soft
start
S2
OVERPOWER
PROTECTION
clamp
OVER-
VOLTAGE
PROTECTION
DRIVER
LEB
blank
OCP
0.75 V
short
winding
100 mV
START-UP
CURRENT SOURCE
VALLEY
LOGIC
LOGIC
S
Q
R
$\overline{Q}$
UVLO
MAXIMUM
ON-TIME
PROTECTION
SUPPLY
MANAGEMENT
internal
supply
UVLO
start
VOLTAGE
CONTROLLED
OSCILLATOR
FREQUENCY
CONTROL
OVER-
TEMPERATURE
PROTECTION
POWER-ON
RESET
burst
detect
M-level
S1
−1
2.5 V
TEA1507
1
2
3
V_{CC}
GND
CTRL

Fig.2 Block diagram.

9.9 IC‘sUPC12 Sub PCB

9.9.1 IC7825

Ordering number:ENN2874A

Monolithic Linear IC

SANYO

LA7213

VCR-Use
Automatic Channel Selection Peripheral

Overview

The LA7213 is a VCR-use automatic channel selection peripheral IC that contains a sync separator and a vertical sync separator.

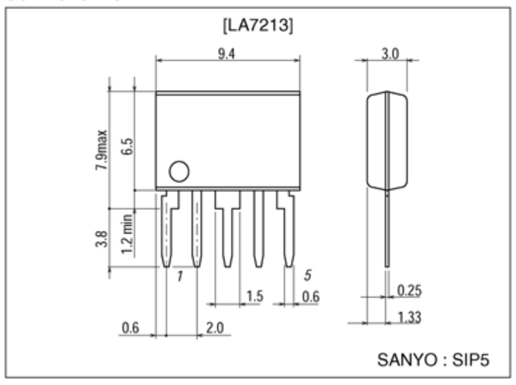
Functions and Features

- Sync separation.
- Vertical sync separation.
- Recommended supply voltage : 5V
- Open collector output (R_L=10k), negative polarity output.

Package Dimensions

unit:mm

3042C-SIP5



Specifications

Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7.0	V
Allowable power dissipation	Pd max	Ta 75˚C	100	mW
Operating temperature	Topr		–15 to +75	˚C
Storage temperature	Tstg		–40 to +125	˚C

Operating Conditions at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		5.0	V
Operating voltage	V_{CC} op		4 to 6	V

Operating Characteristics at Ta = 25˚C, V_{CC}=5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current	I_{CC}	No load	0.5	0.9	1.5	mA
Sync separation operating current	I_{SYNC}	SW1=b		85		μA
Sync separation minimum input level	V_I min	Color bar signal 1Vp-p=0dB, SW1=a		–12		dB
Vertical sync separation output time delay	TV_{OUT}	Color bar of input=1Vp-p, SW1=a	5	10	20	μs
Output DC level	V_{2H}	No load	4.9			V
Output DC level	V_{2L}	No load			0.2	V
Output DC level	V_{4H}	No load	4.9			V
Output DC level	V_{4L}	No load			0.2	V

■ Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft s control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.

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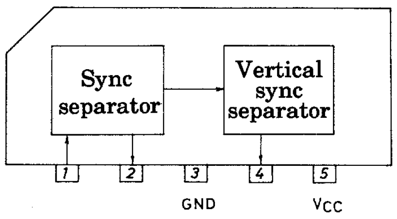
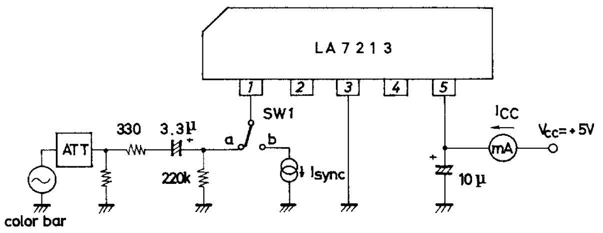
SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

LA7213

Block Diagram

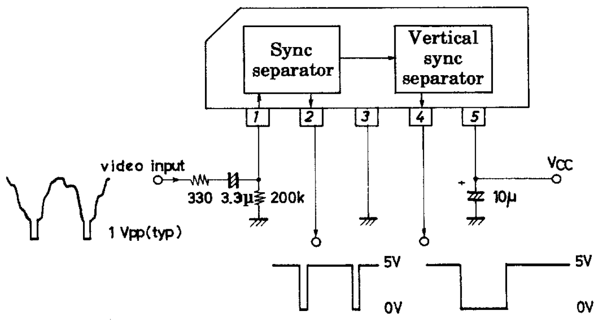


Test Circuit



Unit (resistance : Ω, capacitance : F)

Sample Application Circuit



Unit (resistance : Ω, capacitance : F)

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This catalog provides information as of April, 2000. Specifications and information herein are subject to change without notice.

IC7806

NCP300, NCP301

Voltage Detector Series

The NCP300 and NCP301 series are second generation ultra–low current voltage detectors. These devices are specifically designed for use as reset controllers in portable microprocessor based systems where extended battery life is paramount.

Each series features a highly accurate under voltage detector with hysteresis which prevents erratic system reset operation as the comparator threshold is crossed.

The NCP300 series consists of complementary output devices that are available with either an active high or active low reset output. The NCP301 series has an open drain N–channel output with either an active high or active low reset output.

The NCP300 and NCP301 device series are available in the Thin SOT–23–5 package with seven standard under voltage thresholds. Additional thresholds that range from 0.9 V to 4.9 V in 100 mV steps can be manufactured.

Features

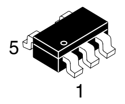
- Quiescent Current of 0.5 µA Typical
- High Accuracy Under Voltage Threshold of 2.0%
- Wide Operating Voltage Range of 0.8 V to 10 V
- Complementary or Open Drain Reset Output
- Active Low or Active High Reset Output

Typical Applications

- Microprocessor Reset Controller
- Low Battery Detection
- Power Fail Indicator
- Battery Backup Detection

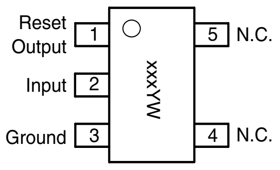
ON Semiconductor™

http://onsemi.com



THIN SOT–23–5
SN SUFFIX
CASE 483

PIN CONNECTIONS AND MARKING DIAGRAM

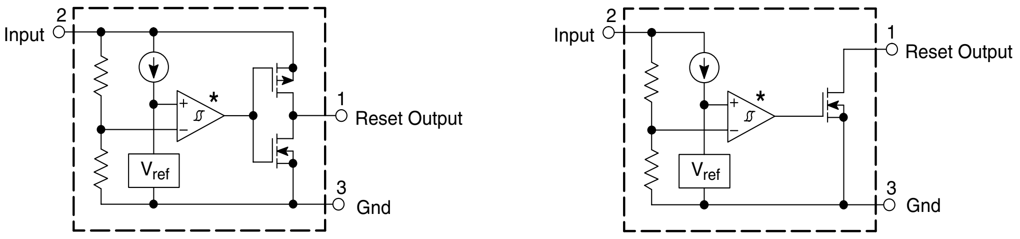


xxx = 300 or 301
Y = Year
W = Work Week

(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 23 of this data sheet.


NCP300xSNxxT1
Complementary Output Configuration

NCP301xSNxxT1
Open Drain Output Configuration

* The representative block diagrams depict active low reset output ‘L’ suffix devices. The comparator inputs are interchanged for the active high output ‘H’ suffix devices.

This device contains 25 active transistors.

Figure 1. Representative Block Diagrams

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August, 2001 – Rev. 9

NCP300, NCP301

OPERATING DESCRIPTION

The NCP300 and NCP301 series devices are second generation ultra–low current voltage detectors. Figures 21 and 22 show a timing diagram and a typical application. Initially consider that input voltage V_{in} is at a nominal level and it is greater than the voltage detector upper threshold (V_{DET+}), and the reset output (Pin 1) will be in the high state for active low devices, or in the low state for active high devices. If there is a power interruption and V_{in} becomes significantly deficient, it will fall below the lower detector threshold (V_{DET-}). This sequence of events causes the Reset output to be in the low state for active low devices, or in the high state for active high devices. After completion of the power interruption, V_{in} will again return to its nominal level and become greater than the V_{DET+}. The voltage detector has built–in hysteresis to prevent erratic reset operation as the comparator threshold is crossed.

Although these device series are specifically designed for use as reset controllers in portable microprocessor based systems, they offer a cost–effective solution in numerous applications where precise voltage monitoring is required. Figure 22 through Figure 29 shows various application examples.

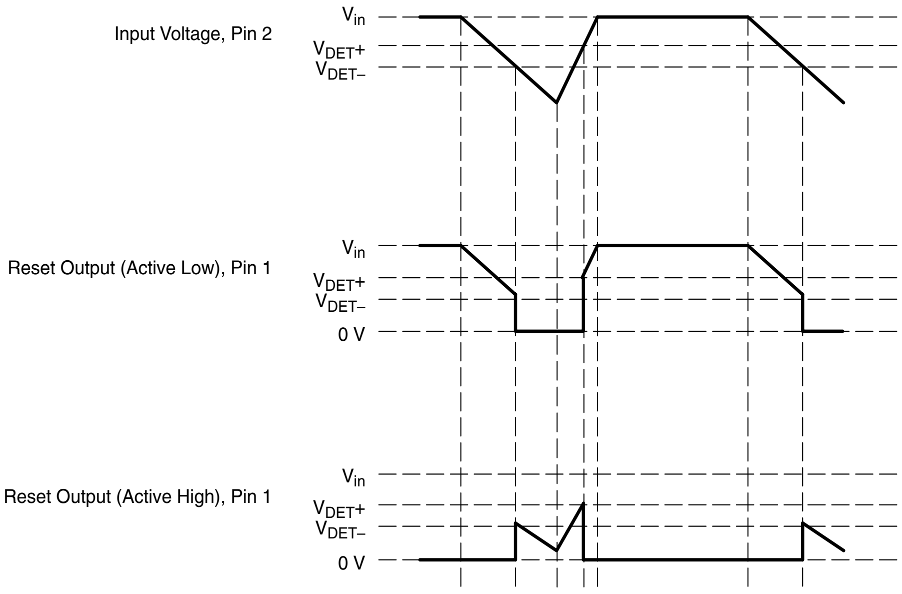

Input Voltage, Pin 2
Vin
VDET+
VDET–
Reset Output (Active Low), Pin 1
Vin
VDET+
VDET–
0 V
Reset Output (Active High), Pin 1
Vin
VDET+
VDET–
0 V

Figure 21. Timing Waveforms

9.10 IC's Digital Board

9.10.1 IC7100: VSM

VERSATILE STREAM MANAGER

GENERAL DESCRIPTION

The Versatile Stream Manager (VSM) is an ASIC used in the first generation DVD Video Recorder. Main function of the VSM is to interface directly to the different hardware modules such as Basic Engine, MPEG encoders, MPEG decoders and buffering the data streams that are coming from or going to these hardware modules.
The VSM contains a memory interface to support one 4M*16 SDRAM device. A host interface allows a CPU to directly access this memory and the VSM s internal registers.
Handling of data streams is done using scatter / gather DMA s under software control. Hardware support is provided in the VSM to support software MPEG AV multiplexing.

FEATURES

The VSM features include:

- SDRAM memory interface to support one 4 banks*1M*16 (64Mbit) SDRAM device.
- Glueless Host Interface for STM s STi5505.
- Glueless MPEG Decoder interface for STM s STi5505
- Glueless interface to Philips SAA6750 MPEG Video Encoder or SAA6752 MPEG AV Encoder.
- Glueless interface to Motorola s DSP56362 used as MPEG Audio Encoder.
- Glueless interface to Philips HDR65 as part of Basic Engine interface including the Sector Processor as also included in the STi5505.
- Audio Clock Control providing PLL loop and clock lock detection.
- Double Extraction of VBI decoded data from extended CCIR 656 stream.
- Double UART with hardware handshake and 8 byte Rx/Tx FIFO.
- Generation of additional Host Bus to support Audio Encoder DSP56362.
- Descriptor based DMA Controllers for data stream handling.
- Hardware support for software MPEG multiplex process.
- Internal Interrupt Controller to handle internal and 4 external interrupt sources.
- Operates from single 27 MHz clock input.
- JTAG for production tests.
- 3.3V logic core.
- 3.3V / 5V toleration IO pins.
- 208 PIN LQFP Package. (CR1087)

BLOCK DIAGRAM

Figure 2.1 shows the block diagram of the VSM. The hardware blocks can be divided in to three categories:

- General modules: Host Interface, Memory Interface, Interrupt Controller.
- DMA Controllers.
- Functional Interfaces; the link between the actual external hardware interface and the DMA Controller. Some Functional Interfaces have knowledge about the stream coming through in order to perform for example MPEG stream characteristics extraction and insertion.

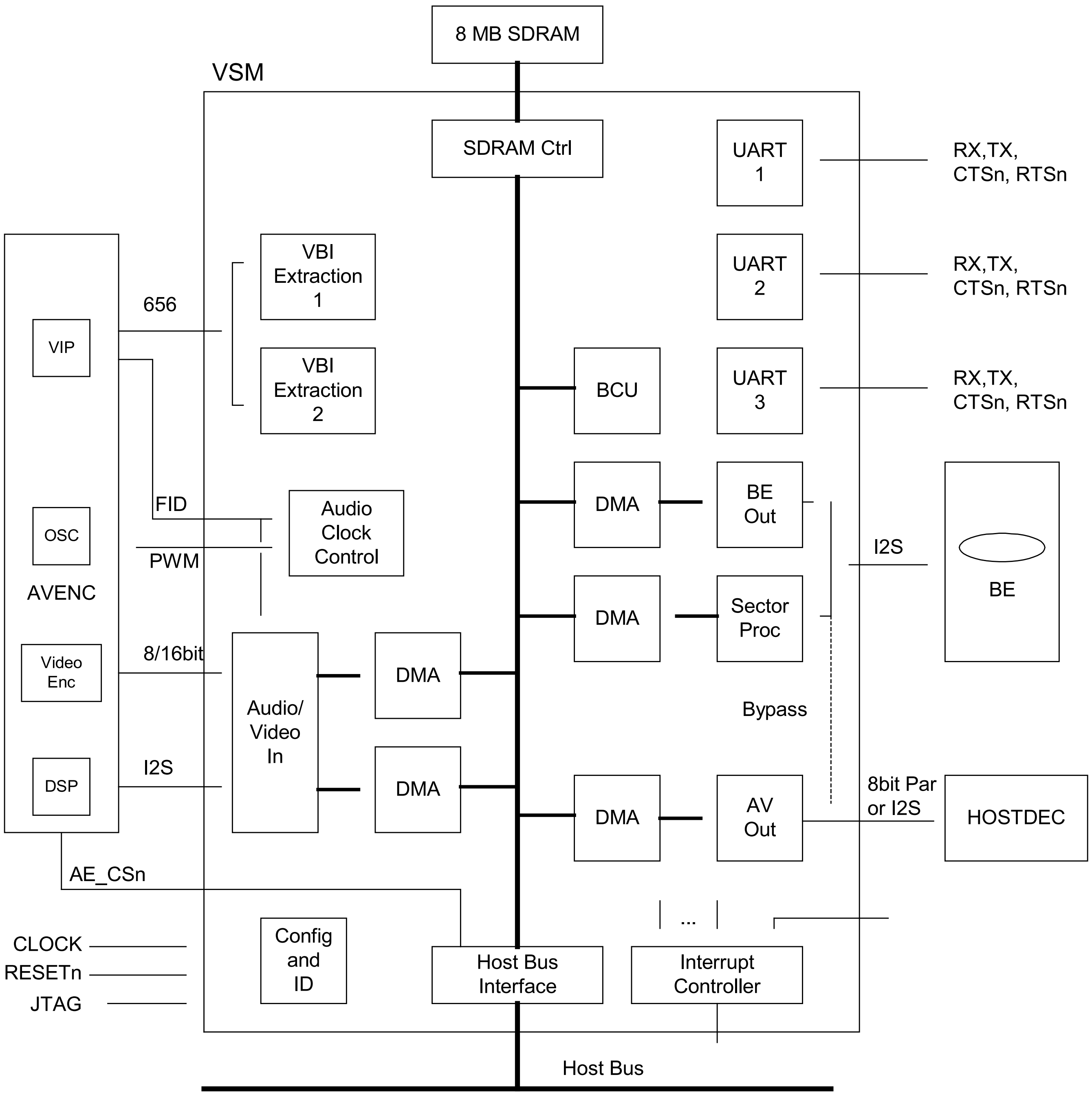

8 MB SDRAM
VSM
SDRAM Ctrl
UART 1
UART 2
UART 3
RX,TX, CTSn, RTSn
RX,TX, CTSn, RTSn
RX,TX, CTSn, RTSn
VBI Extraction 1
VBI Extraction 2
656
VIP
BCU
DMA
BE Out
I2S
BE
FID
Audio Clock Control
OSC
PWM
AVENC
DMA
Sector Proc
Video Enc
8/16bit
Audio/ Video In
DMA
Bypass
I2S
DSP
DMA
DMA
AV Out
8bit Par or I2S
HOSTDEC
AE_CSn
...
CLOCK
RESETn
JTAG
Config and ID
Host Bus Interface
Interrupt Controller
Host Bus

Figure 2.1: VSM Overview

PINNING

OVERVIEW

Name	Pins	Type	Function
System			
RESETn	1	In	
SYSCLK (27MHz)	1	In	
Host Interface			
HO_A(21:1)	21	In	
HO_D(15:0)	16	In/Out	
HO_BEn(1:0)	2	In	
HO_RWn	1	In	
HO_CSLn	1	In	
HO_CSHn	1	In	
HO_A22	1	In	
HO_WAIT	1	Out	
HO_PROCCLK	1	In	
Memory Interface			
M_A(13:0)	14	Out	
M_DQ(15:0)	16	In/Out	
M_RASn	1	Out	
M_CASn	1	Out	
M_WEn	1	Out	
M_LDQM	1	Out	
M_UDQM	1	Out	
M_CLKOUT	1	Out	
M_CLKEN	1	Out	
Basic Engine Interface			
BE_BCLK	1	In	
BE_DATI	1	In	
BE_WCLK	1	In	
BE_SYNC	1	In/Out	
BE_FLAG	1	In	
BE_V4	1	In	
BE_DATO	1	Out	
Video Encoder Interface			
VE_D(15:0)	16	In	
VE_DSn	1	Out	
VE_DTACKn	1	In	
VE_VIP_ERROR	1	In	Signal coming from SAA7114
Audio Encoder Interface			
AE_CSn	1	Out	
AE_BCLK	1	In/Out	(CR151,CR157)
AE_WCLK	1	In/Out	(CR151,CR157)
AE_DATA	1	In	(CR157)

Decoder Interface			
D_PAR_D(7:0)	8	Out	
D_PAR_DVALID	1	Out	
D_PAR_STR	1	Out	
D_PAR_REQ	1	In	
D_PAR_SYNC	1	Out	
D_WCLK	1	Out	
D_V4	1	Out	
Audio Clock Control			
ACC_FID	1	In	(CR200)
ACC_PWM	1	Out	
ACC_ACLK_OSC	1	In	
ACC_ACLK_DAI	1	In	
ACC_ACLK_PLL	1	In	
ACC_ACLK_DEC	1	Out	
VBI Extractor			
VBI_IPD(7:0)	8	In	
VBI_ICLK	1	In	
UART 1			
UART1_RX	1	In	
UART1_TX	1	Out (OC)	
UART1_CTSn	1	In	
UART1_RTSn	1	Out (OC)	
UART 2			
UART2_RX	1	In	
UART2_TX	1	Out (OC)	
UART2_CTSn	1	In	
UART2_RTSn	1	Out (OC)	
UART 3 (**VSM1B**)			
UART3_RX	1	In	
UART3_TX	1	Out	
UART3_CTSn	1	In	
UART3_RTSn	1	Out	
Interrupt Controller			
EXTINT(3:0)	4	In	From: VEnc, AEnc, BE, VSync (STi5505)
CPUINT(1:0)	2	Out (OC)	
JTAG			
TCK	1	In	Boundary Scan
TDI	1	In	
TDO	1	Out/Z	
TMS	1	In	
TRSTn	1	In	
Test			
TEST0	1	In	Amsal Test
TEST1	1	In	
Power Supply			
VDD	20	Power	10% of total pins package
VSS	20	Power	10% of total pins package

Total Pins	208		

9.10.2 IC7403: SAA6752H (EMPRESS)

1 FEATURES

1.1 Video input and preprocessing

- Digital YUV input according to *"ITU-R BT.656"* (8 bits at 27 MHz) and *"ITU-R BT.601"*
- Support of enhanced *"ITU-R BT.656"* input format containing decoded VBI data readable via I^{2}C-bus; Closed Caption (CC), Wide Screen Signalling (WSS) and copyright information [Copy Generation Management System (CGMS)]
- Processing of non broadcast video signals from analog VCR according to IEC 756
- Two video clock input pins for switching two digital video sources
- *"ITU-R BT.601"* format conversion to 1/2D1, 2/3D1 and Standard Interchange Format (SIF)
- 4 : 2 : 2 to 4 : 2 : 0 colour format conversion
- Decimation filtering for all format conversions
- Adaptive median filter and motion compensated filter for input noise reduction.

1.2 Video compression

- Real time MPEG-2 encoding compliant to Main Profile at Main Level (MP@ML) for 625 and 525 interlaced line systems
- Supported resolutions: D1, 2/3D1, 1/2D1 and SIF
- IPB frame, IP frame and I frame only encoding supported at all modes
- Supported bit rates: up to 25 Mbit/s I-only encoding; up to 15 Mbit/s IP-only or IBP encoding.
- Variable video bit rate mode for constant picture quality and constant bit rate mode to gain optimum picture quality from a fixed channel transfer rate
- Access to bit rate control parameters whilst encoding to support external real-time control algorithms (e.g. constrained variable bit rate control)
- Programmable Group Of Pictures (GOP) structure
- Innovative motion estimation with wide search range
- Adaptive quantization
- Motion compensated noise filter.

1.3 Audio input

- Audio inputs: I^{2}S format or EIAJ format (16, 18 or 20 bits), master or slave mode at 32, 44.1 and 48 kHz
- Two digital I^{2}S input ports for selection between two digital audio sources
- Audio clock generation: 256/384 × f_s (48 kHz) locked to video frame rate (if video is present)
- Sample rate conversion to 48 kHz (locked to video frame rate) for slave mode operation in all modes except Digital Versatile Disc (DVD) compliant bypass.

1.4 Audio compression

- Dolby®(1) Digital Consumer Encoding (DDCE) also known as AC-3(2) 2 channel audio encoding at 256 kbit/s or 384 kbit/s (only for SAA6752HS/01)
- MPEG-1 layer 2 audio encoding at 256 kbit/s or 384 kbit/s
- Input data bypass for Linear Pulse Code Modulation (LPCM) and compressed audio data [MPEG-1, MPEG-2, Dolby® Digital (DD) and Digital Theatre System (DTS)] according to IEC 61937
- Preamble Pc, Preamble Pd and bit stream information captured for identification of modes during bypass of compressed audio data for MPEG-1, MPEG-2, DD and DTS according to IEC 61937
- Audio mute via I^{2}C-bus control for all modes except DVD-compliant bypass.

1.5 Stream multiplexer

- Multiplexing of video and audio streams according to the MPEG-2 systems standard (*"ISO 13818-1"*)
- Generation and output of MPEG-2 Transport Streams (TS), MPEG-2 Program Streams (PS), Packetized Elementary Streams (PES) and Elementary Streams (ES) compliant to the DVD, D-VHS and DVB standards
- MPEG time stamp (PTS/DTS/SCR/PCR) generation and insertion (synchronization)
- Insertion of metadata
- Optional generation of empty time slots for subsequent insertion of application specific data packets
- Optional insertion of user data in the GOP header and in the picture header.

---

(1) Dolby is a registered trademark of Dolby Laboratories Licensing Corporation.

(2) AC-3 is a registered trademark of Dolby Laboratories Licensing Corporation.

1.6 Output interface

- Parallel interface 8-bit master/slave output
- 3-state output port
- Glueless interfacing with IEEE 1394 chip sets (for example, PDI 1394 L11)
- Data Expansion Bus Interface (DEBI) interface.

1.7 Control domain

- All control done via I^{2}C-bus
- I^{2}C-bus slave transceiver up to 400 kHz
- I^{2}C-bus slave address select pin
- Host interrupt flag pin.

1.8 Other features

- Single external clock or single crystal 27 MHz
- Separate 27 MHz system clock output
- Interface voltage 3.3 V
- TTL compatible digital outputs
- Power supply voltage 3.3 and 2.5 V
- Boundary Scan Test (BST) supported
- Power-down mode
- Single SDRAM system memory (16 Mbit@16 bit or 64 Mbit@16 bit).

2 GENERAL DESCRIPTION

2.1 General

Philips Semiconductors' second generation real time MPEG-2 encoder, the SAA6752HS, is a highly integrated single chip audio and video encoding solution with very flexible multiplexing functionality. With our expertise in two critical areas for consumer video encoding, noise filtering and motion estimation, we have pushed the boundaries for video quality even further, providing enhanced quality for low bit rates and enabling increased recording times for a given storage capacity. The SAA6752HS will also enable a key driver for new consumer digital recording applications; system cost reduction. By integrating all audio encoding and multiplexing functionality we will be moving from a three chip to a one chip system, with cost efficient design and process technology, thus providing a truly low cost, high quality encoding system.

The SAA6752HS/02 is intended for customers whose application does not require the DDCE function.

The SAA6752HS gives significant advantages to customers developing digital recording applications:

- **Fast time-to-market and low development resources**: By adding a simple external video input processor IC, audio analog-to-digital converter, and an external SDRAM, analog video and audio sources are compressed into high quality MPEG-2 video and MPEG-1 layer 2 or AC-3 audio streams, multiplexed into a single program or transport stream for simple connection to various storage media or broadcast media. Hence, making design effort for our customers a minimum, as well as removing the need for in-depth experience in MPEG encoding.
- **Low system host resources**: All video and audio encoding algorithms and software are run on an internal MIPS®(1) processor. The SAA6752HS only requires small amount of communication from system host processor to set up and control required encoding parameters via I^{2}C-bus.

2.2 Application ?elds

2.2.1 DVD BASED OPTICAL DISC RECORDERS (DVD+RW, DVD-RW, DVD-RAM)

Emerging optical disc based recording systems target to replace the existing consumer recording (VCR) and playback (DVD and VCD) products. The first generation recordable DVD based products will want to maximise recording times for the 4.7 Gbyte storage capacity. For these systems the SAA6752HS is critical, with its superior noise filtering and motion estimation, in enabling high quality at low bit rates.

Playback compatibility with existing DVD decoding solutions will also be important, which is why the SAA6752HS provides Dolby® digital consumer (AC-3) audio encoding to allow playback through existing players implementing DDCE (AC-3) decoding dominant in current DVD platforms.

The DVD stream is based on MPEG Program Stream (PS). The SAA6752HS directly outputs MPEG PS compliant to the DVD standard.

---

(1) MIPS is a registered trademark of MIPS Technologies.

2.2.2 HDD BASED TIME SHIFT RECORDING

Hard Disc Drive (HDD) based time-shift systems enable Personalized TV (PTV) functionality, providing consumers with new powers of control over what and when to watch broadcast content. With the audio and video content recorded digitally, identification, search and retrieval becomes a `no brainer' task as compared to traditional VCR functionality. Combine this with electronic program guides and intelligent control, and the PTV can also analyse the viewers watching habits to search for programs likely to be of interest and automatically recorded in anticipation of the viewers preferences.

Since HDD recorders are closed systems, the recording format stream can be proprietary. SAA6752HS flexible multiplexing formats, support a number of recording stream formats for HDD including MPEG Transport Stream (TS) or MPEG Packetized Elementary Stream (PES).

2.2.3 DIGITAL VCR (DVHS) RECORDING

A DVHS player records streams based on MPEG Transport Streams (TS) packed in logical tape tracks. The SAA6752HS output streams are compliant with DVHS standard requirements.

2.2.4 VIDEO EDITING/TRANSMISSION/SURVEILLANCE/CONFERENCING

The SAA6752HS can operate as a stand-alone device in all above applications. The SAA6752HS' full features and flexibility allows customers to tailor functionality and performance to specific application requirements. All required control settings such as GOP size and bit rate modes can be selected via I^{2}C-bus.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDP}	digital supply voltage (pad cells)	3.0	3.3	3.6	V
V_{DDCO}	digital supply voltage (core)	2.3	2.5	2.7	V
V_{DDA}	analog supply voltage (oscillator and PLL)	2.3	2.5	2.7	V
$I_{DD(tot)}$	analog + digital supply current	407	453	525	mA
P_{tot}	total power dissipation	1.2	1.4	1.9	W
f_{DCXO}	quartz frequency (digital controlled tuning)	$27 \times (1 - 200 \times 10^{-6})$	27	$27 \times (1 + 200 \times 10^{-6})$	MHz
f_{SDRAM}	SDRAM clock frequency	–	108	–	MHz
f_{SCL}	I^{2}C-bus input clock frequency	100	–	400	kHz
B	output bit-rate	1.5	–	25	Mbit/s
V_{IH}	HIGH-level digital input voltage	1.7	–	3.6	V
V_{IL}	LOW-level digital input voltage	–0.5	–	+0.7	V
V_{OH}	HIGH-level digital output voltage	$V_{DDP} - 0.4$	–	V_{DDP}	V
V_{OL}	LOW-level digital output voltage	0	–	0.4	V
T_{amb}	ambient temperature	0	–	70	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA6752HS/01(1)	SQFP208	plastic shrink quad ?at package; 208 leads (lead length 1.3 mm); body 28 × 28 × 3.4 mm; high stand-off height	SOT316-1
SAA6752HS/02(2)			

Notes

1. MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer.
2. MPEG-2 video and MPEG-audio encoder with multiplexer, but without AC-3 audio encoder.

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

5 BLOCK DIAGRAM

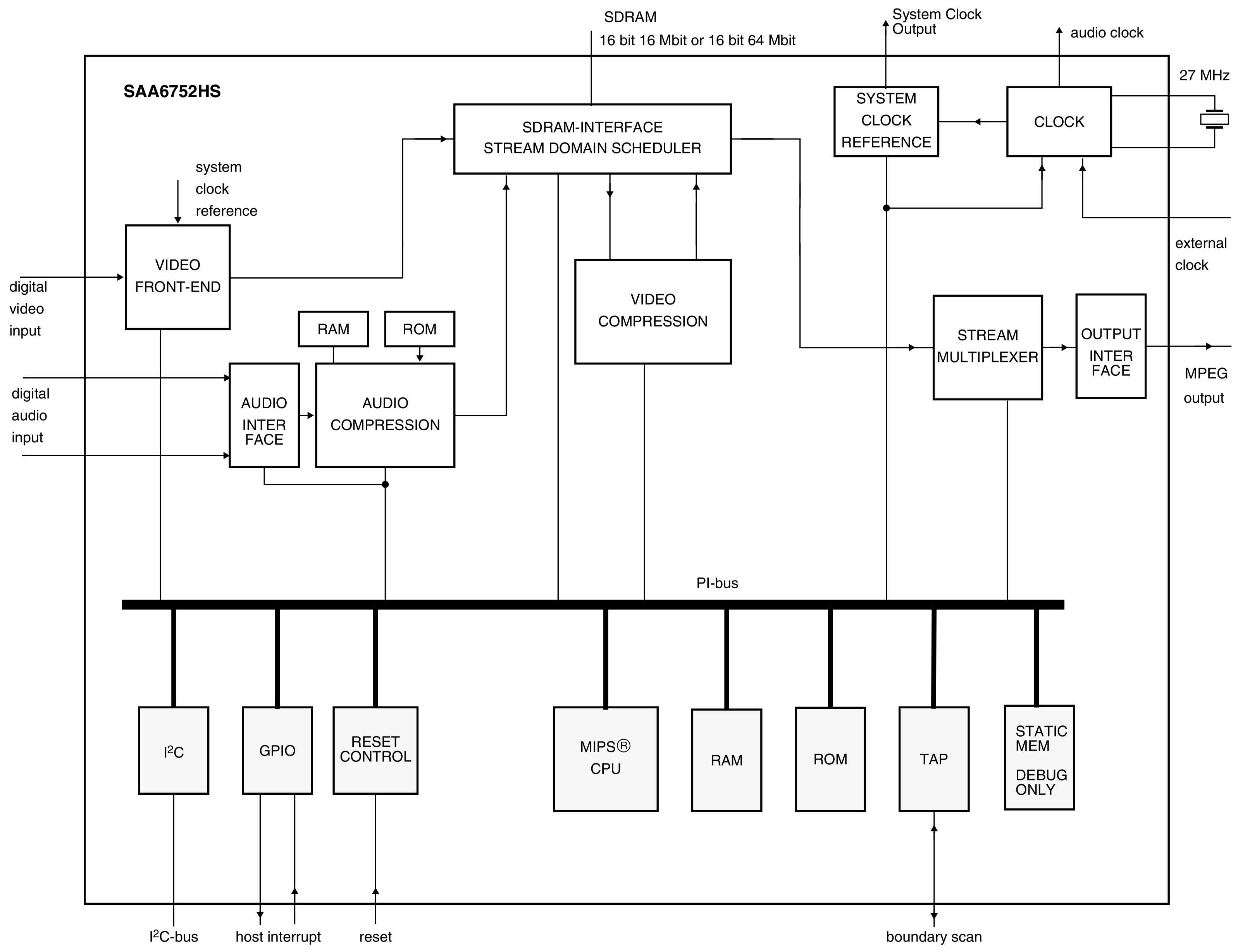

SDRAM
16 bit 16 Mbit or 16 bit 64 Mbit
System Clock Output
audio clock
27 MHz
SAA6752HS
SDRAM-INTERFACE STREAM DOMAIN SCHEDULER
SYSTEM CLOCK REFERENCE
CLOCK
external clock
system clock reference
VIDEO FRONT-END
digital video input
VIDEO COMPRESSION
STREAM MULTIPLEXER
OUTPUT INTER FACE
MPEG output
RAM
ROM
AUDIO INTER FACE
AUDIO COMPRESSION
digital audio input
PI-bus
I²C
GPIO
RESET CONTROL
MIPS® CPU
RAM
ROM
TAP
STATIC MEM DEBUG ONLY
I²C-bus
host interrupt
reset
boundary scan

Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	INPUT/OUTPUT(1)	I_{max} (mA)	DESCRIPTION
V_{SSP}	1	ground	–	pad ground
SDATA1	2	input	–	I^2S-bus serial data input port 1 with internal pull-down resistor
SCLK1	3	input/output	4	I^2S-bus serial clock port 1 with internal pull-down resistor
SWS1	4	input/output	4	I^2S-bus word select port 1 with internal pull-down resistor
V_{DDP}	5	supply	–	pad ring supply voltage (3.3 V)
SDATA2	6	input/output	4	I^2S-bus serial data port 2 with internal pull-down resistor
SCLK2	7	input/output	4	I^2S-bus serial clock port 2 with internal pull-down resistor
SWS2	8	input/output	4	I^2S-bus word select port 2 with internal pull-down resistor
ACLK	9	output	4	audio clock output ($256 \times f_s$ or $384 \times f_s$)
V_{SSP}	10	ground	–	pad ground
IDQ	11	input	–	reserved (recommended connect to pin V_{SSP}) with internal pull-down resistor
YUV0	12	input	–	video input signal bit 0 (LSB)
YUV1	13	input	–	video input signal bit 1
YUV2	14	input	–	video input signal bit 2
YUV3	15	input	–	video input signal bit 3
YUV4	16	input	–	video input signal bit 4
YUV5	17	input	–	video input signal bit 5
YUV6	18	input	–	video input signal bit 6
YUV7	19	input	–	video input signal bit 7 (MSB)
V_{SSP}	20	ground	–	pad ground
HSYNC	21	input	–	horizontal sync input (video) with internal pull-down resistor
VSYNC	22	input	–	vertical sync input (video) with internal pull-down resistor
FID	23	input	–	video ?eld identi?cation input (odd/even ?eld) with internal pull-down resistor
VCLK1	24	input	–	video clock input 1 (27 MHz) with internal pull-down resistor
V_{SSCO}	25	ground	–	core ground
V_{SSCO}	26	ground	–	core ground
V_{DDCO}	27	supply	–	core supply voltage (2.5 V)
V_{DDCO}	28	supply	–	core supply voltage (2.5 V)
V_{DDP}	29	supply	–	pad ring supply voltage (3.3 V)
VCLK2	30	input	–	video clock input 2 (27 MHz) with internal pull-down resistor
PDOAV	31	3-state output	4	parallel stream data output for audio/video identi?er
PDIDS	32	input	–	parallel stream data input for data strobe (request for packet in Data Expansion Bus Interface (DEBI) slave mode) with internal pull-up resistor
PDOSYNC	33	3-state output	4	parallel stream data output for packet sync
V_{SSP}	34	ground	–	pad ground
PDOVAL	35	3-state output	4	parallel stream data valid output with internal pull-up resistor
PDO0	36	3-state output	4	parallel stream data output bit 0 (LSB)

SYMBOL	PIN	INPUT/OUTPUT(1)	I_{max} (mA)	DESCRIPTION
PDO1	37	3-state output	4	parallel stream data output bit 1
PDO2	38	3-state output	4	parallel stream data output bit 2
V_{DDP}	39	supply	–	pad ring supply voltage (3.3 V)
PDO3	40	3-state output	4	parallel stream data output bit 3
PDO4	41	3-state output	4	parallel stream data output bit 4
PDO5	42	3-state output	4	parallel stream data output bit 5
PDO6	43	3-state output	4	parallel stream data output bit 6
V_{SSP}	44	ground	–	pad ground
PDO7	45	3-state output	4	parallel stream data output bit 7 (MSB)
PDIOCLK	46	input/output	4	parallel stream clock input/output
I2CADDRSEL	47	input	–	I^{2}C-bus address select input with internal pull-up resistor
SD_DQ15	48	input/output	8	SDRAM data input/output bit 15 (MSB)
V_{DDP}	49	supply	–	pad ring supply voltage (3.3 V)
SD_DQ0	50	input/output	8	SDRAM data input/output bit 0 (LSB)
SD_DQ14	51	input/output	8	SDRAM data input/output bit 14
SD_DQ1	52	input/output	8	SDRAM data input/output bit 1
V_{SSP}	53	ground	–	pad ground
SD_DQ13	54	input/output	8	SDRAM data input/output bit 13
SD_DQ2	55	input/output	8	SDRAM data input/output bit 2
SD_DQ12	56	input/output	8	SDRAM data input/output bit 12
V_{DDP}	57	supply	–	pad ring supply voltage (3.3 V)
SD_DQ3	58	input/output	8	SDRAM data input/output bit 3
SD_DQ11	59	input/output	8	SDRAM data input/output bit 11
SD_DQ4	60	input/output	8	SDRAM data input/output bit 4
SD_DQ10	61	input/output	8	SDRAM data input/output bit 10
V_{SSP}	62	ground	–	pad ground
SD_DQ5	63	input/output	8	SDRAM data input/output bit 5
SD_DQ9	64	input/output	8	SDRAM data input/output bit 9
SD_DQ6	65	input/output	8	SDRAM data input/output bit 6
SD_DQ8	66	input/output	8	SDRAM data input/output bit 8
V_{DDP}	67	supply	–	pad ring supply voltage (3.3 V)
SD_DQ7	68	input/output	8	SDRAM data input/output bit 7
SD_DQM1	69	output	8	SDRAM data mask enable output bit 1
SD_DQM0	70	output	8	SDRAM data mask enable output bit 0 (LSB)
$\overline{\text{SD\_WE}}$	71	output	8	SDRAM write enable output (active LOW)
V_{SSP}	72	ground	–	pad ground
$\overline{\text{SD\_CAS}}$	73	output	8	SDRAM column address strobe output (active LOW)
SD_CLK	74	output	8	SDRAM clock output
$\overline{\text{SD\_RAS}}$	75	output	8	SDRAM row address strobe output (active LOW)
SD_CKE	76	output	8	SDRAM clock enable output

SYMBOL	PIN	INPUT/OUTPUT(1)	I_{max} (mA)	DESCRIPTION
V_{SSCO}	77	ground	–	core ground
V_{SSCO}	78	ground	–	core and substrate ground
V_{DDCO}	79	supply	–	core supply voltage (2.5 V)
V_{DDCO}	80	supply	–	core supply voltage (2.5 V)
V_{DDP}	81	supply	–	pad ring supply voltage (3.3 V)
$\overline{\text{SD\_CS}}$	82	output	8	SDRAM chip select output (active LOW)
SD_A13	83	output	8	SDRAM address output bit 13 (bank selection for 64 Mbit)
SD_A9	84	output	8	SDRAM address output bit 9
SD_A8	85	output	8	SDRAM address output bit 8
V_{SSP}	86	ground	–	pad ground
SD_A11	87	output	8	SDRAM address output bit 11 (bank selection for 16 Mbit)
SD_A7	88	output	8	SDRAM address output bit 7
SD_A12	89	output	8	SDRAM address output bit 12 (bank selection for 64 Mbit)
SD_A6	90	output	8	SDRAM address output bit 6
V_{DDP}	91	supply	–	pad ring supply voltage (3.3 V)
SD_A10	92	output	8	SDRAM address output bit 10
SD_A5	93	output	8	SDRAM address output bit 5
SD_A0	94	output	8	SDRAM address output bit 0 (LSB)
SD_A4	95	output	8	SDRAM address output bit 4
V_{SSP}	96	ground	–	pad ground
SD_A1	97	output	8	SDRAM address output bit 1
SD_A3	98	output	8	SDRAM address output bit 3
SD_A2	99	output	8	SDRAM address output bit 2
SD_DQM3	100	output	8	reserved (do not connect)
V_{DDP}	101	supply	–	pad ring supply voltage (3.3 V)
SD_DQM2	102	output	8	reserved (do not connect)
SD_DQ31	103	input/output	8	reserved (do not connect)
SD_DQ16	104	input/output	8	reserved (do not connect)
V_{SSP}	105	ground	–	pad ground
SD_DQ30	106	input/output	8	reserved (do not connect)
SD_DQ17	107	input/output	8	reserved (do not connect)
SD_DQ29	108	input/output	8	reserved (do not connect)
V_{DDP}	109	supply	–	pad ring supply voltage (3.3 V)
SD_DQ18	110	input/output	8	reserved (do not connect)
SD_DQ28	111	input/output	8	reserved (do not connect)
SD_DQ19	112	input/output	8	reserved (do not connect)
SD_DQ27	113	input/output	8	reserved (do not connect)
V_{SSP}	114	ground	–	pad ground
SD_DQ20	115	input/output	8	reserved (do not connect)
SD_DQ26	116	input/output	8	reserved (do not connect)

SYMBOL	PIN	INPUT/OUTPUT(1)	I_{max} (mA)	DESCRIPTION
V_{SSCO}	77	ground	–	core ground
V_{SSCO}	78	ground	–	core and substrate ground
V_{DDCO}	79	supply	–	core supply voltage (2.5 V)
V_{DDCO}	80	supply	–	core supply voltage (2.5 V)
V_{DDP}	81	supply	–	pad ring supply voltage (3.3 V)
$\overline{\text{SD\_CS}}$	82	output	8	SDRAM chip select output (active LOW)
SD_A13	83	output	8	SDRAM address output bit 13 (bank selection for 64 Mbit)
SD_A9	84	output	8	SDRAM address output bit 9
SD_A8	85	output	8	SDRAM address output bit 8
V_{SSP}	86	ground	–	pad ground
SD_A11	87	output	8	SDRAM address output bit 11 (bank selection for 16 Mbit)
SD_A7	88	output	8	SDRAM address output bit 7
SD_A12	89	output	8	SDRAM address output bit 12 (bank selection for 64 Mbit)
SD_A6	90	output	8	SDRAM address output bit 6
V_{DDP}	91	supply	–	pad ring supply voltage (3.3 V)
SD_A10	92	output	8	SDRAM address output bit 10
SD_A5	93	output	8	SDRAM address output bit 5
SD_A0	94	output	8	SDRAM address output bit 0 (LSB)
SD_A4	95	output	8	SDRAM address output bit 4
V_{SSP}	96	ground	–	pad ground
SD_A1	97	output	8	SDRAM address output bit 1
SD_A3	98	output	8	SDRAM address output bit 3
SD_A2	99	output	8	SDRAM address output bit 2
SD_DQM3	100	output	8	reserved (do not connect)
V_{DDP}	101	supply	–	pad ring supply voltage (3.3 V)
SD_DQM2	102	output	8	reserved (do not connect)
SD_DQ31	103	input/output	8	reserved (do not connect)
SD_DQ16	104	input/output	8	reserved (do not connect)
V_{SSP}	105	ground	–	pad ground
SD_DQ30	106	input/output	8	reserved (do not connect)
SD_DQ17	107	input/output	8	reserved (do not connect)
SD_DQ29	108	input/output	8	reserved (do not connect)
V_{DDP}	109	supply	–	pad ring supply voltage (3.3 V)
SD_DQ18	110	input/output	8	reserved (do not connect)
SD_DQ28	111	input/output	8	reserved (do not connect)
SD_DQ19	112	input/output	8	reserved (do not connect)
SD_DQ27	113	input/output	8	reserved (do not connect)
V_{SSP}	114	ground	–	pad ground
SD_DQ20	115	input/output	8	reserved (do not connect)
SD_DQ26	116	input/output	8	reserved (do not connect)

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

SYMBOL	PIN	INPUT/OUTPUT(1)	I_{max} (mA)	DESCRIPTION
SD_DQ21	117	input/output	8	reserved (do not connect)
SD_DQ25	118	input/output	8	reserved (do not connect)
V_{DDP}	119	supply	–	pad ring supply voltage (3.3 V)
SD_DQ22	120	input/output	8	reserved (do not connect)
SD_DQ24	121	input/output	8	reserved (do not connect)
SD_DQ23	122	input/output	8	reserved (do not connect)
EXTCLK	123	input	–	27 MHz external clock input with internal pull-up resistor
V_{SSP}	124	ground	–	pad ground
V_{SSA}	125	ground	–	oscillator analog ground
XTALI	126	analog input	–	crystal oscillator input (27 MHz); note 2
XTALO	127	analog output	–	crystal oscillator output (27 MHz)
V_{DDA}	128	supply	–	oscillator analog supply voltage (2.5 V)
V_{SSCO}	129	ground	–	core ground
V_{SSCO}	130	ground	–	core ground
V_{DDCO}	131	supply	–	core supply voltage (2.5 V)
V_{DDCO}	132	supply	–	core supply voltage (2.5 V)
V_{DDP}	133	supply	–	pad ring supply voltage (3.3 V)
TDI	134	input	–	boundary scan test data input; pin must ?oat or set to HIGH during normal operating; with internal pull-up resistor; note 3
TMS	135	input	–	boundary scan test mode select; pin must ?oat or set to HIGH during normal operating; with internal pull-up resistor; note 3
TCK	136	input	–	boundary scan test clock; pin must be set to LOW during normal operating; with internal pull-up resistor; note 3
TDO	137	3-state output	4	boundary scan test data output; pin not active during normal operating; with 3-state output; note 3
V_{SSP}	138	ground	–	pad ground
$\overline{TRST}$	139	input	–	test reset input (active LOW), for boundary scan test (with internal pull-up); notes 3 and 4
CLKOUT	140	output	4	27 MHz system clock output
TEST0	141	input/output	4	reserved (do not connect)
TEST1	142	input/output	4	reserved (do not connect)
V_{DDP}	143	supply	–	pad ring supply voltage (3.3 V)
TEST2	144	input/output	4	reserved (do not connect)
SDA	145	input/open-drain output	–	serial data input/output (I^{2}C-bus)
SCL	146	input/open-drain output	–	serial clock input/output (I^{2}C-bus)
$\overline{RESET}$	147	input	–	reset input (active LOW); with internal pull-up resistor
V_{SSP}	148	ground	–	pad ground
$\overline{RTS}$	149	output	4	reserved (do not connect); Universal Asynchronous Receiver/Transmitter (UART) request to send output (active LOW)

SYMBOL	PIN	INPUT/OUTPUT[1]	I_{max} (mA)	DESCRIPTION
$\overline{\text{CTS}}$	150	input	–	reserved (recommended connect to pin V_{DDP}); UART clear to send input; external static memory select input (active LOW); with internal pull-up resistor
RXD	151	input	–	reserved (recommended connect to pin V_{DDP}); UART receive data; internal boot select input; with internal pull-up resistor
TXD	152	output	4	reserved (do not connect); UART transmit data
V_{DDP}	153	supply	–	pad ring supply voltage (3.3 V)
$\overline{\text{SM\_LB}}$	154	input/output	4	reserved (do not connect)
$\overline{\text{SM\_UB}}$	155	input/output	4	reserved (do not connect)
H_IRF	156	3-state output	4	host interrupt flag output; with internal pull-up resistor
V_{SSP}	157	ground	–	pad ground
$\overline{\text{SM\_OE}}$	158	output	4	reserved (do not connect), static memory output enable output (active LOW)
SM_A9	159	output	4	reserved (do not connect), static memory address output bit 9
SM_A10	160	output	4	reserved (do not connect), static memory address output bit 10
V_{DDP}	161	supply	–	pad ring supply voltage (3.3 V)
SM_A8	162	output	4	reserved (do not connect), static memory address output bit 8
SM_A11	163	output	4	reserved (do not connect), static memory address output bit 11
SM_A7	164	output	4	reserved (do not connect), static memory address output bit 7
SM_A12	165	output	4	reserved (do not connect), static memory address output bit 12
V_{SSP}	166	ground	–	pad ground
SM_A6	167	output	4	reserved (do not connect), static memory address output bit 6
SM_A13	168	output	4	reserved (do not connect), static memory address output bit 13
SM_A5	169	output	4	reserved (do not connect), static memory address output bit 5
SM_A14	170	output	4	reserved (do not connect), static memory address output bit 14
V_{DDP}	171	supply	–	pad ring supply voltage (3.3 V)
$\overline{\text{SM\_WE}}$	172	output	4	reserved (do not connect), static memory write enable output (active LOW)
SM_D7	173	input/output	4	reserved (do not connect), static memory data input/output bit 7 with internal pull-down resistor
SM_D8	174	input/output	4	reserved (do not connect), static memory data input/output bit 8 with internal pull-down resistor
SM_D6	175	input/output	4	reserved (do not connect), static memory data input/output bit 6 with internal pull-down resistor
V_{SSP}	176	ground	–	pad ground
SM_D9	177	input/output	4	reserved (do not connect), static memory data input/output bit 9 with internal pull-down resistor
SM_D5	178	input/output	4	reserved (do not connect), static memory data input/output bit 5 with internal pull-down resistor
SM_D10	179	input/output	4	reserved (do not connect), static memory data input/output bit 10 with internal pull-down resistor

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

SYMBOL	PIN	INPUT/OUTPUT(1)	I_{max} (mA)	DESCRIPTION
SM_D4	180	input/output	4	reserved (do not connect), static memory data input/output bit 4 with internal pull-down resistor
V_{SSCO}	181	ground	–	internal pre-driver and substrate ground
V_{SSCO}	182	ground	–	core ground
V_{DDCO}	183	supply	–	core supply voltage (2.5 V)
V_{DDCO}	184	supply	–	internal pre-driver supply voltage (2.5 V)
V_{DDP}	185	supply	–	pad ring supply voltage (3.3 V)
SM_D11	186	input/output	4	reserved (do not connect), static memory data input/output bit 11 with internal pull-down resistor
SM_D3	187	input/output	4	reserved (do not connect), static memory data input/output bit 3 with internal pull-down resistor
SM_D12	188	input/output	4	reserved (do not connect), static memory data input/output bit 12 with internal pull-down resistor
SM_D2	189	input/output	4	reserved (do not connect), static memory data input/output bit 2 with internal pull-down resistor
V_{SSP}	190	ground	–	pad ground
SM_D13	191	input/output	4	reserved (do not connect), static memory data input/output bit 13 with internal pull-down resistor
SM_D1	192	input/output	4	reserved (do not connect), static memory data input/output bit 1 with internal pull-down resistor
SM_D14	193	input/output	4	reserved (do not connect), static memory data input/output bit 14 with internal pull-down resistor
SM_D0	194	input/output	4	reserved (do not connect), static memory data input/output bit 0 (LSB) with internal pull-down resistor
V_{DDP}	195	supply	–	pad ring supply voltage (3.3 V)
SM_D15	196	input/output	4	reserved (do not connect), static memory data input/output bit 15 (MSB) with internal pull-down resistor
$\overline{SM\_CS3}$	197	output	4	reserved (do not connect), static memory chip select output for external ROM or RAM (active LOW)
SM_A4	198	output	4	reserved (do not connect), static memory address output bit 4
SM_A3	199	output	4	reserved (do not connect), static memory address output bit 3
V_{SSP}	200	ground	–	pad ground
SM_A2	201	output	4	reserved (do not connect), static memory address output bit 2
SM_A15	202	output	4	reserved (do not connect), static memory address output bit 15
SM_A1	203	output	4	reserved (do not connect), static memory address output bit 1
SM_A16	204	output	4	reserved (do not connect), static memory address output bit 16
V_{DDP}	205	supply	–	pad ring supply voltage (3.3 V)
SM_A0	206	output	4	reserved (do not connect), static memory address output bit 0 (LSB)
SM_A17	207	output	4	reserved (do not connect), static memory address output bit 17 (MSB)
$\overline{SM\_CS0}$	208	output	4	reserved (do not connect)

IC7700:FLI2200

FLI2200

Description

The FLI2200 is a single chip implementation of Faroudja Laboratories' award winning deinterlacing and post-processing algorithms that produce the highest quality progressive video output from a variety of interlaced video inputs including 525/60 (NTSC) or 625/50 (PAL or SECAM). It uses patented and patent pending motion-adaptive deinterlacing that selects the optimal filtering on a per-pixel basis. This includes detection and proper interleaving of 3:2 and 2:2 pulldown for film-base sources, including continuous monitoring and compensation for bad edits that occur frequently in broadcast material due to poor scene cuts or insertion of commercials. Video material is processed by a set of content-sensitive spatio-temporal filters that adapt to the appropriate direction for smoothest interpolation using the patented Faroudja DCDi™ algorithm. The FLI2200 also includes motion-adaptive cross-color suppression that removes highly objectionable coloration artifacts produced by commonly used video decoders. Its internal processing uses 10 bits per channel to maintain the highest quality. Its inputs and outputs are 10 bits/channel for best quality but also supports 8 bits/channel for more cost-sensitive applications. The FLI2200 requires 4 MB of low cost SDRAM for best quality deinterlacing, but it can also be operated in an optimized intra-field mode without memory for more cost-sensitive applications. This makes possible the use of a single design for both high-end and low-end applications.

The FLI2200 integrates a number of functions to provide maximum flexibility in a low cost configuration. This includes an on-chip clock generator, SDRAM controller, display controller, input and output color-space converters. It uses a standard 2-wire serial control interface for easy control and access to the registers.

The FLI2200 can be connected without glue logic to the FLI2000 video decoder and FLI2220 Enhancer and OSD Generator to produce the highest quality video pipeline for premium applications. It is also fully compatible with other decoders having a ITU-R BT 656 output format.

Applications

Flat panel TV – LCD, PDP

Progressive scan TVs

Multimedia front/rear projectors

Home Theater

Scan Converters

Multimedia PCs/Workstations

DCDi™ is a Faroudja trademark

Features

Motion-adaptive cross-color suppression removes artifacts produced by improper Y/C separation in low-cost video decoders

Motion-adaptive video deinterlacing selects optimal filtering on a per-pixel basis

- Film-mode for proper handling of 3:2 and 2:2 pulldown material
- Bad-edit detection/correction compensates for poor scene cuts and insertions common in broadcast material
- Motion-weighted interpolation for video sources produces maximum resolution without introducing motion artifacts
- Directional Correlational Deinterlacing (DCDi™) minimizes jaggies on angled lines

8/10-bit Y/Cb/Cr (D1) (ITU-R BT 656), 16/20-bit Y Cb/Cr (ITU-R BT 601), 24/30-bit RGB or YCbCr/YPbPr interlaced input options

? Supports 525/60 (NTSC), 625/50 (PAL/SECAM)

? Accepts up to 1100 pixels/line

8/10-bit, 16/20-bit YUV, 24/30-bit RGB or YCbCr/YPbPr progressive output options

Supports 8- or 10-bit inputs and outputs

10-bit internal processing for highest quality

Includes color-space converters at input and output for maximum flexibility

Auto-detection of NTSC/PAL/SECAM inputs

High-order filtering produces smooth chroma output in 4:2:2 to 4:4:4 or 4:4:4 to 4:2:2 conversions

Resolution recovery maximizes output signal-to-noise ratio and dynamic range

Can be operated without glue logic with FLI2000 Video Decoder and FLI2220 Enhancer and OSD Generator ICs to produce highest quality video pipeline

Glue-less interface to most standard video decoders

Built-in display timing generator

On-chip clock generator eliminates external PLLs

On-chip SDRAM controller

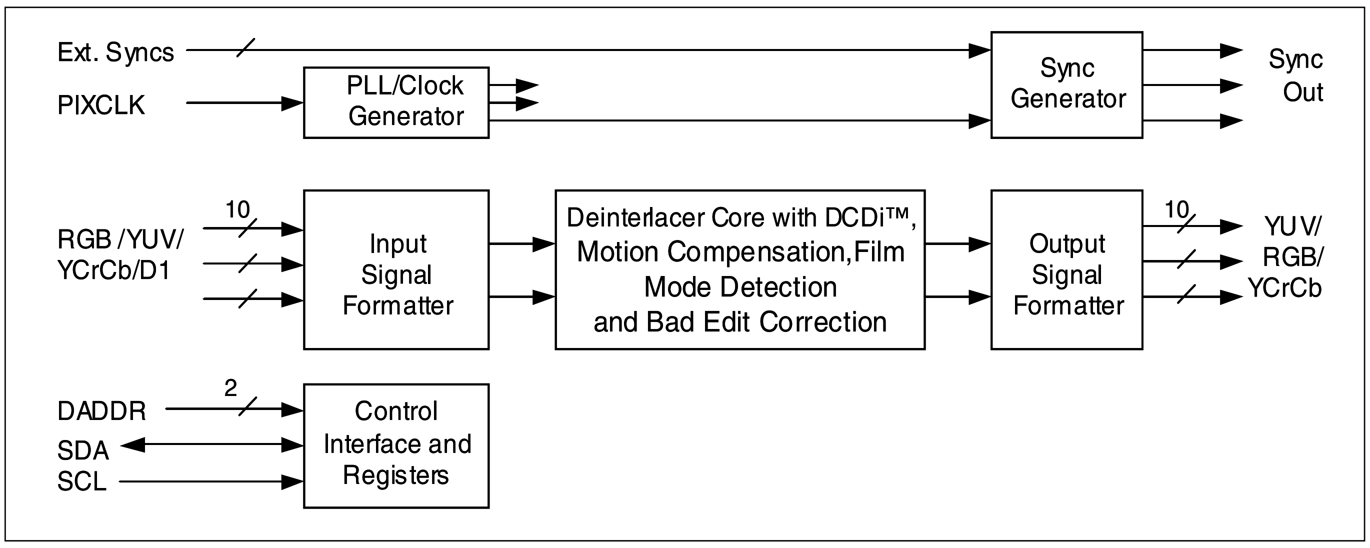
Uses low cost SDRAM as field memory – 4 MB

Optimized intra-field operation allows memory-less configuration for lowest cost applications with same design and layout as for high-end applications

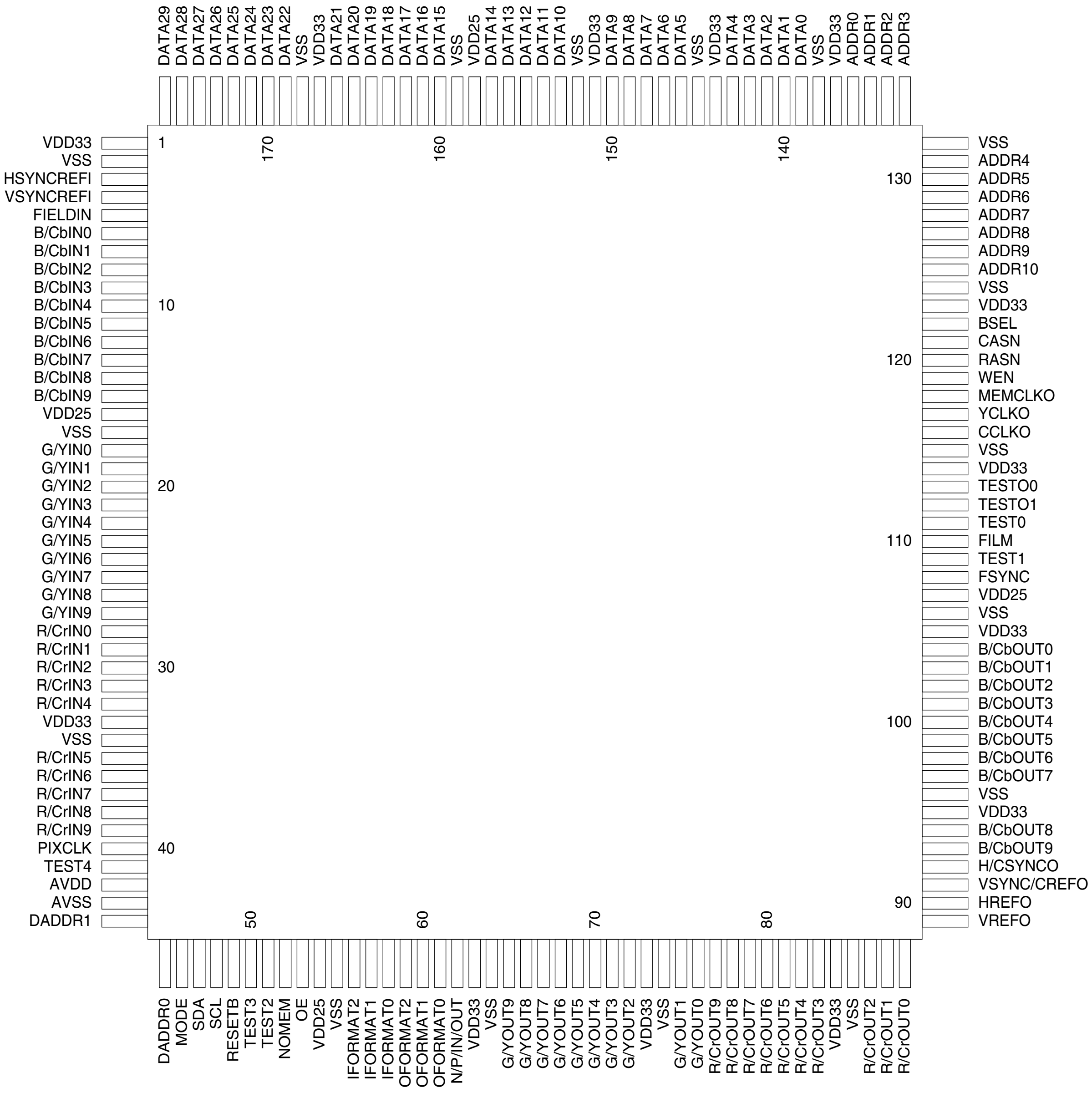
2-wire serial control interface for easy control

176-pin TQFP package

Simplified Block Diagram


Ext. Syncs
PIXCLK
PLL/Clock Generator
Sync Generator
Sync Out
10
RGB /YUV/ YCrCb/D1
Input Signal Formatter
Deinterlacer Core with DCDi™, Motion Compensation,Film Mode Detection and Bad Edit Correction
Output Signal Formatter
10
YUV/ RGB/ YCrCb
2
DADDR
SDA
SCL
Control Interface and Registers

Pin description


DATA29
DATA28
DATA27
DATA26
DATA25
DATA24
DATA23
DATA22
VSS
VDD33
DATA21
DATA20
DATA19
DATA18
DATA17
DATA16
DATA15
VSS
VDD25
DATA14
DATA13
DATA12
DATA11
DATA10
VSS
VDD33
DATA9
DATA8
DATA7
DATA6
DATA5
VSS
VDD33
DATA4
DATA3
DATA2
DATA1
DATA0
VSS
VDD33
ADDR0
ADDR1
ADDR2
ADDR3
1
170
160
150
140
130
120
110
100
90
10
20
30
40
50
60
70
80
VDD33
VSS
HSYNCREFI
VSYNCREFI
FIELDIN
B/CbIN0
B/CbIN1
B/CbIN2
B/CbIN3
B/CbIN4
B/CbIN5
B/CbIN6
B/CbIN7
B/CbIN8
B/CbIN9
VDD25
VSS
G/YIN0
G/YIN1
G/YIN2
G/YIN3
G/YIN4
G/YIN5
G/YIN6
G/YIN7
G/YIN8
G/YIN9
R/CrIN0
R/CrIN1
R/CrIN2
R/CrIN3
R/CrIN4
VDD33
VSS
R/CrIN5
R/CrIN6
R/CrIN7
R/CrIN8
R/CrIN9
PIXCLK
TEST4
AVDD
AVSS
DADDR1
DADDR0
MODE
SDA
SCL
RESETB
TEST3
TEST2
NOMEM
OE
VDD25
VSS
IFORMAT2
IFORMAT1
IFORMAT0
OFORMAT2
OFORMAT1
OFORMAT0
N/P/IN/OUT
VDD33
VSS
G/YOUT9
G/YOUT8
G/YOUT7
G/YOUT6
G/YOUT5
G/YOUT4
G/YOUT3
G/YOUT2
VDD33
VSS
G/YOUT1
G/YOUT0
R/CrOUT9
R/CrOUT8
R/CrOUT7
R/CrOUT6
R/CrOUT5
R/CrOUT4
R/CrOUT3
VDD33
VSS
R/CrOUT2
R/CrOUT1
R/CrOUT0
VSS
ADDR4
ADDR5
ADDR6
ADDR7
ADDR8
ADDR9
ADDR10
VSS
VDD33
BSEL
CASN
RASN
WEN
MEMCLKO
YCLKO
CCLKO
VSS
VDD33
TESTO0
TESTO1
TEST0
FILM
TEST1
FSYNC
VDD25
VSS
VDD33
B/CbOUT0
B/CbOUT1
B/CbOUT2
B/CbOUT3
B/CbOUT4
B/CbOUT5
B/CbOUT6
B/CbOUT7
VSS
VDD33
B/CbOUT8
B/CbOUT9
H/CSYNCO
VSYNC/CREFO
HREFO
VREFO

Pin #	Name	Description
52	NOMEM	No Memory Mode control input. This pin controls the operation of the FLI2200 as follows: When this pin is set low the device is used with external field memories and operates in the full set of deinterlacing modes, i.e., motion adaptive video deinterlacing and full frame film source deinterlacing using 3:2 pulldown detection (2:2 pulldown for 625/50 sources). When this pin is set high the FLI2200 is forced into the intra-field only deinterlacing mode, which requires no external memories, allowing the FLI2200 to be used in low-cost applications where the ultimate video quality is not a requirement. ***To ensure proper startup of the SDRAMs this pin should be set high during the power-up sequence.*** This can be overridden by the NMOvr bit, bit 1 in register 05_H, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register 05_H for details.
27-18	G/YIN$_{9-0}$	10-bit green or luminance signal input bus. The mode is set by the IFORMAT$_{2-0}$ pins. This can be overridden by the IFmtOvr bit, bit 3 in register 00_H, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register 00_H for details. This signal is sampled on the rising edge of PIXCLK.
15-6	B/CbIN$_{9-0}$	10-bit blue or Cb chroma signal input bus. The mode is set by the IFORMAT$_{2-0}$ pins. This can be overridden by the IFmtOvr bit, bit 3 in register 00_H, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register 00_H for details. Bits 6, 4 and 3 in register 08_H specify the busses used in the multiplexed modes. In all cases the signals are sampled on the rising edges of PIXCLK. In the Y Cb Cr and Y Pb Pr modes the Cb or Pb signal is sampled on alternate rising edges of PIXCLK in 4:2:2 mode. The frequency of PIXCLK will be 27 MHz in the multiplexed Y/Cb/Cr mode and 13.5 MHz in all other modes. These pins should be tied low when not used.
39-35 32-28	R/CrIN$_{9-0}$	10-bit red or Cr chroma signal input bus. The mode is set by the IFORMAT$_{2-0}$ pins. This can be overridden by the IFmtOvr bit, bit 3 in register 00_H, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register 00_H for details. Bits 6, 4 and 3 in register 08_H specify the busses used in the multiplexed modes. In all cases the signals are sampled on the rising edges of PIXCLK. In the Y Cb Cr mode the Cr signal is sampled on alternate rising edges of PIXCLK in 4:2:2 mode. The frequency of PIXCLK will be 27 MHz in the multiplexed Y/Cb/Cr mode and 13.5 MHz in all other modes. These pins should be tied low when not used.
3	HSYNCREFI	Horizontal sync or reference. The horizontal sync or reference of the input signal should be connected to this pin. The function is programmed with bit 4 in register 00_H. The polarity and position of the sync or reference pulse relative to the start of active video are both programmable within a small range. When the FLI2200 is used in the ITU-R BT 601/D1 input mode with embedded syncs (IFormat = 110) this input is not used and should be tied low; in this case all sync information will be derived from the signal.
4	VSYNCREFI	Vertical sync or reference. The vertical sync or reference of the input signal should be connected to this pin. The function is programmed with bit 4 in register 00_H. The polarity and position of the sync or reference pulse relative to the start of active video are both programmable within a small range. When the FLI2200 is used in the ITU-R BT 601/D1 input mode with embedded syncs (IFormat = 110) this input is not used and should be tied low; in this case all sync information will be derived from the signal.
5	FLDIN	Field identifier input. The field identifier output of the source signal should be connected to this pin. A low setting signifies an even field and a high level signifies an odd field. When bit 4 in register 00_H is set low, the input timing is based on HREF and VREF and this signal is required. When this bit is set high the input timing is based on HSYNC and VSYNC and this signal is generated internally and is not required. When bit 5 in register 06 is set high this signal is also used as the frame boundary identifier for 30 Hz film sources.

Pin Connections and Functions

Pin #	Name	Description
See list	V_{SS}	Ground connections. Connect to the digital ground plane. Pins: 2, 17, 34, 55, 64, 74, 85, 96, 106, 115, 124, 132, 138, 145, 152, 159, 168
See list	V_{DD33}	Pad Ring digital power connections. Connect to the digital 3.3 volt power supply and decouple to the digital ground plane. Pins: 1, 33, 63, 73, 84, 95, 105, 114, 123, 137, 144, 151, 167
See list	V_{DD25}	Core Logic digital power connections. Connect to the digital 2.5 volt power supply and decouple to the digital ground plane. Pins: 16, 54, 107, 158
43	AV_{SS}	Ground connection for the clock PLL circuits. Connect to the digital ground plane
42	AV_{DD}	Analog power connections for the clock PLL circuit. Connect to a separately decoupled 2.5 volt power supply and decouple directly to the AV_{SS} pin..
49	RESETB	Reset. When this input is set low it will reset all the internal registers to the default states. Refer to the section on the control registers for details of these states. The device must be reset after it is powered-up.
53	OE	When this pin is set high the outputs of the FLI2200 will be enabled; when it is set low the outputs will be set into a high-impedance state.
56-58	$IFORMAT_{2\text{-}0}$	Input signal format control. The settings of these pins set the format of the input signal. This can be overridden by the IFmtOvr bit, bit 3 in register 00_H, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register 00_H for details.
59-61	$OFORMAT_{2\text{-}0}$	Output signal format control. The settings of these pins set the format of the output signal. This can be overridden by the OFmtOvr bit, bit 3 in register 07_H, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register 07_H for details.
44-45	$DADDR_{1\text{-}0}$	The settings of $DADDR_{1\text{-}0}$ allow the device address of the control bus to be programmed to prevent conflict with the other devices connected to the bus. $DADDR_{1\text{-}0}$ allow the device address to be set to any of the following values: $C0/C1_H$, $C2/C3_H$, $E0/E1_H$, $E2/E3_H$. Please refer to the section “Control Bus Operation and Protocol” for further information.
46	MODE	When this pin is set low the control bus will operate in the slave mode; allowing the device to programmed from an external controller. When it is set high the FLI2200 will self-program from an external I^2C memory connected to the bus. Please refer to the “Control Bus Operation and Control Protocol” section for more details.
47	SDA	2-wire serial control bus data. Data can be written to the control registers via this pin when it is in the input mode and data can be read from the status registers when it is in the output mode. Refer to the section on the serial port for timing and format details and to the section on the registers for programming information.
48	SCL	2-wire serial control bus clock. When the control port operates in slave mode this pin will be an input and when it operates in the self programming mode it will be an output.
40	PIXCLK	Pixel clock input. This clock is used to drive all the circuits in the FLI2200. An internal PLL is used to upconvert this clock to provide the master clock signal and other clocks used internally. Note that when the FLI2200 is used in the D1 input mode the PIXCLK input should run at the rate of two cycles per pixel (one for luma and one for chroma).
62	N/P/IN/OUT	NTSC/PAL input or output. The default function of this pin is NTSC/PAL signal indicator output. When the input video signal is a 525 line signal this pin will be set high and when it is a 625 line signal the pin is set low. This function of this pin can be programmed to be an input according to the setting of this pin if the $NPOp_{1\text{-}0}$ bits, bits 5-4 in register 03_H, are set to 00_H, overriding the internal line counter. i.e., it will treat the signal as a 525 line signal when it is set high and a 625 line signal when it is set low.

Pin #	Name	Description
65-72 75-76	G/YOUT$_{9\text{-}0}$	Green or luminance output bus. In the RGB mode this output is the Green signal and in the YCbCr mode it is the Y signal. The mode is set by the OFORMAT$_{2\text{-}0}$ pins. This can be overridden by the OFmtOvr bit, bit 3 in register 07$_H$, allowing this function to be set or changed via the I^{2}C bus. Please refer to the description of register 07$_H$ for details. The signal is clocked out on the falling edge of YCLKO.
93-94 97-104	B/CbOUT$_{9\text{-}0}$	Blue or Cb chrominance output bus. In the RGB mode this output is the Blue signal, in the Y Cb Cr mode it is the Cb signal. The mode is set by the OFORMAT$_{2\text{-}0}$ pins. This can be overridden by the OFmtOvr bit, bit 3 in register 07$_H$, allowing this function to be set or changed via the I^{2}C bus. Please refer to the description of register 07$_H$ for details. The busses used in the multiplexed modes are set by means of bit 5 in register 08$_H$. The signal is clocked out on the falling edge of YCLKO in the RGB and YUV 4:4:4 modes, on the falling edge of YCLKO prior to the next rising edge of CCLKO in the YUV 4:2:2 mode, and on the rising edge of MEMCLKO in the multiplexed YCbCr (pseudo D1) mode.
77-83 86-88	R/CrOUT$_{9\text{-}0}$	Red or Cr chrominance output bus. In the RGB mode this output is the Red signal, in the YCbCr mode it is the Cr signal. The mode is set by the OFORMAT$_{2\text{-}0}$ pins. This can be overridden by the OFmtOvr bit, bit 3 in register 07$_H$, allowing this function to be set or changed via the I^{2}C bus. Please refer to the description of register 07$_H$ for details. The busses used in the multiplexed modes are set by means of bit 5 in register 08$_H$. The signal is clocked out on the falling edge of YCLKO in the RGB and YUV 4:4:4 modes, on the falling edge of YCLKO prior to the next rising edge of CCLKO in the YUV 4:2:2 mode, and on the rising edge of MEMCLKO in the multiplexed YCbCr (pseudo D1) mode.
116	CCLKO	Chroma output sampling clock. This clock is derived from PIXCLK and will be at half the frequency of YCLKO. In 30-bit 4:2:2 output mode the chroma output signals will change on the falling edge of YCLKO prior to the next rising edge this clock.
117	YCLKO	Luma output sampling clock. This clock is derived from PIXCLK and is double the frequency of PIXCLK. In 30-bit and 20-bit output modes the output signals will change on the falling edge of this clock.
89	VREFO	Start of active field or frame indicator. This signal goes high to indicate the first active line in each field or frame and goes low during the vertical blanking interval. The polarity and timing of this signal are programmable.
90	HREFO	Start of active line indicator output. This signal goes high to indicate the first active pixel in each line and goes low during the horizontal blanking interval. The polarity and timing of this signal are programmable.
91	VSYNC/ CREFO	Vertical sync output. This signal provides the vertical sync function for the outputs. Its polarity is programmable to be active high or active low. It can also be programmed to be a composite reference for applications requiring this instead of sync.
92	H/CSYNCO	Horizontal or composite sync output. This signal provides the horizontal sync function for the outputs. Its polarity is programmable to be active high or active low. This signal can also be programmed to be the composite sync output, CSYNC.
108	FSYNC	Film mode sync output. When film mode is detected this pin will toggle in sync with the 3:2 (NTSC) or 2:2 (PAL and 30 Hz film in NTSC) pulldown sequence detected in the source.
110	FILM	Film mode detector output. This pin will be set high when the FLI2200 detects that the video input was converted from 24 fps film with a teleciné machine. If film mode is not detected this pin will be set low.

Pin #	Name	Description
125-131 133-136	ADDR$_{10-0}$	SDRAM Address bus. This signal bus is used to address the external SDRAM(s) used for field memories. It should be connected to the A$_{10-0}$ bus of the memory chip(s). Please refer to the Applications section of this data sheet for further details.
176-169 166-160 157-153 150-146 143-139	DATA$_{29-0}$	SDRAM Data bus. This signal bus is used to transfer the data to and from the external SDRAM(s) used for field memories. It should be connected to the DQ$_{29-0}$ bus of the memory chip when using a 64 Mbit SDRAM. When using two 16 Mbit SDRAMs this 30-bit bus may be connected to the two 16-bit data busses of the memories in two ways: either connect 16 lines to one chip and 14 to the other, or connect 15 to both. In all cases the two unused data lines on the memory chip(s) should be connected to ground via 22 k? resistors. Please refer to the Applications section of this data sheet for further details.
118	MEMCLKO	SDRAM clock and 2x output sampling clock. This clock is derived from PIXCLK and will be at double the frequency of YCLKO. This active signal should be connected to the CLK pin(s) on the SDRAM(s). When the 10-bit output mode selected the output signals will also change at this clock rate and this should then be used as the output clock..
119	WEN	SDRAM Write Enable. This active low signal should be connected to the WE pin(s) on the SDRAM(s).
120	RASN	SDRAM Row Address Select. This active low signal should be connected to the RAS pin(s) on the SDRAM(s).
121	CASN	SDRAM Column Address Select. This active low signal should be connected to the CAS pin(s) on the SDRAM(s).
122	BSEL	SDRAM Bank Select. When using two 16 Mbit SDRAMs this signal should be connected to the BA (also called BS or A$_{11}$) pin on both SDRAMs. When using a 64 Mbit SDRAM this signal should be connected to the BA0 (also called BS0 or A$_{11}$) pin on the SDRAM and BA1/ BS1 (also called BA when BA0 is referred to as A$_{11}$) should be tied low.
41, 50, 51, 109, 111	TEST$_{4-0}$	These pins are used for test purposes only and should always be tied low for normal operation.
112, 113	TESTO$_{1-0}$	These pins are test outputs and should be left unconnected in normal operation.

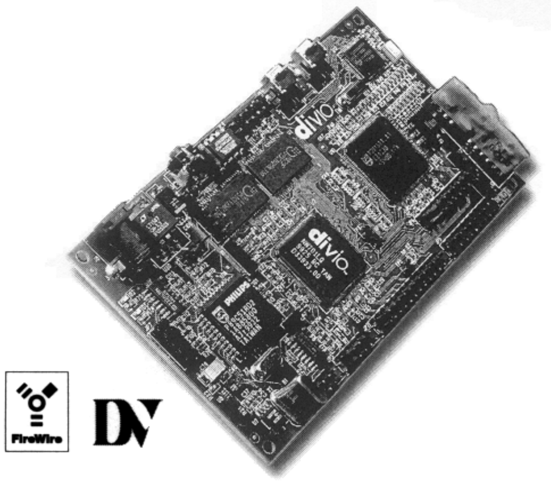
9.11 IC’s Divio Board

9.11.1 IC7404: NW700

divio™

NW700

DV Decoder
Daytona Beach
Reference Solution


divio
FireWire
DV

Features and Benefits

Enhanced Feature set
- Fully DV-SD Compliant
- Automatic Audio and AUX Code Processing
- Pin compatible with NW701 (DV CODEC)

Low System Cost
- Integrated single-chip design including AV processing and video decoding
- Glue-less interface to Video Encoder (SAA7121), Audio Encoder (UDA1340), Micro-controller, and memory
- Integrated shuffle memory logic
- Requires only one 256K x 32 EDO DRAM

Real-time Performance
- High speed (33Mbytes/s throughput)
- 54MHz double clock speed for dual stream applications

Video and Audio Support
- CCIR656 Video output and I^{2}S Audio output
- Support NTSC and PAL
- Selectable Audio channel (A/B or C/D)
- 48, 44.1, and 32KHz (12- and 16-bit) audio support

Simple Host Bus connectivity
- 8 or 16-bit asynchronous host bus interface
- built-in 512 byte DV FIFO
- Three interrupt pins for enhanced system control

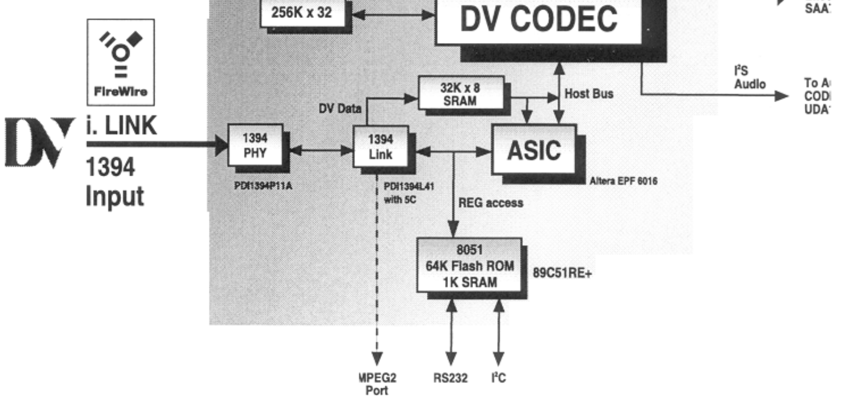
NW700 DV Decoder Daytona Beach Reference Solution

divio introduces the NW700, the world’s first single-chip DV decoder. Fully DV-SD compliant and designed with divio’s patented pending compression technology, the NW700 delivers unrivaled video quality, performance and compatibility. With a single-chip design and glueless interface to standard video components, divio’s single chip DV decoder will replace current multi-chip solution and enable a new generation of cost-effective digital video consumer products.

divio has created the “Daytona Beach” reference solution that includes the NW700, Philips Semiconductor’s PDI1394L4X audio/video 1394 LINK layer controller and PDI1394P11A 200 Mbits/sec PHY. divio provides a complete easy to integrate DV/IEEE1394 solution to OEMs to reduce time-to-market and development costs.

The NW700 provides an unprecedented feature-set that deliver real-time DV decoding functions to empower the next generation of consumer electronics devices.

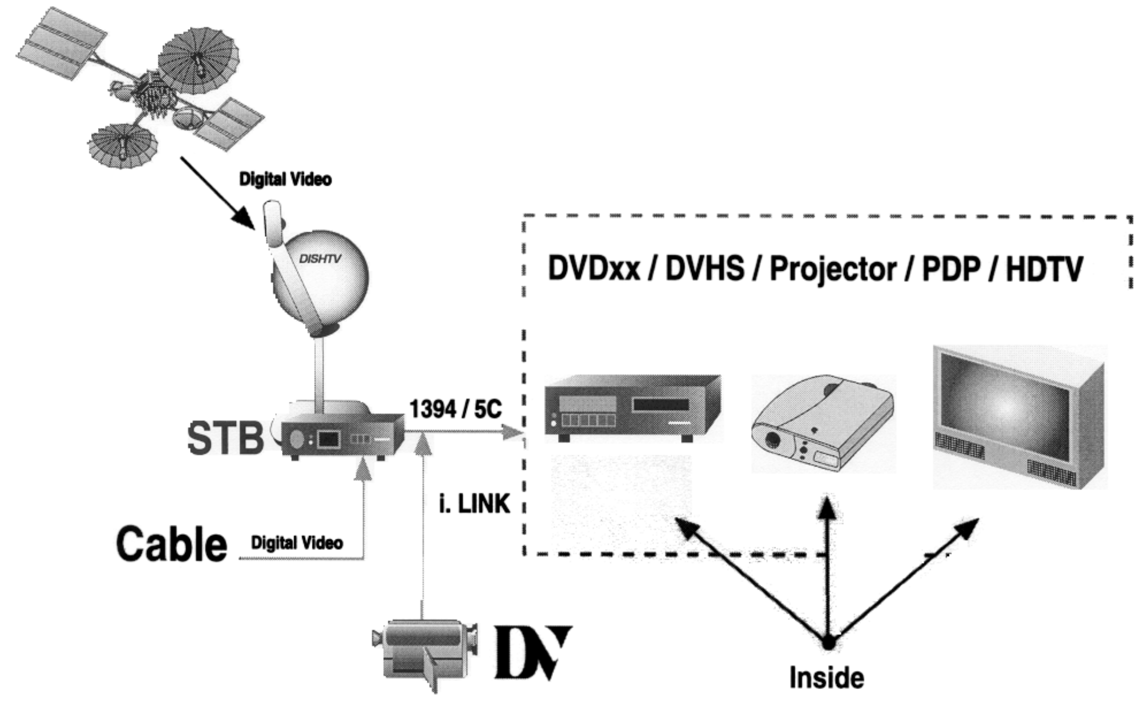
DAYTONA BEACH DV Decode Module


FireWire
DV
i. LINK
1394
Input
Shuffle Memory
256K x 32
Divio NW700
DV CODEC
CCIR656
Video
To V
Enc
SAA
I²S
Audio
To A
COD
UDA
DV Data
32K x 8
SRAM
Host Bus
1394
PHY
PDI1394P11A
1394
Link
PDI1394L41
with 5C
ASIC
Altera EPF 6016
REG access
8051
64K Flash ROM
1K SRAM
89C51RE+
MPEG2
Port
RS232
I²C

APPLICATIONS

NW700

DV Decoder
Daytona Beach
Reference Solution



Applications

Plasma Display Panel and Video Projector
Digital VCR / D-VHS
DVD-RAM
Digital Set-top-box
HDTV

Daytona Beach Reference Kit

Board Components

- divio NW700 - DV Decoder
- 8051 µC (P89C51RD2)
- 100p FPGA/32k x 8 SRAM
- IEEE1394 LINK (PDI1394L4X)
- IEEE1394 PHY (PDI1394P11A)
- 256 x 32 EDO Memory

Manufacturing Kit Contents

- Daytona Beach Reference Design
- Schematics, Gerber Files and BOM
- Technical Documents and Manuals
- FPGA and Firmware Source Code

Ordering Information

Part Number	*Description*
• NW700LQ	DV Decoder
• Daytona Beach	Manufacturing Kit

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9.12 List of Abbreviations

Digital Board

+12V
+12V Power Supply
+2V5_FLI
+2V5 Power Supply for FLI
+2V5_PLL
+2V5 Power Supply for PLL
+3V3
+3V3 Power Supply
+3V3_ANA
+3V3 Power Supply Analogue
+3V3_DD
+3V3 Power Supply Digital
+3V3_FLI
+3V3 Power Supply for FLI
+5V
+5V Power Supply
+5V_BUFFER
+5V Power Supply for Video Filters
5508_HS
Horizontal Synchronisation from Host Decoder to Progressive Scan
5508_ODD_EVEN
Odd - Even control from Host Decoder to Progressive Scan
-5V
-5V Power Supply
-5V_BUFFER
-5V Power Supply for Video Filters
A_EMPRESS(13:0)
EMPRESS address output to SDRAM
ACC_ACLK_OSC
Audio Clock PLL output sync with incoming video for record
ACC_ACLK_PLL
Audio Clock PLL output for play back
ACLK_EMP
EMPRESS audio clock output
AD_ACLK
Audio Decoder Clock
AD_BCLK
Audio Decoder I2S bit clock
AD_DATAO
Audio Decoder Output data (PCM)
AD_SPDIF33
Audio digital output to the analog board
AD_WCLK
Audio Decoder I2S word clock
AE_ACLK
Audio Encoder Clock
AE_ACLK_OEN
Audio Encoder Clock Output Enable
AE_BCLK
Audio Encoder I2S bit clock
AE_BCLK_DV
Audio Encoder I2S bit clock to DVIO
AE_BCLK_VSM
Audio Encoder I2S bit clock to VSM
AE_DATAI
Audio Encoder Input data (PCM)
AE_DATAI_DV
Audio Encoder Input data (PCM) from DVIO
AE_DATAO
Audio Encoder Output data (PCM)
AE_WCLK
Audio Encoder I2S word clock
AE_WCLK_DV
Audio Encoder I2S word clock to DVIO
AE_WCLK_VSM
Audio Encoder I2S word clock to VSM
ANA_WE
Analogue write enable
ANA_WE_LV
Analogue write enable Low Voltage
B_IN_VIP
Video blue input to Video Input Processor
B_OUT
Video blue output from Host Decoder
B_OUT_B
Filtered blue video output
BA
Bank Address
BCLK_CTL_SERVICE
Bitclock control Service Interface
BE_BCLK
Basic Engine I2S bit clock
BE_BCLK_VSM
Basic Engine I2S bit clock to VSM
BE_CPR
Basic Engine Control Processor ready to accept data
BE_DATA_RD
Basic Engine Data read
BE_DATA_WR
Basic Engine Data write
BE_FAN
Basic Engine FAN
BE_FLAG
Basic Engine error flag
BE_IRQN
Basic Engine interrupt request
BE_LOADN
Basic Engine LOAD(LOW active)
BE_RXD
Basic Engine S2B received data
BE_SUR
Basic Engine servo unit ready to accept data (S2B)
BE_SYNC
Basic Engine sector/abs time sync
BE_TXD
Basic Engine S2B transmitted data
BE_V4
Basic Engine versatile input pin
BE_WCLK
Basic Engine I2S word clock
C_IN
Video Chrominance input
C_IN_VIP
Chrominance input to Video Input Processor
C_OUT
Chrominance output from Host Decoder
C_OUT_B
Filtered Chrominance output
CAS
Column Address strobe
CB_OUT(9:0)
Chrominance Blue out
CLK4
SDRAM clock
CPUINT0
Control processor unit interrupt
CPUINT1
Control processor unit interrupt
CR_OUT(9:0)
Chrominance Red out
CTS1P
Clear to send (Service Interface)
CVBS_OUT
Composite video output out of the Host Decoder
CVBS_OUT_B
Filtered Composite video output
CVBS_OUT_B_VIP
Composite video output to Video Input Processor(digital board video loop)
CVBS_Y_IN
Composite video/Luminance input
CVBS_Y_IN_A
Composite video/Luminance input to Video Input Processor
CVBS_Y_IN_B

Composite video/Luminance input to Video Input Processor

CVBS_Y_IN_C
Composite video/Luminance input to Video Input Processor

D_ADDR(10:0)
Address bus

D_DATA(29:0)
Data bus

D_EMPRESS(15:0)
SDRAM data input/output of EMPRESS

D_PAR_D(7:0)
Front-end parallel interface data (record)

D_PAR_DVALID
Front-end parallel interface data valid

D_PAR_REQ
Front-end parallel interface request

D_PAR_STR
Front-end parallel interface strobe

D_PAR_SYNC
Front-end parallel interface sync

DV_IN_CLK
Digital Video in clock from DVIO board

DV_IN_DATA(7:0)
Digital Video in data bus from DVIO board

DV_IN_HS
Digital Video in horizontal synchronisation from DVIO board

DV_IN_VS
Digital Video in vertical synchronisation from DVIO board

EMI_A(21:1)
External Memory Interface Address Bus(Host Decoder)

EMI_BE0N
External Memory Interface Lower byte enable(Host Decoder)

EMI_BE1N
External Memory Interface Upper byte enable(Host Decoder)

EMI_CAS0N
External Memory Interface SDRAM column address strobe(Host Decoder)

EMI_CE1N
External Memory Interface VSM Lower bank enable

EMI_CE2N
External Memory Interface VSM Higher bank enable

EMI_CE3N
External Memory Interface flash IC's enable

EMI_D(15:0)
External Memory Interface Data Bus(Host Decoder)

EMI_PROCCLK
External Memory Interface Processor Clock(Host Decoder)

EMI_RWN
External Memory Interface Read/Write control signal(Host Decoder)

EMI_WAIT
External Memory Interface Wait state request(Host Decoder)

EMPRESS_BOOT
EMPRESS BOOT select input

EMPRESS_IRQN
EMPRESS Interrupt request output

FLASH_OEN
FLASH output enable control signal

G_IN_VIP
Video green input to Video Input Processor

G_OUT
Video green output from Host Decoder

G_OUT_B
Filtered green video output from Host Decoder

GNDD
Digital Ground

HD_M_AD(13:0)
Host Decoder SDRAM address bus

HD_M_CASN
Host Decoder SDRAM column address strobe

HD_M_CLK
Host Decoder SDRAM clock

HD_M_CS0N
Host Decoder SDRAM chip select

HD_M_DQ(15:0)
Host Decoder SDRAM data bus

HD_M_DQML
Host Decoder SDRAM data mask enable(Lower)

HD_M_DQMU
Host Decoder SDRAM data mask enable(Upper)

HD_M_RASN
Host Decoder SDRAM row address strobe

HD_M_WEN
Host Decoder SDRAM write enable

HSOUT
Horizontal synchronisation OUT

ION
Inverted ON: Enable the power supply for the digital board when LOW

IRESET_DIG
Initialisation of the digital board, HIGH when power ON

JTAG3_TCK
JTAG Test Clock

JTAG3_TD_VIP_TO_VE
JTAG Transmitted Data Video Input Processor to Video Encoder

JTAG3_TD_VSM_TO_VIP
JTAG Transmitted Data Versatile Stream Manager to Video Input Processor

JTAG3_TMS
JTAG Test Mode Select

JTAG3_TRSTN
JTAG Test part ResetN

LOAD_DVN
LOAD Digital Video(LOW active)

MUTEN
Mute enable

MUTEN_LV
Mute enable Low Voltage

P_SCAN_YUV(7:0)
Progressive Scan digital video bus

R_IN_VIP
Video Red input to Video Input Processor

R_OUT
Video Red output from Host Decoder

R_OUT_B
Filtered Red Video output from Host Decoder

RAS
Row Address Strobe

RESETN
Reset Host Decoder

RESETN_BE
System reset basic engine (buffered)

RESETN_DVIO
System reset Digital Video Input Output (buffered)

RESETN_VE
System reset Video Encoder

ROMH_CEN
Flash 2 chip enable

ROML_CEN
Flash 1 chip enable

RSTN_BE
Reset control of basic engine

RSTN_DVIO
Reset control of DVIO

RTS1P
Ready To Send data to service serial interface

RX1P
Receive data from service serial interface

SCL
I2C bus clock

SD_CASN
SDRAM Column Address strobe output (active LOW)

SD_CLK
SDRAM clock output

SD_CLKE
SDRAM clock enable output

SD_CSN
SDRAM

SD_DQM(1:0)
SDRAM data mask enable output

SD_RASN	SDRAM row address strobe output
SD_WEN	SDRAM write enable output
SDA	I2C bus data
SEL_ACLK1	Select audio clock(playback)
SM_CS3N	SRAM chip select
SM_LBN	SRAM lower bank
SM_OEN	SRAM output enable
SM_UBN	SRAM upper bank
SM_WEN	SRAM write enable
SMA(17:0)	SRAM address output
SMD(15:0)	SRAM data input/output
SYSCLK_EMPRESS	System clock EMPRESS
SYSCLK_PROGSCAN	System clock Progressive Scan
SYSCLK_VSM_5508	System clock VSM and Host decoder
TX1P	Transmit data to service serial interface
U_IN	Video U input
U_IN_VIP	Video U input to Video Input Processor
V_IN	Video V input
V_IN_VIP	Video V input to Video Input Processor
VCC3_CLK_BUF	Power supply 3V3 clock buffer
VCC3_VSM	Power supply 3V3 Versatile Stream Manager
VCC3_VSM_MEM	Power supply 3V3 Versatile Stream Manager Memory
VCC5_4046	Power supply 5V to PLL IC
VDD_125	Power supply 5V to buffer 7202
VDD_CORE	Sti5508 Core supply voltage 2.5V
VDD_EMP	Empress supply voltage 3.3V
VDD_EMP_CORE	Empress Core supply voltage 2.5V
VDD_FLASH_H	Flash 7301 supply voltage
VDD_FLASH_L	Flash 7302 supply voltage
VDD_LVC32	Power supply LVC32
VDD_PCM	Power supply Audio decoder of Sti5508
VDD_PLL	Power supply PLL audio decoder of Sti5508
VDD_RGB	Power supply video encoder of Sti5508
VDD_STI	Power supply of Sti5508
VDD_YCC	Power supply video encoder of Sti5508
VDD5_MK2703	Power supply MK2703
VDD5_OSC	Power supply Oscillator
VDDA1A_7118	Power supply for analog input of VIP
VDDA2A_7118	Power supply for analog input of VIP
VDDA3A_7118	Power supply for analog input of VIP
VDDA4A_7118	Power supply for analog input of VIP
VDDE_7118	Power supply digital for peripheral cells of VIP
VDDI_7118	Power supply digital for core of VIP
VDDX_7118	Power supply for crystal oscillator of VIP
VE_DATA(7:0)	Video Encoder data Bus
VE_DSN	Video Encoder Data Strobe
VE_DTACKN	Video Encoder Data Transfer acknowledge
VIP_ERROR	Video Input Processor error
VIP_FB	Video Input Processor Fast Blanking
VIP_FID_FF	Video Input Processor field indentifier to Flip Flop
VIP_HS	Video Input Processor horizontal synchronisation
VIP_ICLK	Video Input Processor input Clock
VIP_IDQ	Video Input Processor output data qualifier
VIP_IGP1	Video Input Processor input general purpose 1
VIP_INT	Video Input Processor interrupt
VIP_RTS1	Video Input Processor ready to send
VIP_VS	Video Input Processor vertical synchronisation
VIP_YUV(7:0)	Video Input Processor digital video(CCIR 656)
VS_IN	Vertical synchronisation IN
VSM_M_A(13:0)	Versatile Stream Manager SDRAM address bus
VSM_M_CASN	Versatile Stream Manager SDRAM column address strobe
VSM_M_CLKEN	Versatile Stream Manager SDRAM clock enable
VSM_M_CLKOUT	Versatile Stream Manager SDRAM clock out
VSM_M_D(15:0)	Versatile Stream Manager SDRAM data bus
VSM_M_LDQM	Versatile Stream Manager SDRAM lower data mask enable
VSM_M_RASN	Versatile Stream Manager SDRAM row address strobe
VSM_M_UDQM	Versatile Stream Manager SDRAM upper data mask enable
VSM_M_WEN	Versatile Stream Manager SDRAM write enable
VSM_UART1_CTSN	Versatile Stream Manager UART1 clear to send to analog board (UART1 is gateway to analog board)
VSM_UART1_RTSN	Versatile Stream Manager UART2 clear to send to DVIO board (UART2 is gateway to DIVIO board)
VSM_UART1_RX	Versatile Stream Manager UART1 ready to send to analog board
VSM_UART1_TX	Versatile Stream Manager UART2 ready to send to DVIO board
VSM_UART2_CTSN	

Versatile Stream Manager UART1 received data to analog board
VSM_UART2_RTSN
Versatile Stream Manager UART2 received data to DVIO board
VSM_UART2_RX
Versatile Stream Manager UART1 transmitted data to analog board
VSM_UART2_TX
Versatile Stream Manager UART2 transmitted data to DVIO board
VSOUT
Vertical synchronisation OUT
WE
Write Enable
Y_IN
Luminance input from analog board
Y_OUT
Luminance output from Host Decoder
Y_OUT_B
Filtered luminance output
YY_OUT(9:0)
Luminance output from FLI

Divio Board

+35V_DV_EDO
+3V3 Power supply EDO Bus IC7404
+3V3
+3V3 Power supply
+3V3_DLY
+3V3 Power supply for IC7500
+3V3_DV
+3V3 Power supply for IC7404
+3V3_FPGA
+3V3 Internal Power supply for IC7303
+3V3_FPGA_CONF
+3V3 Power supply for IC 7300
+3V3_IEEE_A
+3V3 Analogue Power supply for PHY IC 7101
+3V3_IEEE_D
+3V3 Digital Power supply for PHY IC 7101
+3V3_IEEE_PLL
+3V3 PLL Power supply for PHY IC 7101
+3V3_LINK
+3V3 Power supply IC7103
+3V3_PLL
+3V3 Power supply IC7307 & IC7308
+3V3_SRAM
+3V3 Power supply IC7301, IC7302, IC7305 & IC7306
+5V
+5V Power supply
+5V_PROC
+5V Power supply IC7200, IC7201, IC7203 & IC7208
+VCC_DV_RAM
+3V3 Power supply for DV_RAM (IC7400--> IC7404)
1394_RSTN
Reset of LINK IC (7103) and PHY IC (7101)
A(0:8)
Address lines
AUD_BCLK
Audio Bit Clock
AUD_MUTE
Audio Mute
AUD_SDI
Audio Serial Data Input
AUD_SDO_CON
Audio Serial Data Output to buffer IC 7505
AUD_SDO_DAC
Audio Serial Data Output to DAC IC 7506
AUD_WS_701
Audio Word Select to DV CODEC IC 7404
AUD_WS_OUT
Audio Word Select to buffer IC 7505
BUFENN_AUD
Buffer Enable Audio
BUFENN_VID
Buffer Enable Video
CCLK
Configuration Clock
CLK27M
27MHz Clock
CLK27M_CON
27MHz Clock to Digital Board
CLK27M_DV
27MHz Clock Digital Video Codec
CLK27M_OSC
27MHz Clock IC7304
CLOCKGENAUD
Clock generator Audio
CLOCKGENVID
Clock generator Video
CTSN
Clear to Send
DATA
Data from config ROM
DONE
Indication of the completion of the configuration process
DOUT
Serial configuration data output
DV_ASN
DVCODEC Address Strobe
DV_DRQN
DVCODEC Data Request Interrupt
DV_DSLN
DVCODEC Data Strobe Lower 8 bits
DV_DSUN
DVCODEC Data Strobe Upper 8 Bits
DV_DTACKN
DVCODEC Data Transfer Acknowledge
DV_ERRN
DVCODEC Error Interrupt
DV_HS_IN
DVCODEC Horizontal synchronisation In
DV_HS_OUT
DVCODEC Horizontal synchronisation Out
DV_LCN
DVCODEC Last Code Interrupt
DV_PDN
DVCODEC Power Down
DV_RSTN
DVCODEC System Reset for NW701
DV_RWN
DVCODEC Read/Write control signal
DV_VS
DVCODEC Vertical synchronisation
FIFOA_A(0:15)
FIFO buffer A Address bus
FIFOA_OEN
FIFO buffer A Output enable
FIFOA_WEN
FIFO buffer A Write enable
HAD(0:7)
Host Address/Data bus for register settings of IC7404
INITN
Initiate Configuration
IO(0:30)
Data bus of IC7404
ISPN
In System Program Line (used for programming IC7203)
LCASN
Lower Column Address strobe for IC7404 DRAMS
LINK_AVCLK
LINK IC Audio/Video Interface Clock
LINK_AVFSYNC
LINK IC Audio/Video frame sync
LINK_AVREADY
LINK IC Audio/Video data ready to send
LINK_AVSYNC
LINK IC Audio/Video packet sync

LINK_AVVALID
LINK IC Audio/Video data valid
LINK_CSN
LINK IC chip select
LINK_INTN
LINK IC interrupt
LINKFIFO_DQ(0:7)
Audio Video data interface
PA(0:15)
SRAM processor address
PAD(0:7)
SRAM processor data
PALE
Processor Address Latch Enable
PHY_CNA
PHY 1394 cable not active
PHY_LPS
LINK IC power status
PINT0N
Processor interrupt 0
PINT1N
Processor interrupt 1
PRDN
Processor read
PROGRAMN
Low active input to initiate a configuration cycle
PRSTN
Processor reset
PWRN
Processor write
RASN
Row address strobe
RESETN
DVIO board reset
RTSN
System Reset
RXD
Receive Data
SRAMCE0N
SRAM processor chip enable 0
SRAMRDN
SRAM processor output enable
TCK
Boundary scan Test Clock
TDI
Boundary scan Test Data Input
TDO
Boundary scan Test Data Output
TDO_CONF
Boundary scan Test Data Output from IC 7309
TMS
Boundary scan Test Mode Select
TXD
Transmitted Data
UCASN
Upper column address strobe
WEN
Write Enable control signal to SRAM
YUV(0:7)
Digital Video

Analog Board

+5VSTBY
Permanent Supply 5V
8SC2
Pin8 Scart2 (only for Europe)
A_DATA
Data from Analog- to Digital-Board (UART-Communication)
A_RDY
Analog-board ready (status information to digital-board)
A18 - A19
Parallel Address Bus (CC - Flash-ROM and S-RAM)
A8 - A17
Parallel Address Bus (CC - Flash-ROM and S-RAM)
AD0 - AD7
Parallel Address and Data Bus (CC - Flash-ROM and S-RAM)
AFC
Automatic Frequency Control
AFEL
Audio Frontend Left
AFER
Audio Frontend Right
AGC / WSRI
Automatic Gain Control (for Europe), Wide Screen Rear In (for NTSC)
AINFL
Audio In Front Left
AINFR
Audio In Front Right
AKILL
Audio Kill Signal
ALADC
Audio Left to ADC
ALDAC
Audio Left from DAC
ALE
Address Latch Enable
AM0
Adress-mode 0
AM1
Adress-mode 1
ARADC
Audio Right to ADC
ARDAC
Audio Right from DAC
ASCC1M
Audio Scart 1 Mute (System Clock Output for Real time Clock-Adjustment)
AVCC
Power Supply for A/D-converter
AVSS
GND-Pin for A/D-converter
CFIN
Chroma Front In
CS0_
Chip Select 0 (CC - S-RAM)
CS2_
Chip Select 2 (CC - Flash-ROM)
CVBSFIN
Video Front In
D_DATA
Data from Digital- to Analog-Board (UART-Communication)
D_RDY
Digital-board ready (status information from digital-board)
DAC_MUTE
Mute Signal for DAC
DAOUT
Digital Audio Out
DVAL
Audio from Digital Video In Left
DVAR
Audio from Digital Video In Right
DVCC1
Power Supply Pin
DVCC2
Power Supply Pin
DVCC3
Power Supply Pin
DVSS1
GND Pin
DVSS2
GND Pin
DVSS3
GND Pin
FAN_OFF
Fan for Basic engine
FBIN
Fast Blanking input
FOME

	FOllow ME Status line (matching signals yes/no; only for Europe)
G1…10	DISPLAY GRID
INT	Interrupt OUT for the CC
INT	Interrupt – line from Display Print
ION	Inverse ON-Line
IPFAIL	Inverse Power Fail Detection
IPOR	Inverse Power On Reset
IRESET	Inverse Reset Input
IRR	Signal from IR-Receiver
K1	Key-Input-Line
K2	Key-Input-Line
KILL	Audio Mute
P50 IN	P50 INput-line (only for Europe)
P50 OUT	P50 OUTput-line (only for Europe)
POR_DC	Power On Reset for Display Control Print (Ext_DL)
PSS	Pal/Secam-Select
PWM_FIL	Control line for Filament Voltage Generation
PWONSW	Amplifier Switch Audio A/D Converter
RD_	Output Enable ReaD (CC - Flash-ROM and S-RAM)
RECLED	Control Signal for REC-LED
RESET_DIG	Reset Line to Digital Board
RP_	Inverse Reset line to Flash-ROM
RSA1/2	Record Selector 1/2
RY/BY_	Ready/Busy – input line (from Flash-ROM)
SIF1	Sound intermediate frequency
SB1	Secam Band 1 (PCB-Test entrance)
SCL	I²C-Bus
SCLSW	Switched I²C-Bus
SDA	I²C-Bus
SDASW	Switched I²C-Bus
SFS_TS	SAW Filter Select Trap Select
STBY	Standby-Line (Flash_Toshiba)
SYNC	Video Sync input
TEMP_SENSE	Temperature Sense Line
VER	HW-version input
VFV	Video from Frontend
VKK	VFT Driver Power Supply
VREFH	Pin for Reference-voltage input to A/D-converter
VREFL	Pin for Reference-voltage input to A/D-converter
VS1/2	View Selector 1/2
WR_	Write Enable (CC - Flash-ROM and S-RAM)
WSFI	Wide Screen Signalling Front In
WU	Wake Up
X1	Oscillator Pin
X2	Oscillator Pin
XIN	Oscillator Pin
XOUT	Oscillator Pin
XT1	Low Frequency Oscillator Pin
XT2	Low Frequency Oscillator Pin
YFIN	Luminance Front In

10. Spare Parts List

Mechanical Parts

0001	3103 607 90062	CONTROL PANEL ASSY EU DVIO, DVDR890
0001	3103 607 90071	CONTROL PANEL ASSY EU, DVDR880
0001	3103 607 90101	CONTROL PANEL ASSY UK, DVDR880/05x
0001	3103 607 90112	CONTROL PANEL ASSY UK DVIO, DVDR890/05x
0010	3103 607 50101	KEY-SET RIGHT ASSY
0011	3103 607 50131	KEY-SET LEFT ASSY
0012	3103 607 50161	KEY REC ASSY
0021	3103 607 50181	DISPLAY-DECOR-WINDOW ASSY
0026	3103 607 50191	FLAP ASSY , DVDR880
0026	3103 607 50271	FLAP ASSY DVIO, DVDR890
0070	3103 607 90081	TRAY FRONT ASSY
0105	3103 607 50251	FOOT ASSY
0300	3103 607 50231	COVER ASSY

Miscellaneous Parts

0350	3128 147 14021	REMOTE CONTROL 25110/01
0351▲	2422 070 98133	MAINSCORD EURO
0351▲	4822 321 10713	MAINSCORD UK
0352	3103 601 00111	SCART CABLE EU
0355	3103 308 92610	CABLE AUDIO 2X2RCA MALE 1.5MTR
0356	4822 321 61579	VIDEO-CABLE
0357	4822 320 50377	CONNECT. CABLE PAL
0365	9307 002 60006	DVDRW/006 PHILIPS DISC EUROPE
0380	3103 605 20011	DIR. FOR USE DVDR 880/001
0380	3103 605 20031	DIR. FOR USE DVDR 880/021
0380	3103 605 20051	DIR. FOR USE DVDR 880/051
0380	3103 605 20061	DIR. FOR USE DVDR 890/001
0380	3103 605 20101	DIR. FOR USE DVDR 890/051
0381	3103 605 20021	DIR. FOR USE DVDR 880/001
0381	3103 605 20041	DIR. FOR USE DVDR 880/021
0381	3103 605 20071	DIR. FOR USE DVDR 890/001
0381	3103 605 20091	DIR. FOR USE DVDR 890/021
1001▲	3103 608 50180	ANALOGUE/ POWER BOARD EURO
1001▲	3103 608 50240	ANALOGUE/ POWER BOARD UK
1002	3104 128 08440	PCB ASSY DIG BOARD 1.5 EU
1003▲	3104 128 08500	PCB ASSY DVIO 4323
1004▲	3103 608 50170	DISPLAY BOARD
1005	3103 608 50320	FRONT CONNECTOR BOARD
1006	3104 128 07610	PCB ASSY 4319 DVIO-FRONT
1007		BASIC ENGINE VAE8020

Cables

8001	3103 601 00012	FFC FOIL 22P/90/22P BD FO
8003	3103 601 00032	FFC FOIL 10P/100/10P AD
8004	3103 601 00042	CBLE KR 4P/205/4P KR SHI.
8005	3103 601 00052	FFC FOIL 22P/200/22P BD
8006	3103 601 00062	CBLE KR 12P/115/12P KR UL
8007	3103 601 00072	FFC FOIL 10P/647/10P BD UL
8008	3104 157 11790	CWAS SPLIT FLEX 30 100 32S
8009	3103 601 00082	CBLE KR 8P/110/8P KR UL
8010	3103 601 00132	CBLE KR 9P/715/9P KR SHIELDED
8011	3104 128 92921	CABLE IEEE-1394 4P AMP

Display Board

Various

1111	4822 242 82114	EFOEC8004/T4
1160	4822 276 13732	SWITCH TACT PUSH
1161	4822 276 13732	SWITCH TACT PUSH
1162	4822 276 13732	SWITCH TACT PUSH
1163	4822 276 13732	SWITCH TACT PUSH
1164	4822 276 13732	SWITCH TACT PUSH
1165	4822 276 13732	SWITCH TACT PUSH
1166	4822 276 13732	SWITCH TACT PUSH
1170	4822 276 13732	SWITCH TACT PUSH
1171	4822 276 13732	SWITCH TACT PUSH
1180	4822 276 13732	SWITCH TACT PUSH
1916	4822 267 11031	10P. FEM. V

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2100	3198 017 34730	0603 16V 47nF COL
2101	4822 124 81151	22µF 50V
2102	4822 121 51252	470nF 5% 63V
2103	4822 124 21732	10µF 20% 25V
2104	3198 017 34730	0603 16V 47nF COL
2105	5322 126 11578	1nF 10% 50V 0603
2106	4822 126 13879	220nF 20% 16V
2111	3198 017 34730	0603 16V 47nF COL
2112	4822 124 11946	22µF 20% 16V
2119	2238 586 59812	0603 50V 100NP80M
2150	4822 124 11946	22µF 20% 16V
2168	5322 126 11583	10nF 10% 50V 0603
2169	5322 126 11583	10nF 10% 50V 0603

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3100	4822 051 30103	10k 5% 0.062W
3101	4822 116 52304	82k 5% 0.5W
3102	4822 116 52304	82k 5% 0.5W
3103	4822 051 30471	470Ω 5% 0.062W
3104	4822 051 30471	470Ω 5% 0.062W
3105	4822 051 30331	330Ω 5% 0.062W
3106	4822 051 30331	330Ω 5% 0.062W
3107	4822 051 30103	10k 5% 0.062W
3108	4822 051 30102	1k 5% 0.062W
3109	4822 116 52283	4k7 5% 0.5W
3110	4822 050 11002	1k 1% 0.4W
3111	4822 051 30471	470Ω 5% 0.062W
3113	4822 116 83884	47k 5% 0.5W
3120	4822 050 21003	10k 1% 0.6W
3121	4822 051 30101	100Ω 5% 0.062W
3122	4822 116 52175	100Ω 5% 0.5W
3123	4822 116 52175	100Ω 5% 0.5W
3127	4822 050 11002	1k 1% 0.4W
3128	4822 116 52257	22k 5% 0.5W
3150	4822 116 83872	220Ω 5% 0.5W
3151	4822 051 30102	1k 5% 0.062W
3160	4822 051 30103	10k 5% 0.062W
3161	4822 051 30221	220Ω 5% 0.062W
3162	4822 051 30103	10k 5% 0.062W
3163	4822 051 30221	220Ω 5% 0.062W
3168	4822 051 30222	2k2 5% 0.062W
3169	4822 051 30222	2k2 5% 0.062W
3170	4822 116 52283	4k7 5% 0.5W
3171	4822 051 30102	1k 5% 0.062W
3172	4822 117 12063	NTC DC 5W 10k 5%
3180	4822 117 12925	47k 1% 0.063W 0603
3181	4822 051 30221	220Ω 5% 0.062W
3182	4822 051 30221	220Ω 5% 0.062W
3194	4822 117 12917	1Ω 5% 0.062W CASE0603

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5110	4822 157 11706	10µH 5% 2.4X3.4
5191	2422 549 44607	IND FXD SM EMI100mH z 600RR
5192	2422 549 44607	IND FXD SM EMI100mH z 600RR
5193	4822 157 50964	100µH

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6100	4822 130 10852	BZX284-C6V8
6180	4822 130 83092	TLHR4205

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7100	2722 171 07729	VFD 10-BT-242GNK (FTB0)B
7101	3198 010 42310	BC847BW
7102	3198 010 42310	BC847BW
7103	4822 130 40981	BC337-25
7104	4822 130 41246	BC327-25
7105	3198 010 42310	BC847BW
7106	3198 010 42310	BC847BW
7110	3103 165 13731	TMP87C874F/LDCP1
7150	9322 155 82667	IR RECEIVER TSOP2236
7180	4822 130 60854	DTA124EU-W

Front AV Board

Various

1910	2422 026 05301	SOC CINCH V 3P FJPJ1127 B
1911	2422 025 10185	CON BM H 9P M 2.00 PH B
1912	2422 026 05307	CON MDIN H 4P F YKF51 B

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2202	4822 126 14241	0603 50V 330P COL R
2205	4822 126 14241	0603 50V 330P COL R
2206	2238 586 59812	0603 50V 100NP80M

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3201	4822 051 30102	1k 5% 0.062W
3202	4822 051 30105	1M 5% 0.062W
3206	4822 051 30102	1k 5% 0.062W
3207	4822 051 30105	1M 5% 0.062W
3210	4822 116 83868	150Ω 5% 0.5W
3211	4822 051 30759	75Ω 5% 0.062W
3212	4822 051 30759	75Ω 5% 0.062W
3213	4822 051 30759	75Ω 5% 0.062W

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6200	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ
6201	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ
6202	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ
6203	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ
6204	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ

Analog Board

Various

1001▲	2422 086 10919	PROT DEV 65V 125MA MP13
1302▲	4822 252 11215	DSP301N-A21F
1303▲	4822 071 51002	19372(1A)
1304▲	2422 086 10786	FUSE,RADIAL4AMP,
1306▲	2422 086 10919	PROT DEV 65V 125MA MP13
1307▲	2422 086 10954	PROT DEV 65V 1A PSC
1308▲	2422 086 10951	PROT DEV 65V 500MA PSC
1309▲	4822 071 58001	FUSE 800MA PSC
1600	4822 242 10434	L1101-95263-0E1(18,432MHz)
1701	4822 242 81436	OFWK3953M
1702	2422 549 44341	FIL SAW 38MHz 9 OFWK9656M
1703	4822 242 10307	OFWG3956M
1703	4822 242 81436	OFWK3953M
1704	2422 549 44611	FIL CER 5MHz 5 TPSR*MBQ2 BS A
1705	3139 147 17001	TUNER UV1316MK3
1706	4822 242 81572	TPS6,0MB-TF21
1900	4822 265 11154	52030-2210 (22P)
1931▲	2422 030 00304	SOC SUPP AC HOR MALE 9452 B
1932	2422 025 10772	CON BM V 12P M 2.00 PH B
1933	4822 265 11352	CONN. 8P

1940	2422 033 00334	CON BM EURO H 42P F BK GRND-L
1942	2422 025 10769	CON BMT 9P VERT PH-B
1943	4822 267 11031	10P. FEM. V
1945▲	3103 608 50330	UP SUB PCB EURO
1947	4822 265 11154	52030-2210 (22P)
1948	4822 267 10994	4P, MDIN
1949	2422 026 05308	SOC CINCH H 3P F YEWHRD Y
1951	4822 267 31729	CON BM CINCH H1P F BK B
1960	2422 025 09406	CON BM 4P VERT PH-B
1990	4822 242 73552	13,875 000 MHz

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2001	4822 124 80483	47µF 20% 6.3V
2002	2238 586 59812	0603 50V 100NP80M
2003	2238 586 59812	0603 50V 100NP80M
2004	4822 124 80483	47µF 20% 6.3V
2005	4822 124 42234	100µF 20% 6.3V
2006	4822 126 11785	0603 50V 47P PM5
2007	4822 124 21732	10µF 20% 25V
2008	3198 016 31020	0603 25V 1nF
2009	2238 586 59812	0603 50V 100NP80M
2010	4822 124 80483	47µF 20% 6.3V
2011	4822 124 21732	10µF 20% 25V
2012	2238 586 59812	0603 50V 100NP80M
2013	4822 124 42234	100µF 20% 6.3V
2014	2238 586 59812	0603 50V 100NP80M
2015	2238 586 59812	0603 50V 100NP80M
2018	2238 586 59812	0603 50V 100NP80M
2019	2238 586 59812	0603 50V 100NP80M
2020	4822 124 80483	47µF 20% 6.3V
2023	4822 124 80483	47µF 20% 6.3V
2024	4822 126 14225	56pF 5% 50V 0603
2025	3198 016 31020	0603 25V 1nF
2026	4822 126 14225	56pF 5% 50V 0603
2029	4822 124 80483	47µF 20% 6.3V
2031	4822 124 22652	2.2µF 20% 50V
2032	5322 126 11583	10nF 10% 50V 0603
2033	4822 126 13881	470pF 5% 50V
2034	4822 126 13881	470pF 5% 50V
2037	4822 126 13193	4.7nF 10% 63V
2038	4822 126 13193	4.7nF 10% 63V
2039	4822 126 13193	4.7nF 10% 63V
2040	4822 126 13193	4.7nF 10% 63V
2301▲	4822 126 14088	2.2nF 20% 250V
2302▲	4822 121 10512	275V 220nF 20%
2303	4822 122 31175	1nF 10% 500V
2304	4822 126 10206	2.2nF 10% 500V
2305	4822 124 40849	330µF 20% 16V
2306	4822 124 40184	1000µF 20% 10V
2307	4822 122 31175	1nF 10% 500V
2308	4822 121 70386	47nF 10% 250V
2309▲	2222 151 90053	EL 151 400V S 68µF PM20
2310	5322 126 11578	1nF 10% 50V 0603
2311	5322 126 11578	1nF 10% 50V 0603
2312	2020 021 91506	EL ZL 16V S 1000µF PM20 B
2313	4822 124 40184	1000µF 20% 10V
2315▲	4822 126 14525	47pF 5% 1KV
2317	5322 126 11578	1nF 10% 50V 0603
2318	4822 126 10206	2.2nF 10% 500V
2319	4822 124 40849	330µF 20% 16V
2320	4822 124 80791	470µF 16V 20% 105C DXH=8X11.5
2321	2238 586 59812	0603 50V 100NP80M
2322	4822 124 41584	100µF 20% 10V
2323	4822 124 42234	100µF 20% 6.3V
2324	2238 586 59812	0603 50V 100NP80M
2325	4822 124 81151	22µF 50V
2326	4822 121 41857	10nF 5% 250V
2327	2238 586 59812	0603 50V 100NP80M
2328	4822 124 81151	22µF 50V
2329	2238 586 59812	0603 50V 100NP80M
2330	5322 126 11578	1nF 10% 50V 0603
2331	2238 586 59812	0603 50V 100NP80M
2332	4822 124 22651	1.0µF 20% 50V
2334	2238 586 59812	0603 50V 100NP80M
2335	4822 124 21732	10µF 20% 25V
2336	2238 586 59812	0603 50V 100NP80M
2337	4822 122 33741	10pF 10% 50V
2338	2238 586 59812	0603 50V 100NP80M
2339	3198 017 41050	0603 10V 1µF COL R
2340	2020 554 90148	CERSAF NSA 250V S 470P PM20
2341	3198 017 41050	0603 10V 1µF COL R
2342	3198 017 41050	0603 10V 1µF COL R
2402	2238 586 59812	0603 50V 100NP80M
2403	4822 124 80483	47µF 20% 6.3V
2404	2238 586 59812	0603 50V 100NP80M
2405	4822 124 80483	47µF 20% 6.3V
2406	5322 126 11583	10nF 10% 50V 0603
2407	4822 122 33741	10pF 10% 50V
2408	3198 017 41050	0603 10V 1µF COL R
2409	2238 586 59812	0603 50V 100NP80M
2410	3198 017 41050	0603 10V 1µF COL R
2411	2238 586 59812	0603 50V 100NP80M
2412	4822 122 33741	10pF 10% 50V
2413	4822 124 80483	47µF 20% 6.3V
2414	2238 586 59812	0603 50V 100NP80M
2416	3198 017 41050	0603 10V 1µF COL R
2417	4822 124 11947	10µF 20% 16V
2418	3198 017 41050	0603 10V 1µF COL R
2419	3198 017 41050	0603 10V 1µF COL R
2420	2238 586 59812	0603 50V 100NP80M
2421	4822 124 11947	10µF 20% 16V
2422	5322 126 11583	10nF 10% 50V 0603
2423	3198 017 41050	0603 10V 1µF COL R
2424	4822 124 80483	47µF 20% 6.3V
2425	2238 586 59812	0603 50V 100NP80M
2427	3198 017 41050	0603 10V 1µF COL R
2428	4822 124 11947	10µF 20% 16V
2429	4822 124 11946	22µF 20% 16V
2430	2238 586 59812	0603 50V 100NP80M
2432	4822 124 42234	100µF 20% 6.3V
2433	3198 017 34730	0603 16V 47nF COL
2434	4822 124 80483	47µF 20% 6.3V
2435	2238 586 59812	0603 50V 100NP80M
2436	3198 017 41050	0603 10V 1µF COL R
2437	3198 017 41050	0603 10V 1µF COL R
2438	3198 017 41050	0603 10V 1µF COL R
2439	2238 586 59812	0603 50V 100NP80M
2440	3198 017 41050	0603 10V 1µF COL R
2441	3198 017 41050	0603 10V 1µF COL R
2442	4822 124 11946	22µF 20% 16V
2443	4822 124 42234	100µF 20% 6.3V
2444	4822 126 13881	470pF 5% 50V
2445	4822 126 13881	470pF 5% 50V
2446	3198 017 41050	0603 10V 1µF COL R
2447	4822 126 13881	470pF 5% 50V
2448	4822 126 13881	470pF 5% 50V
2449	4822 126 13956	68pF 5% 63V CASE 0603
2450	2238 586 59812	0603 50V 100NP80M
2459	3198 017 41050	0603 10V 1µF COL R
2460	4822 124 40769	4.7µF 20% 100V
2461	4822 124 40769	4.7µF 20% 100V
2462	4822 124 11947	10µF 20% 16V
2463	4822 124 11947	10µF 20% 16V
2464	4822 124 21732	10µF 20% 25V
2501	3198 017 41050	0603 10V 1µF COL R
2502	2238 586 59812	0603 50V 100NP80M
2503	2238 586 59812	0603 50V 100NP80M
2504	3198 017 41050	0603 10V 1µF COL R
2505	3198 017 41050	0603 10V 1µF COL R
2506	3198 017 41050	0603 10V 1µF COL R
2507	3198 017 41050	0603 10V 1µF COL R
2508	3198 017 41050	0603 10V 1µF COL R
2509	2238 586 59812	0603 50V 100NP80M
2510	4822 124 42234	100µF 20% 6.3V
2511	2020 009 90097	EL BP NA 16V S 100µF PM20 A
2512	2238 586 59812	0603 50V 100NP80M
2513	3198 017 41050	0603 10V 1µF COL R
2514	2238 586 59812	0603 50V 100NP80M
2515	3198 017 41050	0603 10V 1µF COL R
2516	2020 009 90097	EL BP NA 16V S 100µF PM20 A
2517	5322 126 11578	1nF 10% 50V 0603
2518	2238 586 59812	0603 50V 100NP80M
2519	4822 124 42234	100µF 20% 6.3V
2520	5322 126 11578	1nF 10% 50V 0603
2521	2238 586 59812	0603 50V 100NP80M
2522	2020 009 90097	EL BP NA 16V S 100µF PM20 A
2523	5322 126 11578	1nF 10% 50V 0603
2524	3198 017 41050	0603 10V 1µF COL R
2525	3198 017 41050	0603 10V 1µF COL R
2526	2020 009 90097	EL BP NA 16V S 100µF PM20 A
2527	5322 126 11578	1nF 10% 50V 0603
2530	2238 586 59812	0603 50V 100NP80M
2535	2238 586 59812	0603 50V 100NP80M
2536	2238 586 59812	0603 50V 100NP80M
2580	2238 586 59812	0603 50V 100NP80M
2581	4822 124 42234	100µF 20% 6.3V
2585	2238 586 59812	0603 50V 100NP80M
2586	5322 126 11578	1nF 10% 50V 0603
2587	3198 017 41050	0603 10V 1µF COL R
2590	4822 122 33753	150pF 5% 50V
2600	4822 124 21732	10µF 20% 25V
2601	5322 126 11583	10nF 10% 50V 0603
2602	4822 124 21732	10µF 20% 25V
2603	2238 586 59812	0603 50V 100NP80M
2604	5322 126 11583	10nF 10% 50V 0603
2605	4822 124 21732	10µF 20% 25V
2606	2238 586 59812	0603 50V 100NP80M
2607	4822 126 14225	56pF 5% 50V 0603
2608	4822 124 21732	10µF 20% 25V
2609	4822 126 14225	56pF 5% 50V 0603
2610	5322 126 11583	10nF 10% 50V 0603
2611	4822 124 80231	47µF 20% 16V
2612	4822 124 40769	4.7µF 20% 100V
2616	5322 126 11578	1nF 10% 50V 0603
2617	5322 126 11578	1nF 10% 50V 0603
2620	3198 016 33380	0603 50V 3P3 COL
2621	3198 016 33380	0603 50V 3P3 COL
2623	2238 586 59812	0603 50V 100NP80M
2626	4822 124 22652	2.2µF 20% 50V
2627	4822 124 22652	2.2µF 20% 50V
2713	4822 124 11946	22µF 20% 16V
2719	4822 126 13883	220pF 5% 50V
2720	4822 124 42234	100µF 20% 6.3V
2721	5322 122 33861	120pF 10% 50V
2722	5322 124 41379	2.2µF 20% 50V
2723	4822 126 13881	470pF 5% 50V
2724	2238 586 59812	0603 50V 100NP80M
2725	4822 122 33761	22pF 5% 50V
2727	2238 586 59812	0603 50V 100NP80M
2728	5322 126 11583	10nF 10% 50V 0603
2729	4822 124 21732	10µF 20% 25V
2730	4822 126 13879	220nF 20% 16V
2731	2020 552 94523	0603 50V 8P2 PM0P5
2732	4822 124 22652	2.2µF 20% 50V
2733	2238 586 59812	0603 50V 100NP80M
2734	5322 126 11578	1nF 10% 50V 0603
2737	4822 124 80483	47µF 20% 6.3V
2740	4822 124 22652	2.2µF 20% 50V
2741	5322 126 11578	1nF 10% 50V 0603
2742	5322 126 11578	1nF 10% 50V 0603
2932	2238 586 59812	0603 50V 100NP80M
2933	4822 124 80483	47µF 20% 6.3V
2934	2238 586 59812	0603 50V 100NP80M
2935	2238 586 59812	0603 50V 100NP80M
2936	4822 122 33761	22pF 5% 50V
2937	4822 122 33761	22pF 5% 50V
2938	2238 586 59812	0603 50V 100NP80M
2940	2238 586 59812	0603 50V 100NP80M
2941	4822 124 21732	10µF 20% 25V
2942	4822 126 14238	0603 50V 2N2 COL R
2943	4822 126 14508	180pF 5% 50V 0603
2944	4822 126 14238	0603 50V 2N2 COL R
2945	4822 126 14508	180pF 5% 50V 0603
2946	3198 017 41050	0603 10V 1µF COL R
2947	3198 017 41050	0603 10V 1µF COL R

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3001	4822 117 13613	2Ω2 5% 0603
3002	4822 117 13613	2Ω2 5% 0603
3003	4822 051 30103	10k 5% 0.062W
3004	4822 117 12139	22Ω 5% 0.062W
3005	4822 117 12139	22Ω 5% 0.062W
3006	4822 117 12139	22Ω 5% 0.062W
3007	4822 117 12925	47k 1% 0.063W 0603
3008	4822 051 30102	1k 5% 0.062W
3009	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3010	4822 117 13632	100k 1% 0603 0.62W
3011	4822 117 12917	1Ω 5% 0.062W CASE0603
3012	5322 117 13047	330Ω 1% 0.063W 0603 RC22H
3013	4822 117 12139	22Ω 5% 0.062W
3014	4822 051 30103	10k 5% 0.062W
3015	4822 117 13613	2Ω2 5% 0603
3017	4822 117 13613	2Ω2 5% 0603
3018	4822 117 12139	22Ω 5% 0.062W
3019	4822 117 12139	22Ω 5% 0.062W
3020	4822 117 12139	22Ω 5% 0.062W
3024	4822 117 12925	47k 1% 0.063W 0603
3026	4822 117 12925	47k 1% 0.063W 0603
3027	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3029	4822 117 12917	1Ω 5% 0.062W CASE0603
3030	5322 117 13047	330Ω 1% 0.063W 0603 RC22H
3034	4822 117 12925	47k 1% 0.063W 0603
3035	4822 050 21003	10k 1% 0.6W
3039	4822 050 21003	10k 1% 0.6W
3041	4822 050 21003	10k 1% 0.6W
3043	4822 117 12139	22Ω 5% 0.062W
3044	4822 051 30472	4k7 5% 0.062W
3045	4822 117 13632	100k 1% 0603 0.62W
3046	4822 051 30471	470Ω 5% 0.062W
3047	4822 117 13632	100k 1% 0603 0.62W
3048	4822 051 30101	100Ω 5% 0.062W
3049	4822 051 30472	4k7 5% 0.062W
3050	4822 117 13632	100k 1% 0603 0.62W
3051	4822 051 30223	22k 5% 0.062W
3052	4822 051 30332	3k3 5% 0.062W
3053	4822 117 13632	100k 1% 0603 0.62W
3054	4822 051 30332	3k3 5% 0.062W
3300▲	4822 053 21335	3M3 5% 0.5W

3301▲	4822 053 21335	3M3 5% 0.5W
3302	4822 051 30102	1k 5% 0.062W
3303	4822 051 30102	1k 5% 0.062W
3304▲	4822 051 30103	10k 5% 0.062W
3305▲	4822 053 21684	680k 5% 0.5W
3306	4822 116 83872	220Ω 5% 0.5W
3307	4822 051 30103	10k 5% 0.062W
3308	4822 116 52272	330k 5% 0.5W
3309	4822 116 52272	330k 5% 0.5W
3310	4822 116 52272	330k 5% 0.5W
3311	4822 051 30102	1k 5% 0.062W
3312	4822 051 30221	220Ω 5% 0.062W
3313	4822 116 52234	100k 5% 0.5W
3314	4822 117 13611	1k 1% 0603 ERJ3Ω
3315	4822 117 12902	8k2 1% 0.063W 0603
3316	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3317	4822 051 30102	1k 5% 0.062W
3318	4822 116 52175	100Ω 5% 0.5W
3321	2322 193 14477	RST MFLM PR01 A 0Ω47 PM5 A
3323	4822 117 12891	220k 1% ERJ3Ω
3324	2322 702 60564	RST SMD 0603 560k 5%
3325	4822 117 12925	47k 1% 0.063W 0603
3326▲	4822 116 52175	100Ω 5% 0.5W
3327	4822 051 30105	1M 5% 0.062W
3328	4822 051 30103	10k 5% 0.062W
3329	3198 021 32250	RST SM 0603 2M 2 PM5 COL R
3330	4822 051 30471	470Ω 5% 0.062W
3331	4822 051 30109	10Ω 5% 0.062W
3332	2120 108 93941	RST SM 0603 MCR03 5k62 PM1 R
3333	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3335	4822 051 30471	470Ω 5% 0.062W
3336	4822 051 30471	470Ω 5% 0.062W
3337	4822 051 30102	1k 5% 0.062W
3338	4822 051 30221	220Ω 5% 0.062W
3339	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3340	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3341	4822 051 30683	68k 5% 0.062W
3342	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3343	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3344	4822 051 30683	68k 5% 0.062W
3346	4822 051 30222	2k2 5% 0.062W
3347	4822 051 30472	4k7 5% 0.062W
3348	4822 051 30681	680Ω 5% 0.062W
3349	4822 051 30479	47Ω 5% 0.062W
3350	4822 051 30102	1k 5% 0.062W
3351	2322 702 60564	RST SMD 0603 560k 5%
3352	2322 193 14687	RST MFLM PR01 A 0Ω68 PM5
3353	4822 051 30272	2k7 5% 0.062W
3354	4822 051 30272	2k7 5% 0.062W
3355	4822 051 30479	47Ω 5% 0.062W
3356	4822 116 52228	680Ω 5% 0.5W
3357	4822 051 30472	4k7 5% 0.062W
3358	4822 051 30109	10Ω 5% 0.062W
3360	4822 116 52231	820Ω 5% 0.5W
3361	4822 051 30102	1k 5% 0.062W
3362	4822 051 30681	680Ω 5% 0.062W
3363	4822 051 30222	2k2 5% 0.062W
3364	4822 051 30103	10k 5% 0.062W
3365	4822 051 30332	3k3 5% 0.062W
3366	4822 051 30152	1k5 5% 0.063W 0603
3367	4822 117 12903	1k8 1% 0.063W 0603
3368	4822 051 30332	3k3 5% 0.062W
3371	4822 051 30479	47Ω 5% 0.062W
3372	4822 051 30339	33Ω 5% 0.062W
3373	4822 051 30339	33Ω 5% 0.062W
3401	4822 051 30152	75Ω 1% 0.062W
3402	4822 051 30152	75Ω 1% 0.062W
3403	4822 051 30152	75Ω 1% 0.062W
3404	4822 051 30759	75Ω 5% 0.062W
3405	4822 051 30223	22k 5% 0.062W
3406	4822 117 12891	220k 1% ERJ3Ω
3407	4822 051 30332	3k3 5% 0.062W
3408	4822 051 30392	3k9 5% 0.063W 0603
3409	4822 051 30152	75Ω 1% 0.062W
3410	4822 051 30152	75Ω 1% 0.062W
3411	4822 051 30759	75Ω 5% 0.062W
3412	4822 116 52201	75Ω 5% 0.5W
3413	4822 051 30152	75Ω 1% 0.062W
3414	4822 051 30759	75Ω 5% 0.062W
3415	4822 051 30102	1k 5% 0.062W
3416	4822 051 30472	4k7 5% 0.062W
3417	4822 051 30759	75Ω 5% 0.062W
3418	4822 117 13632	100k 1% 0603 0.62W
3419	4822 051 30223	22k 5% 0.062W
3420	4822 051 30151	150Ω 5% 0.062W
3421	4822 051 30273	27k 5% 0.062W
3422	4822 116 52231	820Ω 5% 0.5W
3423	4822 051 30391	390Ω 5% 0.062W
3424	4822 051 30333	33k 5% 0.062W
3425	4822 051 30471	470Ω 5% 0.062W
3426	4822 051 30333	33k 5% 0.062W
3427	4822 051 30759	75Ω 5% 0.062W
3428	4822 117 13632	100k 1% 0603 0.62W
3429	4822 117 12925	47k 1% 0.063W 0603
3431	4822 051 30472	4k7 5% 0.062W
3432	4822 116 52175	100Ω 5% 0.5W
3433	4822 116 52175	100Ω 5% 0.5W
3434	4822 116 52283	4k7 5% 0.5W
3435	4822 116 52201	75Ω 5% 0.5W
3436	4822 116 52199	68Ω 5% 0.5W
3437	4822 051 30103	10k 5% 0.062W
3438	4822 051 30103	10k 5% 0.062W
3439	4822 051 30103	10k 5% 0.062W
3440	4822 051 30103	10k 5% 0.062W
3441	4822 116 52201	75Ω 5% 0.5W
3442	4822 051 30154	150k 5% 0.062W
3443	4822 117 13632	100k 1% 0603 0.62W
3444	4822 117 13632	100k 1% 0603 0.62W
3445	4822 051 30151	150Ω 5% 0.062W
3446	4822 117 12925	47k 1% 0.063W 0603
3447	4822 116 83884	47k 5% 0.5W
3448	4822 051 30471	470Ω 5% 0.062W
3449	4822 051 30151	150Ω 5% 0.062W
3450	4822 051 30471	470Ω 5% 0.062W
3451	4822 050 21003	10k 1% 0.6W
3452	4822 051 30151	150Ω 5% 0.062W
3454	4822 050 11002	1k 1% 0.4W
3455	4822 051 30103	10k 5% 0.062W
3458	4822 051 30472	4k7 5% 0.062W
3459	4822 051 30103	10k 5% 0.062W
3460	4822 051 30472	4k7 5% 0.062W
3461	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR
3462	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR
3463	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR
3464	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR
3465	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR
3466	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR
3467	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR
3468	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR
3469	4822 117 13632	100k 1% 0603 0.62W
3470	4822 117 13632	100k 1% 0603 0.62W
3471	4822 117 13632	100k 1% 0603 0.62W
3472	4822 117 13632	100k 1% 0603 0.62W
3473	4822 051 30101	100Ω 5% 0.062W
3474	4822 051 30101	100Ω 5% 0.062W
3475	4822 051 30101	100Ω 5% 0.062W
3476	4822 051 30101	100Ω 5% 0.062W
3477	4822 051 30101	100Ω 5% 0.062W
3478	4822 051 30101	100Ω 5% 0.062W
3487	4822 117 13632	100k 1% 0603 0.62W
3488	4822 117 13632	100k 1% 0603 0.62W
3489	4822 117 12864	82k 5% 0.6W
3490	4822 051 30151	150Ω 5% 0.062W
3491	4822 051 30151	150Ω 5% 0.062W
3492	4822 051 30151	150Ω 5% 0.062W
3493	4822 051 30151	150Ω 5% 0.062W
3494	4822 051 30151	150Ω 5% 0.062W
3495	4822 051 30472	4k7 5% 0.062W
3496	4822 051 30472	4k7 5% 0.062W
3501	4822 051 30102	1k 5% 0.062W
3502	4822 050 11002	1k 1% 0.4W
3503	4822 117 13632	100k 1% 0603 0.62W
3504	4822 117 13632	100k 1% 0603 0.62W
3505	4822 117 13632	100k 1% 0603 0.62W
3506	4822 117 13632	100k 1% 0603 0.62W
3507	4822 117 13632	100k 1% 0603 0.62W
3508	4822 051 30102	1k 5% 0.062W
3509	4822 050 11002	1k 1% 0.4W
3510	4822 117 13632	100k 1% 0603 0.62W
3511	4822 117 13632	100k 1% 0603 0.62W
3512	4822 051 30102	1k 5% 0.062W
3513	4822 051 30102	1k 5% 0.062W
3514	4822 117 13632	100k 1% 0603 0.62W
3515	4822 050 11002	1k 1% 0.4W
3516	4822 117 13632	100k 1% 0603 0.62W
3517	4822 116 52283	4k7 5% 0.5W
3518	4822 051 30102	1k 5% 0.062W
3519	4822 116 52283	4k7 5% 0.5W
3520	4822 051 30221	220Ω 5% 0.062W
3521	4822 051 30221	220Ω 5% 0.062W
3522	4822 051 30221	220Ω 5% 0.062W
3523	4822 050 11002	1k 1% 0.4W
3524	4822 117 12968	820Ω 5% 0.62W
3525	4822 051 30221	220Ω 5% 0.062W
3526	4822 051 30102	1k 5% 0.062W
3527	4822 117 12968	820Ω 5% 0.62W
3528	4822 051 30472	4k7 5% 0.062W
3529	4822 051 30472	4k7 5% 0.062W
3530	4822 117 12968	820Ω 5% 0.62W
3531	4822 117 12968	820Ω 5% 0.62W
3532	4822 050 11002	1k 1% 0.4W
3533	4822 050 11002	1k 1% 0.4W
3534	4822 117 13632	100k 1% 0603 0.62W
3580	4822 051 30759	75Ω 5% 0.062W
3581	4822 051 30222	2k2 5% 0.062W
3582	4822 051 30331	330Ω 5% 0.062W
3584	4822 051 30471	470Ω 5% 0.062W
3585	4822 051 30561	560Ω 5% 0.062W
3600	4822 051 30103	10k 5% 0.062W
3601	4822 116 52175	100Ω 5% 0.5W
3602	4822 051 30472	4k7 5% 0.062W
3603	4822 116 52175	100Ω 5% 0.5W
3606	4822 051 30102	1k 5% 0.062W
3607	4822 051 30102	1k 5% 0.062W
3611	4822 051 30101	100Ω 5% 0.062W
3612	4822 051 30101	100Ω 5% 0.062W
3701	4822 116 52228	680Ω 5% 0.5W
3702	4822 051 30471	470Ω 5% 0.062W
3703	4822 116 52245	150k 5% 0.5W
3704	4822 051 30221	220Ω 5% 0.062W
3705	4822 051 30103	10k 5% 0.062W
3710	4822 051 30562	5k6 5% 0.063W 0603 RC21 RST SM
3711	4822 051 30333	33k 5% 0.062W
3714	4822 051 30183	18k 5% 0.062W
3715	4822 051 30103	10k 5% 0.062W
3716	4822 051 30472	4k7 5% 0.062W
3717	4822 051 30472	4k7 5% 0.062W
3720	4822 051 30331	330Ω 5% 0.062W
3724	4822 100 12158	22k 30%
3725	4822 117 12902	8k2 1% 0.063W 0603
3726	4822 051 30101	100Ω 5% 0.062W
3727	4822 117 12917	1Ω 5% 0.062W CASE0603
3728	4822 051 30101	100Ω 5% 0.062W
3729	4822 117 12917	1Ω 5% 0.062W CASE0603
3730	4822 051 30472	4k7 5% 0.062W
3731	4822 051 30271	270Ω 5% 0.062W
3731	4822 051 30331	330Ω 5% 0.062W
3732	4822 051 30102	1k 5% 0.062W
3733	4822 051 30472	4k7 5% 0.062W
3734	4822 051 30272	2k7 5% 0.062W
3735	4822 051 30332	3k3 5% 0.062W
3736	4822 051 30331	330Ω 5% 0.062W
3737	4822 051 30222	2k2 5% 0.062W
3738	4822 051 30682	6k8 5% 0.062W
3739	4822 051 30562	5k6 5% 0.063W 0603 RC21 RST SM
3740	4822 051 30681	680Ω 5% 0.062W
3741	4822 051 30472	4k7 5% 0.062W
3742	4822 051 30472	4k7 5% 0.062W
3743	4822 051 30563	56k 5% 0.062W
3744	4822 117 13632	100k 1% 0603 0.62W
3745	4822 051 30562	5k6 5% 0.063W 0603 RC21 RST SM
3746	4822 051 30562	5k6 5% 0.063W 0603 RC21 RST SM
3758	4822 051 30103	10k 5% 0.062W
3931	4822 117 12925	47k 1% 0.063W 0603
3932	4822 117 12925	47k 1% 0.063W 0603
3933	4822 117 12925	47k 1% 0.063W 0603
3934	4822 051 30101	100Ω 5% 0.062W
3935	4822 051 30101	100Ω 5% 0.062W
3936	4822 051 30103	10k 5% 0.062W
3937	4822 051 30222	2k2 5% 0.062W
3938	4822 051 30222	2k2 5% 0.062W
3939	4822 051 30472	4k7 5% 0.062W
3940	3198 021 31060	RST SM 0603 10M PM5COL R
3941	3198 021 31060	RST SM 0603 10M PM5COL R
3942	4822 051 30333	33k 5% 0.062W
3943	4822 051 30333	33k 5% 0.062W
3944	4822 051 30333	33k 5% 0.062W
3945	4822 051 30333	33k 5% 0.062W
3946	4822 051 30333	33k 5% 0.062W
3947	4822 051 30333	33k 5% 0.062W
3948	4822 051 30472	4k7 5% 0.062W
3950	4822 117 13632	100k 1% 0603 0.62W
3951	4822 051 30223	22k 5% 0.062W
3952	4822 051 30153	15k 5% 0.062W
3953	4822 051 30472	4k7 5% 0.062W
3954	4822 051 30472	4k7 5% 0.062W
3955	4822 051 30103	10k 5% 0.062W

5001	4822 157 11074	100µH
5300▲	2422 531 02546	TFM SMT SLOT SRW28EC9-E01V0* B

5302▲	2422 549 44509	MAINS 25mH 0A4 HF2022R Y
5304	4822 157 70826	2.4µH
5305	4822 157 70826	2.4µH
5306	2422 535 94634	IND FXD LHL08 S 2U2 PM20 A
5307	4822 157 11737	22µH 10% 9X9.5
5308	4822 157 11737	22µH 10% 9X9.5
5309	4822 157 11737	22µH 10% 9X9.5
5401	4822 157 11706	10µH 5% 2.4X3.4
5402	4822 157 11706	10µH 5% 2.4X3.4
5403	4822 157 11706	10µH 5% 2.4X3.4
5404	4822 157 11706	10µH 5% 2.4X3.4
5406	4822 157 11706	10µH 5% 2.4X3.4
5580	2422 536 00019	TRANSFORMER 6RG (SAGA) B
5581	4822 157 11706	10µH 5% 2.4X3.4
5600▲	4822 157 11706	10µH 5% 2.4X3.4
5601▲	4822 157 11706	10µH 5% 2.4X3.4
5602▲	4822 157 11706	10µH 5% 2.4X3.4
5705	4822 157 11139	6.8µH 5%
5709	4822 157 11139	6.8µH 5%
5710	2422 549 44162	IND VAR 7MM Y 77M8 B
5711	2422 549 44162	IND VAR 7MM Y 77M8 B
5713	4822 157 11747	15µH 5%
5714	4822 157 11747	15µH 5%
5931	4822 157 11706	10µH 5% 2.4X3.4
5932	4822 157 11074	100µH

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6001	4822 130 83757	MCL4148
6002	4822 130 83757	MCL4148
6003	4822 130 83757	MCL4148
6300	9322 182 65682	DIO REC STTH302-C2 (ST00) B
6301	4822 130 31603	1N4006
6302	4822 130 31603	1N4006
6303	9322 182 65682	DIO REC STTH302-C2 (ST00) B
6304	4822 130 31878	1N4003G
6305	4822 130 31603	1N4006
6306	4822 130 31603	1N4006
6307	9322 161 77682	DIO REC SB540L-7024 (GI00) B
6308	9322 161 77682	DIO REC SB540L-7024 (GI00) B
6309	9322 126 71673	DIO REC BYT42M A (TEG0) A
6310	9322 182 65682	DIO REC STTH302-C2 (ST00) B
6311	4822 130 31878	1N4003G
6312	9322 129 38685	DIO REG SM BZM55-C6V8 (TEG0)
6313	4822 130 10871	SBYV27-200
6314	9322 129 39685	BZM55-C8V2
6315	4822 130 83757	MCL4148
6316	4822 130 30842	BAV21
6317	4822 130 42488	BYD33D
6318	3198 010 53390	DIO REG BZX79-B33 A COL A
6319	4822 130 42488	BYD33D
6320	4822 130 11397	BAS316
6321	4822 130 10654	BAT254
6322	9322 129 38685	DIO REG SM BZM55-C6V8 (TEG0)
6324	4822 130 82346	BZV55-C27
6325	4822 130 10871	SBYV27-200
6401	9340 548 61115	DIO REG SM PDZ12B (PHSE) R
6402	9340 548 61115	DIO REG SM PDZ12B (PHSE) R
6403	9340 548 61115	DIO REG SM PDZ12B (PHSE) R
6404	9340 548 61115	DIO REG SM PDZ12B (PHSE) R
6409	9322 129 38685	DIO REG SM BZM55-C6V8 (TEG0)
6414	9322 129 38685	DIO REG SM BZM55-C6V8 (TEG0)
6415	9340 548 61115	DIO REG SM PDZ12B (PHSE) R
6416	9340 548 61115	DIO REG SM PDZ12B (PHSE) R
6417	9340 548 61115	DIO REG SM PDZ12B (PHSE) R
6418	9340 548 61115	DIO REG SM PDZ12B (PHSE) R
6419	9340 548 61115	DIO REG SM PDZ12B (PHSE) R
6420	9340 548 61115	DIO REG SM PDZ12B (PHSE) R
6422	9322 129 34685	DIO REG SM BZM55-C3V9 (TEGO)
6423	9340 548 61115	DIO REG SM PDZ12B (PHSE) R
6424	9340 548 61115	DIO REG SM PDZ12B (PHSE) R
6425	9340 548 61115	DIO REG SM PDZ12B (PHSE) R
6426	9340 548 61115	DIO REG SM PDZ12B (PHSE) R
6427	9340 548 61115	DIO REG SM PDZ12B (PHSE) R
6428	9340 548 61115	DIO REG SM PDZ12B (PHSE) R
6429	9340 548 61115	DIO REG SM PDZ12B (PHSE) R
6600	4822 130 83757	MCL4148
6703	9340 552 30115	DIO SIG SM BA591 (PHSE)
6704	9340 552 30115	DIO SIG SM BA591 (PHSE)
6705	9340 552 30115	DIO SIG SM BA591 (PHSE)

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7001	9352 668 47118	IC SM UDA1334BTS/N2 (PHSE) R
7002	4822 209 62312	MC33078D
7003	4822 130 60854	DTA124EU-W
7005	9352 670 99118	IC SM UDA1361TS/N1 (PHSE) R
7006	3198 010 42320	BC857BW
7008	3198 010 42310	BC847BW
7009	3198 010 42310	BC847BW
7010	4822 130 61553	DTC124EU
7011	3198 010 42320	BC857BW
7301	4822 209 14933	TL431IZ
7302	9322 163 75685	FET SIG SM SI2306DS(VISH)
7303	9322 183 38668	FET POW SM STS9NF30L (ST00)
7304	4822 209 14933	TL431IZ
7305	4822 209 14933	TL431IZ
7306	4822 130 61553	DTC124EU
7307	9322 157 37687	FET POW STP3NC60FP (ST00) L
7308	4822 130 61553	DTC124EU
7309	9322 180 12685	FET POW SM SI2312DS (VISH) R
7310	3198 010 42310	BC847BW
7311	3198 010 42310	BC847BW
7312	4822 130 41782	BF422
7313	9352 673 56112	IC TEA1507P/N1 (PHSE) L
7314▲	9965 000 09548	PHOTOCOUPLER TCET1108G VISHAY
7315	4822 209 14933	TL431IZ
7317	9322 163 75685	FET SIG SM SI2306DS(VISH)
7318	9322 163 75685	FET SIG SM SI2306DS(VISH)
7319	5322 130 60159	BC846B
7320	9322 163 75685	FET SIG SM SI2306DS(VISH)
7321	4822 130 61553	DTC124EU
7322	3198 010 42320	BC857BW
7401	3198 010 42320	BC857BW
7402	3198 010 42310	BC847BW
7403	3198 010 42320	BC857BW
7404	3198 010 42320	BC857BW
7405	3198 010 42310	BC847BW
7406	3198 010 42320	BC857BW
7407	3198 010 42310	BC847BW
7408	9322 173 41668	IC SM ST6618 (ST00)R
7409	3198 010 42310	BC847BW
7410	9965 000 03392	NJM2267M
7411	9322 179 71668	IC SM NJM2285M (JRC0) R
7412	4822 130 61553	DTC124EU
7415	4822 130 42804	BC817-25
7416	4822 130 42804	BC817-25
7419	9340 560 36235	BSH111
7420	9340 560 36235	BSH111
7421	3198 010 42310	BC847BW
7501	5322 209 11102	HEF4052BT
7502	4822 209 32071	MC33079D
7503	5322 209 11102	HEF4052BT
7504	5322 209 11102	HEF4052BT
7505	4822 209 62312	MC33078D
7506	4822 130 42804	BC817-25
7508	4822 130 42804	BC817-25
7509	4822 130 42804	BC817-25
7511	4822 130 42804	BC817-25
7580	5322 209 11517	PC74HCU04T
7600	9322 167 63668	IC SM MSP3415G-QG-B8 (MIAS) R
7701	4822 130 61553	DTC124EU
7702	4822 130 61553	DTC124EU
7704	4822 130 61553	DTC124EU
7705	4822 130 61553	DTC124EU
7706	4822 130 61553	DTC124EU
7710	9352 606 11118	IC SM TDA9818T/V1(PHSE) R
7710	9352 621 13118	IC SM TDA9817T/V1(PHSE) R
7711	3198 010 42320	BC857BW
7712	4822 130 61553	DTC124EU
7713	3198 010 42320	BC857BW
7714	3198 010 42310	BC847BW
7716	3198 010 42320	BC857BW
7717	5322 130 42755	BC847C
7931	4822 209 17505	STV5348D
7932	3198 010 42310	BC847BW
7933	3198 010 42310	BC847BW
7934	4822 209 60177	LM339D

UPC12 Sub PWB

Various

1801	2422 543 01115	RES XTL SM 24M576 12P CX-11F R
1805	4822 242 70938	TA252E00 (32,768KHZ)
1980	2422 025 17723	CON BM V 8P M2.00 C36 B
1984	2422 025 17723	CON BM V 8P M2.00 C36 B
1986	2422 025 16677	CON BM H 10P F 1.00 FFC SMT R
1987	2422 025 17723	CON BM V 8P M2.00 C36 B
1988	2422 025 17723	CON BM V 8P M2.00 C36 B

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2800	2238 586 59812	0603 50V 100NP80M
2801	4822 122 33752	15pF 5% 50V
2802	4822 122 33752	15pF 5% 50V
2803	2238 586 59812	0603 50V 100NP80M
2804	2238 586 59812	0603 50V 100NP80M
2805	2238 586 59812	0603 50V 100NP80M
2806	2238 586 59812	0603 50V 100NP80M
2807	4822 126 13879	220nF 20% 16V
2808	2238 586 59812	0603 50V 100NP80M
2809	2238 586 59812	0603 50V 100NP80M
2810	4822 122 33741	10pF 10% 50V
2811	4822 122 33741	10pF 10% 50V
2812	5322 126 11583	10nF 10% 50V 0603
2813	4822 122 33741	10pF 10% 50V
2814	4822 122 33741	10pF 10% 50V
2815	4822 126 13883	220pF 5% 50V
2816	4822 124 11968	220mF 20% 5.5V
2817	2238 586 59812	0603 50V 100NP80M
2818	4822 126 13883	220pF 5% 50V
2819	4822 124 42234	100µF 20% 6.3V
2820	5322 126 11583	10nF 10% 50V 0603
2821	5322 126 11583	10nF 10% 50V 0603
2822	2238 586 59812	0603 50V 100NP80M
2823	5322 126 11578	1nF 10% 50V 0603
2824	3198 017 41050	0603 10V 1µF COL R
2825	2020 552 94427	0603 50V 100P PM5 R
2828	2238 586 59812	0603 50V 100NP80M
2829	4822 124 21732	10µF 20% 25V
2830	2238 586 59812	0603 50V 100NP80M
2831	5322 126 11583	10nF 10% 50V 0603

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3800	4822 051 30223	22k 5% 0.062W
3801	4822 051 30103	10k 5% 0.062W
3802	4822 051 30223	22k 5% 0.062W
3803	4822 051 30102	1k 5% 0.062W
3804	4822 051 30103	10k 5% 0.062W
3805	4822 051 30101	100Ω 5% 0.062W
3806	4822 051 30223	22k 5% 0.062W
3807	4822 117 13632	100k 1% 0603 0.62W
3808	4822 117 13632	100k 1% 0603 0.62W
3809	4822 117 13632	100k 1% 0603 0.62W
3810	4822 117 13632	100k 1% 0603 0.62W
3811	4822 051 30101	100Ω 5% 0.062W
3812	4822 051 30223	22k 5% 0.062W
3813	4822 051 30103	10k 5% 0.062W
3814	4822 051 30103	10k 5% 0.062W
3815	4822 051 30183	18k 5% 0.062W
3816	4822 051 30103	10k 5% 0.062W
3817	4822 051 30103	10k 5% 0.062W
3818	4822 051 30103	10k 5% 0.062W
3819	4822 051 30103	10k 5% 0.062W
3820	4822 051 30102	1k 5% 0.062W
3821	4822 051 30103	10k 5% 0.062W
3822	4822 051 30103	10k 5% 0.062W

3823	4822 117 13632	100k 1% 0603 0.62W
3824	4822 051 30102	1k 5% 0.062W
3825	4822 051 30101	100Ω 5% 0.062W
3826	4822 051 30102	1k 5% 0.062W
3827	4822 051 30102	1k 5% 0.062W
3828	4822 051 30103	10k 5% 0.062W
3829	4822 051 30103	10k 5% 0.062W
3830	4822 051 30102	1k 5% 0.062W
3831	4822 051 30102	1k 5% 0.062W
3832	4822 051 30333	33k 5% 0.062W
3833	4822 051 30102	1k 5% 0.062W
3834	4822 051 30102	1k 5% 0.062W
3835	4822 051 30102	1k 5% 0.062W
3836	4822 051 30101	100Ω 5% 0.062W
3837	4822 051 30123	12k 5% 0.062W
3838	4822 051 30102	1k 5% 0.062W
3839	4822 051 30273	27k 5% 0.062W
3840	4822 051 30472	4k7 5% 0.062W
3841	4822 117 13632	100k 1% 0603 0.62W
3842	4822 117 12891	220k 1% ERJ3Ω
3843	4822 051 30333	33k 5% 0.062W
3844	4822 051 30221	220Ω 5% 0.062W
3845	4822 051 30102	1k 5% 0.062W
3846	4822 051 30333	33k 5% 0.062W
3847	4822 051 30103	10k 5% 0.062W
3849	4822 117 12925	47k 1% 0.063W 0603
3850	4822 051 30183	18k 5% 0.062W
3851	4822 051 30103	10k 5% 0.062W
3852	4822 051 30103	10k 5% 0.062W
3854	4822 051 30103	10k 5% 0.062W
3855	4822 051 30471	470Ω 5% 0.062W
3856	4822 051 30103	10k 5% 0.062W
3857	4822 051 30103	10k 5% 0.062W
3858	4822 117 13632	100k 1% 0603 0.62W
3860	4822 051 30222	2k2 5% 0.062W
3861	3198 021 32250	RST SM 0603 2M 2 PM5 COL R
3862	4822 051 30103	10k 5% 0.062W
3863	4822 117 13608	4.7Ω 5% 0603 0.0016W
3864	4822 117 13608	4.7Ω 5% 0603 0.0016W
3865	4822 117 13608	4.7Ω 5% 0603 0.0016W
3866	4822 117 13608	4.7Ω 5% 0603 0.0016W
3867	4822 051 30759	75Ω 5% 0.062W
3868	4822 051 30103	10k 5% 0.062W
3869	4822 051 30331	330Ω 5% 0.062W
3870	4822 117 13632	100k 1% 0603 0.62W
3871	4822 051 30103	10k 5% 0.062W
3872	4822 051 30103	10k 5% 0.062W
3873	4822 051 30472	4k7 5% 0.062W
3876	4822 051 30103	10k 5% 0.062W
3878	4822 051 30102	1k 5% 0.062W
3879	4822 051 30102	1k 5% 0.062W
3881	4822 117 12925	47k 1% 0.063W 0603
3882	4822 117 12925	47k 1% 0.063W 0603
3884	4822 051 30101	100Ω 5% 0.062W
3885	4822 051 30101	100Ω 5% 0.062W
3886	4822 051 30472	4k7 5% 0.062W
3887	4822 051 30472	4k7 5% 0.062W
3888	4822 051 30471	470Ω 5% 0.062W
3889	4822 051 30183	18k 5% 0.062W
3916	4822 051 30273	27k 5% 0.062W
3917	2322 704 65603	RST SM 0603 RC22H 56k PM1 R
3919	5322 117 13024	33k 1% 0.063W 0603 RC22H
3920	4822 051 30562	5k6 5% 0.063W 0603 RC21 RST SM
3921	4822 051 30471	470Ω 5% 0.062W
3922	4822 051 30102	1k 5% 0.062W
3923	4822 051 30103	10k 5% 0.062W
3925	4822 117 12706	10k 1% 0.063W CASE0603 RC22H
3927	4822 117 12864	82k 5% 0.6W

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5801	2422 549 44607	IND FXD SM EMI100mH z 600RR
5802	2422 549 44607	IND FXD SM EMI100mH z 600RR
5803	2422 549 44607	IND FXD SM EMI100mH z 600RR
5804	2422 549 44607	IND FXD SM EMI100mH z 600RR

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6800	4822 130 11397	BAS316
6801	9322 129 34685	DIO REG SM BZM55-C3V9 (TEGO)
6802	4822 130 10654	BAT254
6803	4822 130 10654	BAT254
6804	4822 130 10654	BAT254
6901	5322 130 34331	BAV70
6903	5322 130 34331	BAV70

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7801	9352 190 00118	IC SM 74LVC573AD (PHSE) R
7802	4822 130 61553	DTC124EU
7803	9322 131 96668	IC SM CY62128VL-70SC (CYPR) R
7804	3103 165 13721	IC TMP91CW12AF/LIRP1
7805	9965 000 13398	M29W800AT-80N1/ AN110021
7806	9322 163 26685	IC SM NCP301LSN30 (ONSE) R
7807	4822 209 73852	PMBT2369
7808	4822 209 16907	M24C16-MN6T
7813	3198 010 42310	BC847BW
7814	3198 010 42310	BC847BW
7815	3198 010 42310	BC847BW
7816	3198 010 42310	BC847BW
7817	3198 010 42310	BC847BW
7818	4822 130 60854	DTA124EU-W
7821	9340 560 36235	BSH111
7822	9340 560 36235	BSH111
7825	8203 107 03690	IC LA7213
7902	5322 209 82941	LM358D

DVIO PWB DVDR890

Various

1101	2422 025 17106	CON BM H 4P F 0.8 IEEE R
1102	2422 543 01115	RES XTL SM 24M576 12P CX-11F R
1200	2422 543 01159	RES XTL SM 11M0592 20P DSX840
1500	2422 025 17084	CON BM V 60P F 0.80 179161 R

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2146	2238 586 59812	0603 50V 100NP80M
2147	2238 586 59812	0603 50V 100NP80M
2148	2238 586 59812	0603 50V 100NP80M
2149	2238 586 59812	0603 50V 100NP80M
2150	2238 586 59812	0603 50V 100NP80M
2151	2238 586 59812	0603 50V 100NP80M
2152	2238 586 59812	0603 50V 100NP80M
2153	2238 586 59812	0603 50V 100NP80M
2154	2238 586 59812	0603 50V 100NP80M
2155	2238 586 59812	0603 50V 100NP80M
2156	2238 586 59812	0603 50V 100NP80M
2157	2238 586 59812	0603 50V 100NP80M
2158	3198 017 41050	0603 10V 1µF COL R
2163	4822 126 14506	270pF 5% 50V 0603
2170	4822 126 11663	12pF
2171	4822 126 11663	12pF
2173	4822 124 23002	10µF 16V
2174	2238 586 59812	0603 50V 100NP80M
2175	4822 124 23002	10µF 16V
2176	2238 586 59812	0603 50V 100NP80M
2177	2238 586 59812	0603 50V 100NP80M
2178	2238 586 59812	0603 50V 100NP80M
2181	4822 124 12095	100µF 20% 16V
2182	4822 124 23002	10µF 16V
2183	2238 586 59812	0603 50V 100NP80M
2184	2238 586 59812	0603 50V 100NP80M
2187	2238 586 59812	0603 50V 100NP80M
2192	2238 586 59812	0603 50V 100NP80M
2193	2238 586 59812	0603 50V 100NP80M
2194	2238 586 59812	0603 50V 100NP80M
2195	2238 586 59812	0603 50V 100NP80M
2196	2238 586 59812	0603 50V 100NP80M
2197	2238 586 59812	0603 50V 100NP80M
2200	4822 126 11663	12pF
2202	2238 586 59812	0603 50V 100NP80M
2203	2238 586 59812	0603 50V 100NP80M
2204	2238 586 59812	0603 50V 100NP80M
2205	4822 126 11663	12pF
2206	2020 552 94427	0603 50V 100P PM5 R
2207	2238 586 59812	0603 50V 100NP80M
2301	2238 586 59812	0603 50V 100NP80M
2302	4822 124 80151	47µF 16V
2303	2238 586 59812	0603 50V 100NP80M
2304	2238 586 59812	0603 50V 100NP80M
2305	2238 586 59812	0603 50V 100NP80M
2306	2238 586 59812	0603 50V 100NP80M
2307	2238 586 59812	0603 50V 100NP80M
2308	2238 586 59812	0603 50V 100NP80M
2309	2238 586 59812	0603 50V 100NP80M
2310	2238 586 59812	0603 50V 100NP80M
2311	2238 586 59812	0603 50V 100NP80M
2312	2238 586 59812	0603 50V 100NP80M
2313	2238 586 59812	0603 50V 100NP80M
2314	4822 124 80151	47µF 16V
2318	2238 586 59812	0603 50V 100NP80M
2319	2238 586 59812	0603 50V 100NP80M
2324	2238 586 59812	0603 50V 100NP80M
2325	2238 586 59812	0603 50V 100NP80M
2400	2238 586 59812	0603 50V 100NP80M
2401	2238 586 59812	0603 50V 100NP80M
2402	2238 586 59812	0603 50V 100NP80M
2403	2238 586 59812	0603 50V 100NP80M
2404	2238 586 59812	0603 50V 100NP80M
2405	2238 586 59812	0603 50V 100NP80M
2406	2238 586 59812	0603 50V 100NP80M
2407	2238 586 59812	0603 50V 100NP80M
2408	2238 586 59812	0603 50V 100NP80M
2409	2238 586 59812	0603 50V 100NP80M
2410	2238 586 59812	0603 50V 100NP80M
2411	2238 586 59812	0603 50V 100NP80M
2412	2238 586 59812	0603 50V 100NP80M
2413	2238 586 59812	0603 50V 100NP80M
2414	2238 586 59812	0603 50V 100NP80M
2415	2238 586 59812	0603 50V 100NP80M
2416	2238 586 59812	0603 50V 100NP80M
2417	2238 586 59812	0603 50V 100NP80M
2418	2238 586 59812	0603 50V 100NP80M
2419	2238 586 59812	0603 50V 100NP80M
2420	2238 586 59812	0603 50V 100NP80M
2421	2238 586 59812	0603 50V 100NP80M
2500	2238 586 59812	0603 50V 100NP80M
2501	2238 586 59812	0603 50V 100NP80M
2502	2238 586 59812	0603 50V 100NP80M
2503	2238 586 59812	0603 50V 100NP80M
2504	2238 586 59812	0603 50V 100NP80M
2505	4822 124 80151	47µF 16V
2506	2238 586 59812	0603 50V 100NP80M
2507	4822 124 80151	47µF 16V
2508	2238 586 59812	0603 50V 100NP80M
2509	2238 586 59812	0603 50V 100NP80M
2510	2238 586 59812	0603 50V 100NP80M
2511	4822 124 80151	47µF 16V
2512	4822 124 80151	47µF 16V
2514	4822 124 80151	47µF 16V
2515	4822 124 80151	47µF 16V
2516	5322 126 11583	10nF 10% 50V 0603
2517	5322 126 11583	10nF 10% 50V 0603
2518	4822 124 80151	47µF 16V
2519	2238 586 59812	0603 50V 100NP80M

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3100	4822 117 12925	47k 1% 0.063W 0603
3101	4822 117 12925	47k 1% 0.063W 0603
3102	4822 051 30103	10k 5% 0.062W
3103	4822 051 30103	10k 5% 0.062W
3104	4822 117 12925	47k 1% 0.063W 0603
3105	4822 051 30109	10Ω 5% 0.062W
3106	4822 051 30103	10k 5% 0.062W
3107	4822 051 30109	10Ω 5% 0.062W
3108	4822 051 30109	10Ω 5% 0.062W
3109	4822 117 12925	47k 1% 0.063W 0603
3110	4822 117 12925	47k 1% 0.063W 0603
3113	4822 051 30103	10k 5% 0.062W
3115	4822 051 30102	1k 5% 0.062W
3116	4822 117 12917	1Ω 5% 0.062W CASE0603
3117	4822 051 30109	10Ω 5% 0.062W
3118	4822 117 12925	47k 1% 0.063W 0603
3119	4822 117 12925	47k 1% 0.063W 0603
3120	4822 117 12925	47k 1% 0.063W 0603
3121	4822 117 12925	47k 1% 0.063W 0603
3122	4822 117 12925	47k 1% 0.063W 0603
3123	4822 117 12925	47k 1% 0.063W 0603
3124	4822 117 12925	47k 1% 0.063W 0603
3125	4822 117 12925	47k 1% 0.063W 0603
3126	4822 117 12925	47k 1% 0.063W 0603
3127	4822 117 12925	47k 1% 0.063W 0603
3128	4822 117 12925	47k 1% 0.063W 0603
3130	4822 117 12925	47k 1% 0.063W 0603
3131	4822 117 12925	47k 1% 0.063W 0603
3132	4822 117 12925	47k 1% 0.063W 0603
3133	4822 051 30223	22k 5% 0.062W
3134	4822 051 30223	22k 5% 0.062W
3136	4822 117 12917	1Ω 5% 0.062W CASE0603
3138	4822 051 30103	10k 5% 0.062W
3140	4822 051 30103	10k 5% 0.062W
3148	2322 704 66342	RST SM 0603 RC22H 6k34 PM1 R
3164	2322 734 65609	RST SM 0805 RC12H 56Ω PM1 R
3165	2322 734 65609	RST SM 0805 RC12H 56Ω PM1 R

3171	4822 051 30109	10Ω 5% 0.062W
3172	4822 051 30109	10Ω 5% 0.062W
3173	2322 734 65609	RST SM 0805 RC12H 56Ω PM1 R
3174	4822 051 30109	10Ω 5% 0.062W
3176	4822 051 30109	10Ω 5% 0.062W
3177	2322 704 65102	RST SM 0603 RC22H 5k1 PM1
3178	2322 734 65609	RST SM 0805 RC12H 56Ω PM1 R
3179	4822 051 30103	10k 5% 0.062W
3188	4822 051 30479	47Ω 5% 0.062W
3189	4822 051 30109	10Ω 5% 0.062W
3190	4822 051 30479	47Ω 5% 0.062W
3191	4822 051 30109	10Ω 5% 0.062W
3192	4822 117 12925	47k 1% 0.063W 0603
3197	4822 117 12925	47k 1% 0.063W 0603
3198	4822 117 12925	47k 1% 0.063W 0603
3199	4822 117 12925	47k 1% 0.063W 0603
3201	4822 051 30479	47Ω 5% 0.062W
3202	4822 051 30103	10k 5% 0.062W
3203	4822 051 30102	1k 5% 0.062W
3204	4822 051 30103	10k 5% 0.062W
3205	4822 117 12925	47k 1% 0.063W 0603
3206	4822 117 12925	47k 1% 0.063W 0603
3223	4822 051 30472	4k7 5% 0.062W
3224	4822 051 30331	330Ω 5% 0.062W
3225	4822 051 30109	10Ω 5% 0.062W
3300	4822 051 30109	10Ω 5% 0.062W
3301	4822 051 30102	1k 5% 0.062W
3303	4822 051 30102	1k 5% 0.062W
3305	4822 051 30102	1k 5% 0.062W
3306	4822 051 30102	1k 5% 0.062W
3307	4822 051 30102	1k 5% 0.062W
3312	4822 051 30109	10Ω 5% 0.062W
3313	4822 051 30103	10k 5% 0.062W
3314	4822 051 30103	10k 5% 0.062W
3315	4822 051 30339	33Ω 5% 0.062W
3317	4822 051 30339	33Ω 5% 0.062W
3318	4822 051 30339	33Ω 5% 0.062W
3319	4822 051 30339	33Ω 5% 0.062W
3320	4822 051 30479	47Ω 5% 0.062W
3321	4822 051 30479	47Ω 5% 0.062W
3322	4822 051 30479	47Ω 5% 0.062W
3325	4822 051 30479	47Ω 5% 0.062W
3327	4822 051 30479	47Ω 5% 0.062W
3328	4822 051 30103	10k 5% 0.062W
3329	4822 051 30103	10k 5% 0.062W
3330	4822 051 30479	47Ω 5% 0.062W
3331	4822 051 30479	47Ω 5% 0.062W
3400	4822 051 30103	10k 5% 0.062W
3401	4822 117 13573	NETW 4 X 47Ω 5% MNR14
3402	4822 117 13573	NETW 4 X 47Ω 5% MNR14
3403	4822 051 30479	47Ω 5% 0.062W
3404	4822 051 30479	47Ω 5% 0.062W
3405	4822 051 30479	47Ω 5% 0.062W
3502	4822 051 30339	33Ω 5% 0.062W
3504	4822 117 13576	NETW 4 X 33Ω 5% 1206
3505	4822 117 13576	NETW 4 X 33Ω 5% 1206
3506	4822 051 30339	33Ω 5% 0.062W
3510	4822 051 30479	47Ω 5% 0.062W
3518	4822 051 30101	100Ω 5% 0.062W
3519	4822 051 30101	100Ω 5% 0.062W
3520	4822 117 12891	220k 1% ERJ3Ω
3521	4822 117 12891	220k 1% ERJ3Ω
3524	4822 051 30339	33Ω 5% 0.062W
3525	4822 051 30339	33Ω 5% 0.062W
3526	4822 051 30339	33Ω 5% 0.062W
3527	4822 051 30339	33Ω 5% 0.062W

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5103	4822 157 11499	BLM11P600SPT
5106	4822 157 11499	BLM11P600SPT
5109	4822 157 11499	BLM11P600SPT
5110	4822 157 11499	BLM11P600SPT
5200	4822 157 11499	BLM11P600SPT
5300	4822 157 11499	BLM11P600SPT
5301	4822 157 11499	BLM11P600SPT
5302	4822 157 11499	BLM11P600SPT
5303	4822 157 11499	BLM11P600SPT
5304	4822 157 11499	BLM11P600SPT
5402	4822 157 11499	BLM11P600SPT
5403	4822 157 11499	BLM11P600SPT
5404	4822 157 11499	BLM11P600SPT
5500	4822 157 11499	BLM11P600SPT
5501	4822 157 11499	BLM11P600SPT
5502	4822 157 11499	BLM11P600SPT
5503	4822 157 11499	BLM11P600SPT

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6300	4822 209 17398	LD1117DT33

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7101	9352 683 02157	IC SM PDI1394P25BD (PHSE) Y
7103	9352 682 52557	IC SM PDI1394L40 (PHSE) Y
7201	4822 209 91023	UM62256EM-70LL
7202	5322 130 60159	BC846B
7204	9337 331 10215	FET SIG SM BST82 (PHSE) R
7207	5322 130 60159	BC846B
7208	9352 456 40115	IC SM 74HCT1G04GW (PHSE) R
7300	3104 123 96640	IC ROM XC17S30XL DVIO 1.5
7301	9322 166 64668	IC SM CY7C1019BV33-10VC(CYPR)R
7303	9322 169 90671	IC SM XCS30XL-4TQ144C (XILI) Y
7304	4822 242 10838	27MHZ 120P FX0-31FT
7307	3104 123 96620	IC FLASH PLL CY2071A DVIO 1.5
7308	3104 123 96620	IC FLASH PLL CY2071A DVIO 1.5
7402	9322 182 57668	MT4LC1M16E5DJ-5
7403	9322 182 57668	MT4LC1M16E5DJ-5
7404	9322 179 31671	IC SM NW700
7500	9352 424 20118	IC SM 74LVC04APW (PHSE) R
7505	9352 351 50118	IC SM 74LVC16244ADGG (PHSE) R
7506	9352 668 39118	IC SM UDA1334ATS/N2 (PHSE) R

Front DV Board DVDR890

Various

1000	2422 033 00363	CON BM H 4P F 0.8 B
1001	2422 025 17106	CON BM H 4P F 0.8 IEEE R

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2000	5322 126 10511	1nF 5% 50V
2001	5322 126 10511	1nF 5% 50V
2002	2020 557 90732	250V 4N7 PM10 R
2002	2222 580 19815	50V 330nF P8020 R
2003	2020 557 90732	250V 4N7 PM10 R
2003	2222 580 19815	50V 330nF P8020 R
2004	2020 557 90732	250V 4N7 PM10 R
2005	2020 557 90732	250V 4N7 PM10 R
2204	2222 867 15339	0603 50V 33P PM5
2205	2222 867 15339	0603 50V 33P PM5

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3000	4822 051 20105	1M 5% 0.1W

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5000	2422 549 44768	IND FXD SM EMI 100mH z 90R R
5001	2422 549 44768	IND FXD SM EMI 100mH z 90R R

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6000	4822 130 11395	TLMH3100
6001	9322 172 97668	DIO SUP SM6T39CA (ST00) R

Digital Board 1.5

Various

1100	2422 025 17018	CON BM V 15P F 1.00 FFC 0.3 R
1101	2422 025 17018	CON BM V 15P F 1.00 FFC 0.3 R
1200	2422 025 16794	CON BM V 7P F 1.00 FFC 0.3 R
1500	2422 543 01115	RES XTL SM 24M576 12P CX-11F R
1600	2422 025 16729	CON BM V 10P F 1.00 FFC 0.3 R
1601	2422 025 16389	CON BM V 22P F 1.00 FFC 0.3 R
1602	2422 025 16389	CON BM V 22P F 1.00 FFC 0.3 R
1603	2422 025 16939	CON BM V 60P F 0.80 84616 R

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2100	2238 586 59812	0603 50V 100NP80M
2101	2238 586 59812	0603 50V 100NP80M
2102	2238 586 59812	0603 50V 100NP80M
2103	2238 586 59812	0603 50V 100NP80M
2104	2238 586 59812	0603 50V 100NP80M
2105	2238 586 59812	0603 50V 100NP80M
2106	2238 586 59812	0603 50V 100NP80M
2107	2238 586 59812	0603 50V 100NP80M
2108	2238 586 59812	0603 50V 100NP80M
2109	2238 586 59812	0603 50V 100NP80M
2110	2238 586 59812	0603 50V 100NP80M
2111	2238 586 59812	0603 50V 100NP80M
2112	2238 586 59812	0603 50V 100NP80M
2113	2238 586 59812	0603 50V 100NP80M
2114	2238 586 59812	0603 50V 100NP80M
2115	2238 586 59812	0603 50V 100NP80M
2116	2238 586 59812	0603 50V 100NP80M
2117	2238 586 59812	0603 50V 100NP80M
2118	2238 586 59812	0603 50V 100NP80M
2119	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2120	2238 586 59812	0603 50V 100NP80M
2121	2238 586 59812	0603 50V 100NP80M
2122	2238 586 59812	0603 50V 100NP80M
2123	2238 586 59812	0603 50V 100NP80M
2124	2238 586 59812	0603 50V 100NP80M
2125	2238 586 59812	0603 50V 100NP80M
2126	2238 586 59812	0603 50V 100NP80M
2127	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2128	3198 016 31020	0603 25V 1nF
2129	4822 126 13956	68pF 5% 63V CASE 0603
2130	3198 030 82280	EL SM 50V 2U2 PM20 COL R
2131	5322 124 41945	22µF 20% 35V
2132	2238 586 59812	0603 50V 100NP80M
2135	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2136	4822 126 11785	0603 50V 47P PM5
2137	2238 586 59812	0603 50V 100NP80M
2139	2238 586 59812	0603 50V 100NP80M
2141	4822 126 11785	0603 50V 47P PM5
2146	2238 586 59812	0603 50V 100NP80M
2200	3198 016 31020	0603 25V 1nF
2201	4822 126 14494	22nF 10% 25V 0603
2202	2238 586 59812	0603 50V 100NP80M
2203	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2204	2222 867 15339	0603 50V 33P PM5
2205	2238 586 59812	0603 50V 100NP80M
2206	2238 586 59812	0603 50V 100NP80M
2207	2222 867 15339	0603 50V 33P PM5
2208	2238 586 59812	0603 50V 100NP80M
2209	2238 586 59812	0603 50V 100NP80M
2210	2238 586 59812	0603 50V 100NP80M
2211	2238 586 59812	0603 50V 100NP80M
2212	2238 586 59812	0603 50V 100NP80M
2213	2238 586 59812	0603 50V 100NP80M
2214	2238 586 59812	0603 50V 100NP80M
2215	2238 586 59812	0603 50V 100NP80M
2216	2238 586 59812	0603 50V 100NP80M
2217	2238 586 59812	0603 50V 100NP80M
2218	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2220	2238 586 59812	0603 50V 100NP80M
2221	2238 586 59812	0603 50V 100NP80M
2222	2238 586 59812	0603 50V 100NP80M
2223	2238 586 59812	0603 50V 100NP80M
2224	2238 586 59812	0603 50V 100NP80M
2225	2238 586 59812	0603 50V 100NP80M
2226	2238 586 59812	0603 50V 100NP80M
2227	2238 586 59812	0603 50V 100NP80M
2228	2238 586 59812	0603 50V 100NP80M
2229	2238 586 59812	0603 50V 100NP80M
2230	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2231	2238 586 59812	0603 50V 100NP80M
2300	2238 586 59812	0603 50V 100NP80M
2301	2238 586 59812	0603 50V 100NP80M
2302	2238 586 59812	0603 50V 100NP80M
2303	2238 586 59812	0603 50V 100NP80M

2304	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2305	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2306	2238 586 59812	0603 50V 100NP80M
2307	2238 586 59812	0603 50V 100NP80M
2308	2238 586 59812	0603 50V 100NP80M
2309	2238 586 59812	0603 50V 100NP80M
2310	2238 586 59812	0603 50V 100NP80M
2311	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2312	2238 586 59812	0603 50V 100NP80M
2402	2238 586 59812	0603 50V 100NP80M
2403	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2404	2238 586 59812	0603 50V 100NP80M
2405	2238 586 59812	0603 50V 100NP80M
2406	2238 586 59812	0603 50V 100NP80M
2407	2238 586 59812	0603 50V 100NP80M
2408	2238 586 59812	0603 50V 100NP80M
2409	2238 586 59812	0603 50V 100NP80M
2410	2238 586 59812	0603 50V 100NP80M
2411	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2412	2238 586 59812	0603 50V 100NP80M
2413	2238 586 59812	0603 50V 100NP80M
2414	2238 586 59812	0603 50V 100NP80M
2415	2238 586 59812	0603 50V 100NP80M
2416	2238 586 59812	0603 50V 100NP80M
2417	2238 586 59812	0603 50V 100NP80M
2418	2238 586 59812	0603 50V 100NP80M
2419	2238 586 59812	0603 50V 100NP80M
2420	2238 586 59812	0603 50V 100NP80M
2421	2238 586 59812	0603 50V 100NP80M
2422	2238 586 59812	0603 50V 100NP80M
2423	2238 586 59812	0603 50V 100NP80M
2424	2238 586 59812	0603 50V 100NP80M
2425	2238 586 59812	0603 50V 100NP80M
2426	2238 586 59812	0603 50V 100NP80M
2427	2238 586 59812	0603 50V 100NP80M
2428	2238 586 59812	0603 50V 100NP80M
2429	2238 586 59812	0603 50V 100NP80M
2430	2238 586 59812	0603 50V 100NP80M
2431	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2432	2238 586 59812	0603 50V 100NP80M
2433	2238 586 59812	0603 50V 100NP80M
2434	2238 586 59812	0603 50V 100NP80M
2435	2238 586 59812	0603 50V 100NP80M
2436	2238 586 59812	0603 50V 100NP80M
2437	2238 586 59812	0603 50V 100NP80M
2438	2238 586 59812	0603 50V 100NP80M
2439	2238 586 59812	0603 50V 100NP80M
2440	2238 586 59812	0603 50V 100NP80M
2441	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2442	2238 586 59812	0603 50V 100NP80M
2443	4822 122 33741	10pF 10% 50V
2444	2238 586 59812	0603 50V 100NP80M
2446	3198 016 31020	0603 25V 1nF
2500	3198 016 31020	0603 25V 1nF
2501	2238 586 59812	0603 50V 100NP80M
2502	2238 586 59812	0603 50V 100NP80M
2503	2238 586 59812	0603 50V 100NP80M
2504	2238 586 59812	0603 50V 100NP80M
2505	2238 586 59812	0603 50V 100NP80M
2506	2238 586 59812	0603 50V 100NP80M
2507	2238 586 59812	0603 50V 100NP80M
2508	2238 586 59812	0603 50V 100NP80M
2509	2238 586 59812	0603 50V 100NP80M
2510	4822 122 33761	22pF 5% 50V
2510	4822 126 14507	18pF 5% 50V 0603
2511	4822 122 33741	10pF 10% 50V
2511	4822 126 14507	18pF 5% 50V 0603
2512	2238 586 59812	0603 50V 100NP80M
2513	2238 586 59812	0603 50V 100NP80M
2514	2238 586 59812	0603 50V 100NP80M
2515	2238 586 59812	0603 50V 100NP80M
2516	2238 586 59812	0603 50V 100NP80M
2517	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2518	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2519	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2520	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2521	2238 586 59812	0603 50V 100NP80M
2522	2238 586 59812	0603 50V 100NP80M
2523	2238 586 59812	0603 50V 100NP80M
2524	2238 586 59812	0603 50V 100NP80M
2525	2238 586 59812	0603 50V 100NP80M
2526	2238 586 59812	0603 50V 100NP80M
2527	2238 586 59812	0603 50V 100NP80M
2528	2238 586 59812	0603 50V 100NP80M
2529	2238 586 59812	0603 50V 100NP80M
2530	2238 586 59812	0603 50V 100NP80M
2531	2238 586 59812	0603 50V 100NP80M
2532	2238 586 59812	0603 50V 100NP80M
2533	2238 586 59812	0603 50V 100NP80M
2534	2238 586 59812	0603 50V 100NP80M
2535	2238 586 59812	0603 50V 100NP80M
2536	2238 586 59812	0603 50V 100NP80M
2537	2238 586 59812	0603 50V 100NP80M
2538	2238 586 59812	0603 50V 100NP80M
2539	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2540	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2541	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2542	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2543	2238 586 59812	0603 50V 100NP80M
2544	2238 586 59812	0603 50V 100NP80M
2565	4822 122 33753	150pF 5% 50V
2600	2238 586 59812	0603 50V 100NP80M
2601	4822 126 11785	0603 50V 47P PM5
2602	4822 126 11785	0603 50V 47P PM5
2605	2238 586 59812	0603 50V 100NP80M
2606	4822 126 11785	0603 50V 47P PM5
2607	4822 126 11785	0603 50V 47P PM5
2608	2238 586 59812	0603 50V 100NP80M
2609	2238 586 59812	0603 50V 100NP80M
2610	2238 586 59812	0603 50V 100NP80M
2611	4822 126 11785	0603 50V 47P PM5
2612	4822 126 11785	0603 50V 47P PM5
2613	2238 586 59812	0603 50V 100NP80M
2614	2238 586 59812	0603 50V 100NP80M
2615	2238 586 59812	0603 50V 100NP80M
2616	4822 126 11785	0603 50V 47P PM5
2617	4822 126 11785	0603 50V 47P PM5
2618	2238 586 59812	0603 50V 100NP80M
2619	2238 586 59812	0603 50V 100NP80M
2620	2238 586 59812	0603 50V 100NP80M
2621	4822 126 11785	0603 50V 47P PM5
2622	4822 126 11785	0603 50V 47P PM5
2625	2238 586 59812	0603 50V 100NP80M
2626	4822 126 11785	0603 50V 47P PM5
2627	4822 126 11785	0603 50V 47P PM5
2628	2238 586 59812	0603 50V 100NP80M
2629	2238 586 59812	0603 50V 100NP80M
2630	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2632	2238 586 59812	0603 50V 100NP80M
2633	2238 586 59812	0603 50V 100NP80M
2634	4822 126 14494	22nF 10% 25V 0603
2635	2238 586 59812	0603 50V 100NP80M
2636	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2722	2238 586 59812	0603 50V 100NP80M
2900	2238 586 59812	0603 50V 100NP80M
2901	2238 586 59812	0603 50V 100NP80M
2902	2238 586 59812	0603 50V 100NP80M
2903	2238 586 59812	0603 50V 100NP80M
2904	2238 586 59812	0603 50V 100NP80M
2906	2238 586 59812	0603 50V 100NP80M
2907	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2908	2238 586 59812	0603 50V 100NP80M
2909	4822 126 14247	0603 50V 1N5 COL R
2911	2238 586 59812	0603 50V 100NP80M
2912	4822 126 14247	0603 50V 1N5 COL R
2914	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2915	2238 586 59812	0603 50V 100NP80M
2916	4822 126 14494	22nF 10% 25V 0603

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3100	4822 051 30103	10k 5% 0.062W
3101	4822 051 30222	2k2 5% 0.062W
3102	4822 051 30103	10k 5% 0.062W
3104	4822 051 30479	47Ω 5% 0.062W
3105	4822 051 30479	47Ω 5% 0.062W
3106	4822 051 30479	47Ω 5% 0.062W
3107	4822 051 30109	10Ω 5% 0.062W
3108	4822 051 30479	47Ω 5% 0.062W
3109	4822 051 30479	47Ω 5% 0.062W
3110	4822 051 30479	47Ω 5% 0.062W
3111	4822 051 30472	4k7 5% 0.062W
3112	4822 051 30472	4k7 5% 0.062W
3113	4822 051 30472	4k7 5% 0.062W
3114	4822 051 30472	4k7 5% 0.062W
3115	4822 051 30103	10k 5% 0.062W
3116	4822 051 30103	10k 5% 0.062W
3117	4822 117 12139	22Ω 5% 0.062W
3118	4822 117 12139	22Ω 5% 0.062W
3119	4822 051 30222	2k2 5% 0.062W
3120	4822 051 30153	15k 5% 0.062W
3121	4822 117 12917	1Ω 5% 0.062W CASE0603
3122	4822 051 30123	12k 5% 0.062W
3123	2322 704 62002	RST SM 0603 RC22H 2k PM1 R
3124	2322 704 63002	RST SM 0603 RC22H 3k PM1 R
3125	4822 117 12139	22Ω 5% 0.062W
3126	4822 117 12891	220k 1% ERJ3Ω
3127	4822 051 30479	47Ω 5% 0.062W
3128	4822 051 30479	47Ω 5% 0.062W
3129	4822 051 30479	47Ω 5% 0.062W
3130	2120 611 00019	NTC SM 0603 0W1 4k7 PM5 R
3131	4822 117 12917	1Ω 5% 0.062W CASE0603
3132	4822 117 12917	1Ω 5% 0.062W CASE0603
3133	4822 117 12917	1Ω 5% 0.062W CASE0603
3134	4822 117 12917	1Ω 5% 0.062W CASE0603
3135	4822 117 12917	1Ω 5% 0.062W CASE0603
3136	4822 117 12917	1Ω 5% 0.062W CASE0603
3137	4822 051 30472	4k7 5% 0.062W
3138	4822 051 30472	4k7 5% 0.062W
3200	4822 051 30332	3k3 5% 0.062W
3201	4822 051 30152	1k5 5% 0.062W
3202	4822 051 30103	10k 5% 0.062W
3203	4822 117 12139	22Ω 5% 0.062W
3204	4822 051 30101	100Ω 5% 0.062W
3205	4822 051 30101	100Ω 5% 0.062W
3206	4822 051 30101	100Ω 5% 0.062W
3207	4822 051 30103	10k 5% 0.062W
3208	4822 117 12139	22Ω 5% 0.062W
3209	4822 051 30103	10k 5% 0.062W
3211	4822 051 30222	2k2 5% 0.062W
3212	4822 051 30152	1k5 5% 0.062W
3213	4822 051 30103	10k 5% 0.062W
3214	4822 051 30103	10k 5% 0.062W
3215	4822 051 30103	10k 5% 0.062W
3216	4822 051 30103	10k 5% 0.062W
3217	4822 051 30101	100Ω 5% 0.062W
3218	4822 051 30101	100Ω 5% 0.062W
3219	4822 051 30103	10k 5% 0.062W
3220	4822 051 30103	10k 5% 0.062W
3221	4822 051 30103	10k 5% 0.062W
3222	4822 051 30103	10k 5% 0.062W
3223	4822 051 30222	2k2 5% 0.062W
3224	4822 051 30103	10k 5% 0.062W
3225	4822 051 30103	10k 5% 0.062W
3226	4822 051 30103	10k 5% 0.062W
3227	4822 117 12139	22Ω 5% 0.062W
3228	4822 117 12139	22Ω 5% 0.062W
3229	2322 704 61303	RST SM 0603 RC22H 13k PM1 R
3230	2322 704 61303	RST SM 0603 RC22H 13k PM1 R
3231	5322 117 13042	3k9 1% 0.063W 0603 RC22H
3232	5322 117 13042	3k9 1% 0.063W 0603 RC22H
3234	3198 031 14720	RST NETW 1206 4X4k7 PM5 COL R
3235	4822 117 12917	1Ω 5% 0.062W CASE0603
3236	4822 117 13576	NETW 4 X 33Ω 5% 1206
3237	4822 117 13576	NETW 4 X 33Ω 5% 1206
3300	4822 051 30479	47Ω 5% 0.062W
3301	4822 051 30479	47Ω 5% 0.062W
3400	4822 051 30101	100Ω 5% 0.062W
3401	4822 051 30101	100Ω 5% 0.062W
3403	4822 051 30103	10k 5% 0.062W
3404	4822 051 30008	0Ω jumper
3405	4822 051 30332	3k3 5% 0.062W
3406	4822 051 30479	47Ω 5% 0.062W
3407	4822 051 30181	180Ω 5% 0.062W
3408	4822 117 12139	22Ω 5% 0.062W
3409	4822 117 12139	22Ω 5% 0.062W
3410	4822 117 12139	22Ω 5% 0.062W
3500	4822 051 30101	100Ω 5% 0.062W
3501	4822 051 30101	100Ω 5% 0.062W
3502	4822 051 30222	2k2 5% 0.062W
3503	4822 051 30102	1k 5% 0.062W
3504	4822 051 30681	680Ω 5% 0.062W
3505	4822 117 12139	22Ω 5% 0.062W
3506	4822 051 30222	2k2 5% 0.062W
3507	4822 051 30472	4k7 5% 0.062W
3508	4822 051 30103	10k 5% 0.062W
3513	4822 051 30681	680Ω 5% 0.062W
3515	4822 117 12917	1Ω 5% 0.062W CASE0603
3600	2322 704 65609	RST SM 0603 RC22H 56Ω PM1 R
3601	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3602	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3603	4822 051 30102	1k 5% 0.062W
3604	4822 051 30101	100Ω 5% 0.062W

3605	4822 117 12917	1Ω 5% 0.062W CASE0603
3606	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3607	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3608	4822 051 30102	1k 5% 0.062W
3610	4822 117 12917	1Ω 5% 0.062W CASE0603
3611	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3612	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3613	4822 051 30102	1k 5% 0.062W
3615	4822 051 30101	100Ω 5% 0.062W
3616	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3617	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3618	4822 051 30102	1k 5% 0.062W
3619	4822 051 30561	560Ω 5% 0.062W
3620	4822 051 30222	2k2 5% 0.062W
3621	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3622	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3623	4822 051 30101	100Ω 5% 0.062W
3624	4822 051 30102	1k 5% 0.062W
3625	4822 051 30101	100Ω 5% 0.062W
3626	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3627	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3628	4822 051 30102	1k 5% 0.062W
3629	4822 051 30181	180Ω 5% 0.062W
3630	4822 051 30181	180Ω 5% 0.062W
3631	4822 117 12917	1Ω 5% 0.062W CASE0603
3632	4822 051 30561	560Ω 5% 0.062W
3633	4822 051 30561	560Ω 5% 0.062W
3635	4822 051 30101	100Ω 5% 0.062W
3636	4822 051 30181	180Ω 5% 0.062W
3637	4822 051 30101	100Ω 5% 0.062W
3638	4822 051 30222	2k2 5% 0.062W
3900	4822 051 30103	10k 5% 0.062W
3901	4822 117 12139	22Ω 5% 0.062W
3902	4822 117 12925	47k 1% 0.063W 0603
3903	4822 117 13632	100k 1% 0603 0.62W
3904	4822 117 12139	22Ω 5% 0.062W
3906	4822 051 30479	47Ω 5% 0.062W
3908	4822 117 12139	22Ω 5% 0.062W
3910	4822 051 30101	100Ω 5% 0.062W
3911	4822 051 30103	10k 5% 0.062W
3913	4822 051 30682	6k8 5% 0.062W
3914	4822 051 30479	47Ω 5% 0.062W
3915	4822 051 30479	47Ω 5% 0.062W
3916	4822 117 13632	100k 1% 0603 0.62W
3917	4822 117 12139	22Ω 5% 0.062W
3918	4822 117 13632	100k 1% 0603 0.62W
3919	4822 051 30101	100Ω 5% 0.062W
3920	4822 117 12139	22Ω 5% 0.062W
3921	4822 051 30103	10k 5% 0.062W
3922	4822 051 30682	6k8 5% 0.062W
3923	4822 117 13632	100k 1% 0603 0.62W
3924	4822 051 30152	1k5 5% 0.062W
3925	4822 051 30472	4k7 5% 0.062W

5100	4822 157 11717	BLM31P500SPT
5101	4822 157 11717	BLM31P500SPT
5102	4822 157 11499	BLM11P600SPT
5103	4822 157 11499	BLM11P600SPT
5200	4822 157 11499	BLM11P600SPT
5201	4822 157 11499	BLM11P600SPT
5202	4822 157 11499	BLM11P600SPT
5203	4822 157 11499	BLM11P600SPT
5204	4822 157 11499	BLM11P600SPT
5205	4822 157 11499	BLM11P600SPT
5207	4822 157 11499	BLM11P600SPT
5208	4822 157 11499	BLM11P600SPT
5209	4822 157 11499	BLM11P600SPT
5300	4822 157 11499	BLM11P600SPT
5302	4822 157 11499	BLM11P600SPT
5400	4822 157 11499	BLM11P600SPT
5402	4822 157 11499	BLM11P600SPT
5403	4822 157 11499	BLM11P600SPT
5404	4822 157 11499	BLM11P600SPT
5500	4822 157 11499	BLM11P600SPT
5501	4822 157 11499	BLM11P600SPT
5502	4822 157 11499	BLM11P600SPT
5503	4822 157 11499	BLM11P600SPT
5504	4822 157 11499	BLM11P600SPT
5505	4822 157 11499	BLM11P600SPT
5506	4822 157 11499	BLM11P600SPT
5507	4822 157 11499	BLM11P600SPT
5508	4822 157 11499	BLM11P600SPT
5600	4822 157 70651	12µH (NL322522T-120J)
5601	4822 157 70651	12µH (NL322522T-120J)
5602	4822 157 70651	12µH (NL322522T-120J)
5603	4822 157 70651	12µH (NL322522T-120J)
5604	4822 157 70651	12µH (NL322522T-120J)
5605	4822 157 70651	12µH (NL322522T-120J)
5606	4822 157 70649	4.7µH (NL322522T-4R7J)
5607	4822 157 70649	4.7µH (NL322522T-4R7J)
5900	4822 157 11717	BLM31P500SPT
5901	4822 157 11717	BLM31P500SPT
5903	4822 157 11499	BLM11P600SPT
5904	4822 157 11717	BLM31P500SPT
5905	4822 157 11499	BLM11P600SPT
5907	4822 157 11499	BLM11P600SPT

6500	4822 130 80622	BAT54
6900	4822 130 80622	BAT54

7100	9352 692 48557	IC SM SAA7333HL/M1 (PHSE) Y
7101	9322 166 67668	IC SM MT48LC4M16A2TG-7E(MRN0)R
7102	5322 209 16384	PC74HCT9046AD
7103	9322 170 16685	IC SM NC7SZ58 (FSC0) R
7104	9352 456 50115	HC1G04
7200	9322 169 81671	STI5508EVB
7201	9322 130 41668	IC SM M24C64-WMN6 (ST00) R
7202	4822 209 30212	PC74HCT125T
7203	9322 142 88668	IC SM LF25CDT (ST00) R
7300	9322 166 67668	IC SM MT48LC4M16A2TG-7E(MRN0)R
7303	9352 499 60118	IC SM 74LVC00AD (PHSE) R
7402	9322 166 67668	IC SM MT48LC4M16A2TG-7E(MRN0)R
7403	9352 701 80557	IC SM SAA6752HS/V101 (PHSE) Y
7404	9322 142 88668	IC SM LF25CDT (ST00) R
7500	9352 673 95518	IC SM SAA7118E/V1 (PHSE) R
7501	9352 500 60118	IC SM 74LVC32AD (PHSE) R
7502	5322 209 71589	74HC74D
7504	5322 130 60159	BC846B
7600	5322 130 60159	BC846B
7601	5322 130 60159	BC846B
7602	5322 130 60159	BC846B
7603	5322 130 60159	BC846B
7604	5322 130 60159	BC846B
7605	5322 130 60159	BC846B
7606	5322 130 60159	BC846B
7702	9352 501 00118	IC SM 74LVC86ADB (PHSE) R
7900	9322 151 71668	IC SM MK2703STR (MICL) R
7901	5322 130 60159	BC846B
7902	9322 165 15685	IC SM NCP303LSN30 (ONSE) R
7904	4822 209 16399	74LVC04AD
7905	5322 209 71568	PC74HCT14T
7906	4822 242 10838	27MHZ 120P FX0-31FT